Data Sheet

AD1030

High Precision Analog Front End with TEC/PMIC

FEATURES

- Analog input and output
  - Multichannel, 12-bit, 1 MSPS ADC
    - Up to 10 external channels
    - Power, VDAC, IDAC, and temperature monitor internal channels
    - Single-ended and differential mode
    - 0 V to V_{REF} analog input range
    - Input buffer included
    - Digital comparators
- Nine, 12-bit voltage output DACs
  - 4-channel, selectable output range
    - 0 V to 2.5 V or AVDD − 0.1
    - AVDDNEG + 0.2 or −2.5 V to −0 V
  - 4-channel, 0 V to 2.5 V or AVDD − 0.2 V
  - 1-channel, 0 V to 2.5 V
- Four low noise, 12-bit IDACs
  - Configurable output range: 50 mA, 100 mA, or 150 mA
  - Fast shut down with external IDACDIS pin
- 2 voltage comparators with adjustable hysteresis voltage
- TEC controller
  - Optional buck or LDO regulator mode if not using TEC
  - Maximum heating and cooling current: 1.3 A
  - Current and voltage monitoring and protection
  - Over 90% efficient
  - Soft start function
- Digital Interface
  - 1× SPI, 3.3 V, 40 MHz
  - 1× I^2C, 3.3 V, 100 kHz, 400 kHz, and 1 MHz
  - 14x GPIO shared with analog input and output
- Power
  - Multiple supplies, separate IDAC power supply to save power
    - AVDDx, IOVDD, and PVDDTECx: 2.85 V to 3.63 V
    - AVDDNEG: −1.8 V to −3.63 V
    - PVDDIDACx: 1.60 V to AVDDx
- Packages and temperature range
  - 3.750 mm × 3.750 mm, 0.40 mm pitch, 61-ball WLCSP
  - Fully specified for T_J = –40°C to +125°C

APPLICATIONS

- Optical networking–100G/200G/400G or higher speed optical modules

GENERAL DESCRIPTION

The AD1030 is an analog front end (AFE) that includes a high precision analog-to-digital converter (ADC), voltage output digital-to-analog converters (VDACs), current output digital-to-analog converters (IDACs), thermoelectric cooler (TEC) controller, and analog comparators.

The ADC signal chain contains two analog comparator channels, 10 external voltage inputs, VDAC voltage and current monitor channels, IDAC voltage and current monitor channels, a precharge buffer, and a 1 MSPS successive approximation register (SAR) ADC.

The AD1030 provides four IDAC channels. These are low noise, low drift current sources with programmable full-scale output ranges (50 mA, 100 mA, or 150 mA). Each IDAC channel has 12-bit resolution.

There are 9×, 12-bit VDAC outputs. Four of these VDACs (Channel 0 to Channel 3) support either a positive voltage range of 0 V to 2.5 V or a negative range from 0 V to –2.5 V. These ranges can be extended to 0 V to AVDD and 0 V to AVDDNEG.

Channel 4 to Channel 7 of the VDACs support a positive voltage range of 0 V to 2.5 V. VDAC Channel 8 supports a positive voltage range of 0 V to 2.5 V. Optionally, Channel 4 to Channel 7 of the VDACs can support an output range of 0 V to AVDD.

The AD1030 also integrates a TEC controller with a heating and cooling current up to 1.3 A, is over 90% efficient, and supports a soft start function.

Use the 4-wire serial port interface (SPI) for up to 40 MHz or the 2-wire I^2C interface for up 1 MHz to configure each functional block and to collect the ADC data.

Note that throughout this data sheet, multifunction pins, such as VDACP0/AIN4/GPIO0, are referred to either by the entire pin name or by a single function of the pin, for example, AIN4, when only that function is relevant.

For more information on the AD1030, contact InfoOpticalNetwork@analog.com.

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NOTES