Precision Analog Microcontroller, 12-Bit Analog I/O, ARM7TDMI MCU with Enhanced IRQ Handler

Silicon Anomaly

ADuC7023

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7023 MicroConverter® Revision A and Revision C silicon. The anomalies listed apply to all ADuC7023 packaged material branded as follows:

First Line ADuC7023
Third Line A50

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuC7023 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Issues
A	0	All silicon branded A50	Released	Rev. C	10

ADuC7023 PERFORMANCE ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Issues
A	0	All silicon branded A50	Released	Rev. C	3

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FUNCTIONALITY ISSUES

Table 1. ADC Conversion—Single Software Edge Triggered Mode [er001]

Background	The ADC can be set to single software conversion mode by setting ADCCON[2:0] = 011b. The ADC can also be configured in continuous software conversion mode by setting ADCCON[2:0] = 100b. The ADC is then triggered by the $\overline{CONV_{START}}$ pin. ADCCON[13] configures the $\overline{CONV_{START}}$ pin for level or edge triggered mode. When ADCCON[13] = 0, a low level on the $\overline{CONV_{START}}$ pin triggers an ADC conversion. When ADCCON[13] = 1, a rising edge on the $\overline{CONV_{START}}$ pin triggers an ADC conversion.
Issue	After a single conversion when in single software conversion mode, ADCCON[2:0] changes to 000b automatically. Extra ADC triggers can occur if the $\overline{CONV_{START}}$ pin is low and ADCCON[13] = 0.
Workaround	When using single conversion mode, set ADCCON[13] = 1 to configure the $\overline{CONV_{START}}$ pin for edge-based triggered mode.
Related Issues	None.

Table 2. ADC Conversion—$\overline{CONV_{START}}$ Edge Triggered Mode [er002]

Background	An ADC conversion can be triggered by a rising edge on the $\overline{CONV_{START}}$ if ADCCON[13] is set to 1, or by a low level on the $\overline{CONV_{START}}$ pin if ADCCON[13] is cleared to 0.
Issue	ADC conversions triggered by a rising edge of the $\overline{CONV_{START}}$ are not reliable.
Workaround	Use PLA conversion mode instead to implement an edge triggered-based ADC conversion.
Related Issues	None.

Table 3. ADC Conversion—PLA Edge Triggered Mode [er003]

Background	An ADC conversion can be set to PLA positive edge triggered mode by setting ADCCON[13] = 1 and ADCCON[2:0] = 101. Clearing ADCCON[13] enables PLA low level triggered mode.
Issue	An ADC conversion by PLA edge triggered mode is not reliable.
Workaround	Configure the PLA element output through another PLA flip-flop with ULCK as its clock. This ensures that the ADC is triggered by the PLA edge when the clock divide (CD) bits in POWCON0 is less than 5.
Related Issues	None.

Table 4. SPI Bit Rate Issue [er004]

Background	In SPI master mode, polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register. The maximum speed of the SPI clock is independent from the clock divider bits.
Issue	When SPICON[6] = 0, transfers are initiated in master mode by reading the SPIRX register. When SPICON[6] = 0, SPIDIV must not be set to a value greater than 0x2 because bytes may be lost.
Workaround	Set the SPIDIV register to a value less than or equal to 0x32. Alternatively, set SPICON[6] = 1 to initiate transfers on a write to SPITX. In this mode, all values of SPIDIV are valid.
Related Issues	None.

Table 5. Internal Pull-Up Resistor on P2.0 Cannot be Disabled on 40-Lead Package [er005]

Background	The GPIO has internal weak pull-up resistors that can be disabled by setting GPxPAR. P2.0 can also be configured as Differential Analog Input 12, ADC12, by setting GP2CON = 0x1 (Bit 0 = 1 and Bit 1 = 0).
Issue	When P2.0 is set as Analog Input ADC12, its internal pull-up resistor cannot be disabled by setting GP2PAR. The input leakage is large and affects the ADC result when this channel is selected.
Workaround	Select other ADC channels through the ADCCP MMR.
Related Issues	None.

Table 6. Disabling I²C Interface in Slave Mode When a Transfer is in Progress [er006]

Background	The I2CxSCON register Bit 0 enables/disables the I²C slave interface. I2CxSSTA Register Bit 6 indicates if the I²C slave interface is busy or not.
Issue	If I²C slave mode is enabled (I2CxSCON Bit 0 = 1), and a transfer is in progress with the master, then I2CxSCON Bit0 should not be cleared to 0 to disable the I²C slave interface until Bit 6 of I2CxSSTA (the I²C busy bit) is cleared. When I2CxSCON Bit0 is cleared to 0 and the busy bit is still set, the ADuC7023 may drive the SDA pin low indefinitely. Once this condition occurs, the ADuC7023 will not release the SDA unless a hardware reset condition occurs.
Workaround	When disabling I²C slave mode by writing to I2CxSCON Bit0, first set I2CxMCON Bit0 = 1 to enable master mode. Then, disable the slave mode by clearing I2CxSCON Bit0. Finally, clear I2CxMCON Bit0.
Related Issues	None.

Table 7. Operation of SPI in Slave Mode [er007]

Background	When in SPI slave mode, the ADuC7023 expects the number of clock pulses from the master to be divisible by 8 when the Chip Select pin is active. The internal bit shift counter does not reset when the chip select pin is deasserted.
Issue	If the number of clocks from the master is not divisible by 8 when the chip select is active, this can result in incorrect data being received or transmitted by the ADuC7023 as the bit shift counter will not be at 0 for later transfers. The internal bit shift counter for the transmit or receive buffers can only be reset by a hardware, software, or watchdog reset condition.
Workaround	Always ensure that the number of SPI clocks are divisible by 8 when the ADuC7023 chip select is active.
Related Issues	None.

Table 8. Timer0 in Periodic Mode with Internal 32 kHz Clock [er008]

Background	In periodic mode, the internal counter decrements/increments from the value in the load register (T0LD MMR) until zero/full scale and starts again at the value stored in the load register. The value of a counter can be read at any time by accessing its value register (T0VAL).
Issue	The first timer interrupt occurs only after a full 16-bit countdown. After the countdown, the T0LD value is copied into T0VAL as expected. This issue occurs only when the 32 kHz oscillator is serving as the timer source.
Workaround	None.
Related Issues	None.

Table 9. I²C Slave Not Releasing the Bus [er009]

Background	When an I²C read request happens, if the slave's Tx FIFO is empty, the slave should NACK the masters' request. Then it should release the bus, allowing the master to generate a stop condition.
Issue	If the slave's Tx FIFO is loaded with a byte who's MSB is 0 just on the rising edge of SCL for the ACK/NACK, the slave will pull the SDA low and hold the line until the device is reset.
Workaround	Make sure the Tx FIFO is always loaded on time by preloading Tx FIFO in the preceding Rx interrupt.
Related Issues	None.

Table 10. I²C Clock Stretch Issue [er0010]

Background	Clock stretching is a feature that allows a device to halt the I²C bus temporarily by holding SCL low. Bit 6 of the I2CxSCON register enables clock stretching in slave mode. Bit 3 of the I2CxMCON register enables clock stretching in master mode.
Issue	Writing to I2CxSCON Bit 6 or to I2CxMCON Bit 3 on the rising edge of SCL can cause a glitch that may be interpreted by other devices as a real clock edge and might hang the bus.
Workaround	Do not enable clock stretching.
Related Issues	None.

PERFORMANCE ISSUES

Table 11. JTAG Clock Limitation [pr001]

Background	The JTAG clock speed is limited.
Issue	JTAG speed requires TCK < UCLK/((2^{CD}) × 6); that is, TCK should be changed according to how CD is set. If TCK is greater than the limitation, then JTAG cannot download until the JTAG pod (programming device) is at the correct TCK speed.
Workaround	This must be set up manually. The default kernel setting for the CPU clock is CD = 3 (5.22 MHz). Therefore, a JTAG clock speed limitation of 800 kHz or less must be maintained.
Related Issues	None.

Table 12. ADC and DAC Reference Selection Limitation [pr002]

Background	The ADuC7023 provides an on-chip band gap reference of 2.5 V that can be used for the ADC and DACs. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions.
Issue	When REFCON = 0x00, the internal 2.5 V reference is unstable; that is, when ADC uses the external reference (REFCON = 0x00) and the DACs use the internal 2.5 V reference (DACxCON[1:0] = 10b or 01b, then the DAC output is unstable.
Workaround	The ADC and DACs can use the same external reference by setting REFCON = 0x01 and DACxCON[1:0] = 10b. The external reference should be capable of sourcing more than 10 µA.
Related Issues	None.

Table 13. P0.0/P0.1/P0.2/P0.3 Limitations When Used in GPIO or JTAG Modes [pr003]

Background	The ADuC7023 multiplexes the JTAG interface pins, nTRST, TDO, TDI, and TCK, with P0.0, P0.1, P0.2, and P0.3, respectively. During any reset sequence, the level on the P0.0 pin is sampled by the internal kernel program, which determines the mode of operation that the ADuC7023 part will enter after the reset sequence: If P0.0/nTRST/BM = 0 and Flash Address 0x80014 = 0xFFFFFFFF, the part enters I^{2}C download mode. P0.1, P0.2, and P0.3 default as input pins with a weak internal pull-up resistor enabled. If P0.0/nTRST/BM = 0 and Flash Address 0x80014 ≠ 0xFFFFFFFF, the part enters normal operating mode and P0.0, P0.1, P0.2, and P0.3 are normal GPIO or programmable logic array (PLA) pins. If P0.0/nTRST/BM = 1, the part enters JTAG programming/debug mode and P0.0, P0.1, P0.2, and P0.3 are JTAG pins.
Issue	User code should not write to the P0.1, P0.2, or P0.3 pins when the part is in JTAG programming/debug mode. If user code toggles any of these pins, JTAG debug pods will not be able to connect to the ADuC7023. If this happens, the user should ensure that Flash Address 0x80014 is erased to allow the reprogramming of the part through the I^{2}C interface. The user must be very careful when changing the mode of operation of the P0.0 to P0.3 pins. If these pins are incorrectly configured, then it may not be possible to reprogram the part again either via the JTAG interface or via the I^{2}C download interface if Flash Address 0x80014 is not erased.
Workaround	User code should implement a routine for erasing Flash Location 0x80014. It should be possible to call this routine in the end users application if it is deemed necessary to reprogram the flash area. When debugging the part via JTAG, Flash Location 0x80014 should be set to 0xFFFFFFFF. A simple definition at Vector Address 0x80014 in the project start-up file can implement this, that is: DCD 0xFFFFFFFF. This definition allows the part to be mass erased via the I^{2}C download interface if P0.1, P0.2, or P0.3 is accidentally written to by user code.
Related Issues	None.

SECTION 1. ADuC7023 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	ADC conversion—single software edge triggered mode.	Open
er002	ADC conversion—$CONV_{START}$ edge triggered mode.	Open
er003	ADC conversion —PLA edge triggered mode.	Open
er004	SPI bit rate issue.	Open
er005	Internal pull-up resistor on P2.0 cannot be disabled on 40-lead package.	Open
er006	Disabling I^2C interface in slave mode when a transfer is in progress.	Open
er007	Operation of SPI in slave mode.	Open
er008	Timer0 in periodic mode with an internal 32 kHz clock.	Open
er009	I^2C slave not releasing the bus	Open
er0010	I^2C clock stretch issue	Open

SECTION 2. ADuC7023 PERFORMANCE ISSUES

Reference Number	Description	Status
pr001	JTAG clock speed is limited.	Open
pr002	ADC and DAC reference selection limitation.	Open
pr003	P0.0/P0.1/P0.2/P0.3 limitations when used in GPIO or JTAG modes.	Open

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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