ERRATA SHEET
71M6543F

Revision B02 Errata

The errata listed below describe situations where 71M6543F revision B02 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata when the opportunity to redesign the product presents itself.

This errata sheet only applies to 71M6543F revision B02 components. Revision B02 components are branded on the topside of the package with a six-digit code in the form yywwB02, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another 71M6543F die revision, visit our website at www.maximintegrated.com/errata.

1) RTC_Q[1:0] VALUE OF 1 BEHAVES ERRONEOUSLY THE SAME AS A VALUE OF 3

Description:
The RTC_Q[1:0] (I/O RAM 0x289D[1:0]) is one of two locations used for digitally adjusting the real-time clock (RTC). The RTC_Q[1:0] field comprises 2 bits and can be set to 0, 1, 2, or 3. Due to a design error, an RTC_Q[1:0] value of 1 behaves erroneously the same as a value of 3.

Workaround:
The workaround for this issue is to never program RTC_Q[1:0] to a value of 1, as follows:
  a) When using the automatic RTC compensation (i.e., OSC_COMP = 1), and when loading the 128-byte NV RAM with RTC compensation values, entries that would have normally been RTC_Q[1:0] = 1 should be modified to have RTC_Q[1:0] = 0 or 2. In other words, instead of two decision points that would indicate when RTC_Q[1:0] should shift from 0 to 1 and from 1 to 2, there should be one decision point that causes RTC_Q[1:0] to shift between 0 and 2.
  b) When automatic compensation is not used (i.e., OSC_COMP = 0) and the MPU is calculating the RTC_P[16:0] and RTC_Q[1:0] correction, it should similarly replace the two decision points that would have bracketed RTC_Q[1:0] = 1 with a single decision point that causes a transition between 0 and 2.

Although this workaround causes a larger correction step, noise in the temperature sensor and variations in actual temperature should allow the average value of the compensation to remain unchanged.

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2) WATCHDOG RESET CAUSES INCORRECT FUSE READ UNDER SOME CONDITIONS

Description:
The 71M654x devices have a system of nonvolatile fuses that are trimmed during final test to store part-specific information. In operation these data are read from the fuses and stored in the device RAM. The fuse data in RAM are refreshed from the actual fuses whenever a watchdog timer reset instruction is executed and the CE is not enabled. Under some conditions, this fuse read operation can return incorrect data. Reading incorrect fuse data can cause a variety of problems, including:

a) Poor ADC accuracy due to internal reference voltage being off
b) Incorrect power management behavior

The improper fuse data read occurs when the CE has been disabled (CE_E = 0), but the CE is still executing code and a fuse read is performed due to a watchdog timer clear instruction.

Workaround:
The workaround is for software to avoid clearing the watchdog timer whenever the CE is disabled and is executing code (CE_BUSY = 1).

In the watchdog reset function, add an instruction to skip resetting the watchdog if CE is busy and CE_E = 0. The watchdog reset code for this test is as below:

```c
/* clear_wd() is typically called hundreds of times per second
 *   in the main loop. Since the watchdog time is 1.5 seconds and the time
 *   in which a bad read can occur is 0.0004 seconds, this works
 *   and introduces no unpredictable delay
 */
void clear_wd(void)
{
    if((CE6 & CE_E == 0) /* if the CE is not enabled */
    {
        if((INTBITS & 0x08) == 0)    /* if CE is not busy */
        {
            WDRST = 0x80; /* Clear the watchdog timer */
        }
    }
    else
    {
        WDRST = 0x80;    /* if CE is enabled, always clear watchdog */
    }
}
```

Because this function does not always reset the watchdog timer, the watchdog clear function must be called frequently enough to ensure that the watchdog does not expire.

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3) 71M654x DEVICES MAY NOT RESTART PROPERLY FOLLOWING A VOLTAGE DROP

Description:
Some 71M654x devices (71M6541D/F/G, 71M6542F/G, 71M6543F, 71M6543G, 71M6545/H) may not restart properly when the supply voltages fall into but not below a critical voltage range (approximately 600mV to 300mV).

The 71M654x devices maintain some configuration values in nonvolatile I/O RAM that is backed up by VBAT_RTC when the device is in brownout, LCD, or sleep mode. In addition, the state of some internal registers is also backed up by VBAT_RTC. The specified lower limit for VBAT_RTC to maintain these data is 2.0V, but the contents are typically preserved at much lower voltages. These I/O RAM locations are initialized when the device is reset. When the supply voltages drop to 0.0V and are then restored to operating levels, the on-chip POR circuitry generates a device reset which re-initializes the I/O RAM. The MPU is placed in reset when the internal supply voltage VDD drops below 2.0V, and is released from reset when system power is restored. If VBAT_RTC has dropped low enough for the state of nonvolatile bits in I/O RAM and internal registers to be lost, but voltage has not dropped low enough to trigger the internal POR, the MPU will re-start with incorrect contents in I/O RAM and internal registers, preventing proper operation of the device.

Workaround:
The workaround requires making sure that if VBAT_RTC drops below 2.0V while V3P3SYS is also less than 2.0V, a full device reset is performed when one of the voltages rises above 2.0V. Reset can be guaranteed by forcing all supply voltages to 0V before restoring supply voltages, or by asserting the RESET input after either VBAT_RTC or V3P3SYS supply voltages have been restored to above 2.0V. The RESET input can be provided by an external power supply supervisor or reset chip with a reset threshold that is greater than 2.0V. Usually, it will monitor just VBAT_RTC. The external reset circuit must meet the voltage levels, pulse duration, and transition times specified in the most recent data sheet for the metering device. Because the meter will typically require some housekeeping operations when system power is lost, such as saving accumulated measurement data, the reset threshold voltage should not be so high that it asserts device reset before the firmware power-down housekeeping functions are completed.

4) 71M654x DEVICES MAY NOT WAKE FROM SLEEP MODE WITHOUT AN EXTERNAL WAKE SIGNAL

Description:
Some 71M654x devices may not wake from SLP mode when power is restored unless an external WAKE event is asserted. This failure occurs because some gates in the 71M6x01 remote interface are powered by VDD rather than by VBAT_RTC. When the V3P3SYS is removed and the device enters SLP mode, the remote interface may be stuck in the power pulse mode. When system power is restored, V3P3SYS is connected to GND through the pulse transformer or a current shunt. Unless the power supply is capable of reaching 3.0V while supplying the additional current due to the low resistance connection to GND through the remote interface, asserting an external WAKE signal is required to exit SLP mode.

Workaround:
In designs that use the 71M6x01 remote inputs, or that use the inputs that can be configured to operate as remote inputs, connecting VDD to V3P3SYS with a 10kΩ resistor will prevent the remote drivers from sticking in the power pulse mode and connecting V3P3SYS to GND via the shunt or pulse transformer. If the inputs that support the 71M6x01 remote current sensors are unused, the remote mode should be disabled by setting the appropriate RCE0.RMT_E bits to 0, and the inputs should be connected to V3P3SYS with a pullup resistor of approximately 10kΩ.

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5) RTC_FAIL FLAG CAN BE SET INCORRECTLY

Description:
For the 71M654x devices, the RTC_FAIL flag can be set by events other than a failure of the VBAT_RTC voltage. In addition to the VBAT_RTC event, the RTC_FAIL flag can sometimes be set by a hardware reset and also when the WDT overflows (WD_OVF).

Workaround:
The suggested workaround qualifies RTC_FAIL with WF_CSTART, WF_RST, and WF_OVF using the following equation:

$$RTC\_FAIL\_QUAL = RTC\_FAIL \mathbin{\&} \mathord{\sim}(WF\_CSTART \mid WF\_RST \mid WF\_OVF)$$

This operation filters out erroneous setting of the RTC_FAIL flag that could be caused by hardware resets or WDT resets.

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/11	Initial release	—
1	3/13	Added erratum #2, #3, and #4	2, 3
2	9/13	Added erratum #5	4

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