



# DS26503 T1/E1/J1 BITS Element

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## REVISION A2 ERRATA

The errata listed below describe situations where DS26503 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26503 revision A2 components. Revision A2 components are branded on the top side of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS26503 die revision, visit our website at [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

### 1. TCLKO OUTPUT PIN IS NOT FUNCTIONAL IN 6312kHz CLOCK MODE

#### Description:

The Transmit Clock Output pin TCLKO is not functional in the Transmit 6312kHz clock mode (TMODE[3:0] = 1011). When in 6312kHz clock mode, this pin will be driven low and will not output the intended transmit clock frequency as selected by the TCSS1 and TCSS0 bits in the Transmit PLL Control Register (TPCR.1 and TPCR.0).

#### Work Around:

The intended functionality of TCLKO in 6312kHz mode can be achieved by configuring the part as shown when operating in software mode. This will allow the user to output the intended 6312kHz clock frequency on TCLKO.

- 1) Set the transmit mode to T1 D4 operating mode (set TMODE[3:0] = 0000).
- 2) Power down the line side transmitter pins (set TPD = 0 in LIC1)
- 3) Configure TSYNCIO as an input pin in order to keep the part from transmitting a sync pulse (set TSIO = 0 in IOCR1)
- 4) Select the PLL\_CLK as the transmit clock source (set TCSS1 = 0, TCSS0 = 1 in the Transmit PLL Control Register (TPCR)).
- 5) Select the PLL\_CLK frequency to be 6312kHz (set TPLLOFS[1:0] = 11 in TPCR).
- 6) Set the PLL\_CLK source (set TPLLSS in TPCR) correctly for the given application.

There is no direct work around if the part is used in Hardware Mode. The PLL\_OUT pin can be configured in Hardware Mode to output the 6312kHz clock frequency, however this should not be tied directly to TCLKO as TCLKO will still be driven by the part.

**2. TEST1 AND TEST0 BITS DO NOT FUNCTION AS STATED IN THE DATA SHEET****Description:**

The TEST1 and TEST0 bits (TSTRREG.5 and TSTRREG.4) do not function as indicated in the data sheet. These bits are intended to allow the user to force all output and I/O pins to a known state, either all high, all low, or tri-state. In some operating modes, the function of these bits is suppressed by the operating mode that the part is configured for, so that any output pins that are tri-stated based on the operating mode selected are still tri-stated regardless of the setting of the TEST1 and TEST0 bits. The affected operating modes and the associated pins are shown in the table below. The pins shown in the table will not be forced into the state indicated by the TEST1 and TEST0 bits and will instead remain tri-stated.

**Table 1. Pins That Do Not Function According to the Settings of TEST1 and TEST0**

<b>RMODE3</b>	<b>RMODE2</b>	<b>RMODE1</b>	<b>RMODE0</b>	<b>RECEIVE PATH OPERATING MODE</b>	<b>AFFECTED PINS</b>
0	0	0	0	T1 D4	—
0	0	0	1	T1 ESF	—
0	0	1	0	J1 D4	—
0	0	1	1	J1 ESF	—
0	1	0	0	E1 FAS	—
0	1	0	1	E1 CAS	—
0	1	1	0	E1 CRC4	—
0	1	1	1	E1 CAS and CRC4	—
1	0	0	0	E1 G.703 2048kHz Synchronization Interface	—
1	0	0	1	Reserved	—
1	0	1	0	Reserved	—
1	0	1	1	6312kHz Synchronization Interface	RS, RLOF, RSER, RAIS
1	1	0	0	Reserved	—
1	1	0	1	Reserved	—
1	1	1	0	Reserved	—
1	1	1	1	Reserved	—

**Work Around:**

None.

### 3. T1 AND E1 TRANSMIT WAVEFORMS MAY NOT BE CENTERED IN THEIR RESPECTIVE TEMPLATES AND MAY FAIL TEMPLATE COMPLIANCE IN CERTAIN LINE BUILD-OUTS

#### Description:

When the transmit path is configured in certain T1 or E1 line build-outs (LBOs), the transmit waveform may fail template compliance or the transmit waveform may not be centered in the corresponding template. To center the waveforms, several factory test registers should be set as shown below. The setting is also dependent on the use of the automatic gain controller (AGC) and the use of the impedance matching (IM) feature.

#### Work Around:

In order to center the transmit waveforms, set the factory test registers as shown. This work around is not available in hardware mode.

MODE	AGC	IM	ADDRESS	VALUE
T1 LBO1	On	On or Off	F1h	0Ah
T1 LBO2	On	On or Off	F1h	0Ah
T1 LBO3	On	On or Off	F1h	0Ah
T1 LBO4	On	On or Off	F1h	0Ah
E1 LBO0	On or Off	Off	F1h F2h	20h 08h
E1 LBO0	On or Off	On	F1h	20h
E1 LBO1	On	On or Off	F1h	20h
E1 LBO5	On	On or Off	F1h	20h