Engineer-to-Engineer Note EE-441

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ADSP-SC596/SC598 Board Design Guidelines for Dynamic Memory Controller

Contributed by Deepak Huchaiah, Nishant Singh

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Introduction

This EE note describes the recommended board design guidelines for interfacing Double Data Rate (DDR) memory and achieving expected performance from the controller. Use the following guidelines, in addition to standard board-level design practices.

Placement and General Routing Guidelines

Use these guidelines when designing PCB stack up, trace routing, and component placement:

- Place the ADSP-SC596/SC598 SHARC+® Processor and the memory as close as possible to each other, while minimizing routing length.
- The ADSP-SC596/SC598 SHARC+ Processor Dynamic Memory Controller (DMC) interface supports only point-to-point design and does not support fly-by topology.
- Plan the Printed Circuit Board (PCB) stack-up such that all the DMC signals (address, command, and control) have continuous reference planes (ground planes) on an immediately adjacent layer. Ensure that these signals do not travel across splits in the power or ground planes. Better to increase the distance between the signal and its relevant planes than to create the *cross-split* routing.

  For better signal integrity, avoid power-plane-to-signal-plane and power-plane-to-power-plane coupling. Strive to minimize this coupling.
- The PCB trace characteristic impedance must be 50 Ω for single-ended signals and 100 Ω for differential signals, with a 5% tolerance.
- Route all DDR signals as a group in every layer to avoid a mismatch in trace impedance and propagation delay. Keep all grouped signals on the same layer. For example, the signals named DMC_DQ00-07, DMC_LDQS, and DMC_LDQM, should be routed as a group, in the same layer and have the same ground reference.
  Caution: changing the ground reference plane can change the trace impedance.
- To avoid crosstalk, ensure all DDR signals have center-to-center spacing of at least 3 x trace width between DDR signals and 4 x trace width to other signals.
- Maintain perpendicularity between DMC signals routing, for different DMC signals routed in adjacent layers. This configuration reduces crosstalk, as signals on adjacent layers are not parallel to each other.
- Avoid test points on the DDR signals, as they create stubs which can act as EMI sources. Instead, use vias for probing. It is also acceptable to use JEDEC recommended methods that test vendors offer for diagnostics.

To simplify routing, byte lanes can be swapped. You must ensure that all DQ, DQS, and DM signals are substituted.
Example, DQ (7-0) ⇔ DQ (15-8),
DMC_LDQS ⇔ DMC_UDQS,
/DMC_LDQS ⇔ /DMC_UDQS,
DMC_UDM ⇔ DMC_LDM.

Within a byte lane, data bits can be swapped, except for the lowest order bit (for example, DQ0 should be connected to the DQ0 of the processor when lane swapping is not done). Swapping of address lines is not allowed.

Trace Length-Matching Criteria

The routing of all the DDR interface signals must be length-matched to avoid *Setup* and *Hold time* violations due to propagation delay.

Use the following length-matching criteria:

- Match the trace length of all address (DMC_A [nn], DMC_BA[n]) and command (DMC_CKE, DMC_CS[n], DMC_ODT, DMC_RAS, DMC_RESET, DMC_WE) signals within +/- 40 mils relative to the DMC_CK signal.
- Match the trace length of all data (DMC_DQ [nn]) and data mask (DMC_UDM, DMC_LDM) signals within +/- 40 mils relative to their corresponding DQS signal. For example, match the trace length of the lower order data byte (DMC_DQ00 - DMC_DQ07) and the corresponding data mask (DMC_LDM) signals with the lower order strobe (DMC_LDQS) signal.
- Match the trace length of differential signals such as clock (DMC_CK and /DMC_CK) and DQS pairs (DMC_LDQS and /DMC_LDQS, DMC_UDQS and /DMC_UDQS) within +/- 10 mils. For example, match the trace length of the DMC_CK and /DMC_CK signals within +/- 10 mils relative to each other.
- The maximum allowed trace length for DDR signals is 2 inches.

VTT Termination

Use the following guidelines for VTT termination. These guidelines can differ from vendor to vendor.

- For DDR3/3L, VTT termination is recommended by JEDEC, as this mitigates signal reflection. The primary purpose of a VTT island is to prevent reflections at the memory device. Removing the VTT termination results in signal reflections. The removal can lead to higher than nominal voltages at the memory address or command input pins, which can damage or reduce the lifetime of the memory. Check with the appropriate memory vendor for device-specific information.
- Implement VTT termination for the address and command lines as shown in *Figure 1* and taken from the publication *EV-SC598 SOM® Schematic, Rev D*, March 2022. Analog Devices, Inc.

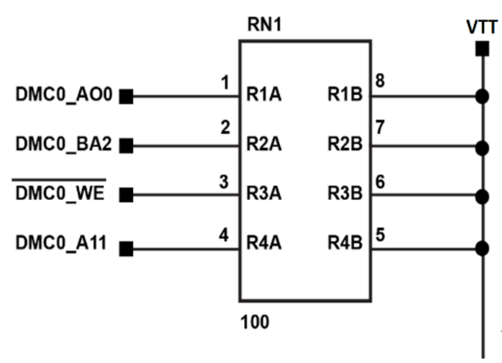

Figure 1. VTT Termination for Address and Command Line

The DMC_CK and /DMC_CK signals must be terminated using a differential termination scheme as in Figure 2. DMC Clock Differential Termination on page 3.

Figure 2. DMC Clock Differential Termination

- VTT termination does *not* play a major role for the ADSP-SC596/SC598 SHARC+ Processor, it is only a requirement for the memory device. Any alternative that prevents reflections on the address or command bus is an acceptable substitute for VTT termination at the processor.
- Separate VTT and VREF islands by a minimum of 150 mils if placed on the same PCB layer. Placing the islands on different layers is preferred.
- Place VTT islands as close as possible to the memory device.
- VTT islands require at least two additional decoupling capacitors (4.7 µF) and two bulk capacitors (100 µF). Place the capacitors at each end, as in Figure 3. VTT Supply and Decoupling Scheme on page 4.
- VTT island surface trace must have a minimum width of 150 mil. A width of 250 mil is preferred.
- Perform a decoupling analysis of the VTT planes.

DMC Power (VDD_DMC) Decoupling

Use the following guidelines for DMC power decoupling:

- The DMC interface should have enough decoupling on the VDD_DMC and the memory power rail to avoid data corruption.
- Refer to the DDR memory data sheet or consult its vendor to identify the decoupling capacitor requirement for the DDR memory power rails.
- The critical parameter `Idd7`, defines peak current during multi-bank operations and depends on the speed grade and ambient temperature of the DDR memory.
- Place all the decoupling capacitors very close to the VDD_DMC power rail and use solid power and ground planes.
- Ensure that the power and ground planes are adjacent to each other to provide the shortest return path and better power integrity.
- Isolate the DDR power planes from other supply planes. If this is not possible, separate them as much as possible and avoid overlapping them.
- Place individual power and ground vias from every power and ground pin of the ADSPSC596 / SC598 SHARC+® Processor and the memory device to its associated plane.
- Ensure that decoupling capacitors for the VDD_DMC power rail are placed as close as possible to the actual power pins. DDR signal slew rates are aggressive. Placing these capacitors close to the pin is *mandatory*. Provide dedicated power and ground vias for each decoupling capacitor pin, wherever possible.
- Ideally, the trace length from the power via to the processor pad should not exceed 30 mils. The maximum trace length from each power via to its decoupling capacitor is 60 mils. The maximum trace length from each power via to its power ball pad is 35 mils.
- Placement of the mid-bulk bypass capacitors (~10 µF) is *not* critical. They can be placed to accommodate other circuitry with more constrained placement and routing requirements.

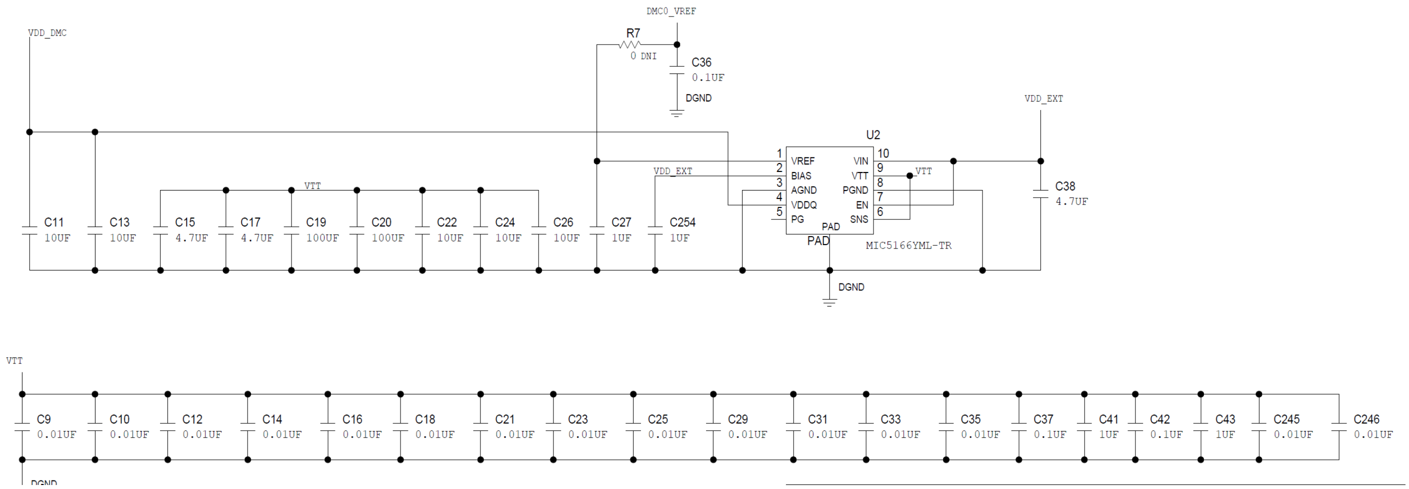

Figure 3. VTT Supply and Decoupling Scheme

DMC_VREF Voltage Supply

DMC_VREF acts as a voltage reference for DDR3/DDR3L data signals and compares the difference between a steady reference voltage (DMC_VREF) and the signal received for identifying the logic. Hence, it is recommended to minimize noise on DMC_VREF.

- Route the DMC_VREF trace at least 40 mil away from high-speed signals and noisy power supply traces.
- Guard traces can be provided around the DMC_VREF trace, if required. Ensure that the guard traces have sufficient ground vias stitched to the main ground.

PCB Placement and Routing Guidelines for the DMC_VREF Filter Network

Use the following guidelines for the plane:

- Provide adequate decoupling near the DMC_VREF pins of the ADSP-SC596/SC598 SHARC+ Processor, as well as at the memory device

  Keep the DMC_VREF trace as short as possible, with a width less than 20 mils.

Recommended DMC_VREF Filtering Scheme

Figure 4. DMC_VREF Filtering Network on page 5 shows the RCR filtering scheme on DMC_VREF that is recommended for ADSP-SC596/SC598 SHARC+ Processor. As shown, DMC_VREF0 and DMC_VREF1 can be shorted together. Use these guidelines for DMC_VREF filter network placement:

- Place the recommended RCR network between the DMC_VREF supply paths from the memory to the processor.
- Place the C (100 pF)-R (2 kΩ) portion of the RCR network as close as possible to the ADSP- SC596 / SC598 SHARC+ Processor DMC_VREF pin.
- Use a package (preferably 0402 size) for the 100 pF capacitor to guarantee a high self-resonant frequency.
- Route the entire RCR network on one layer with no vias in the traces.

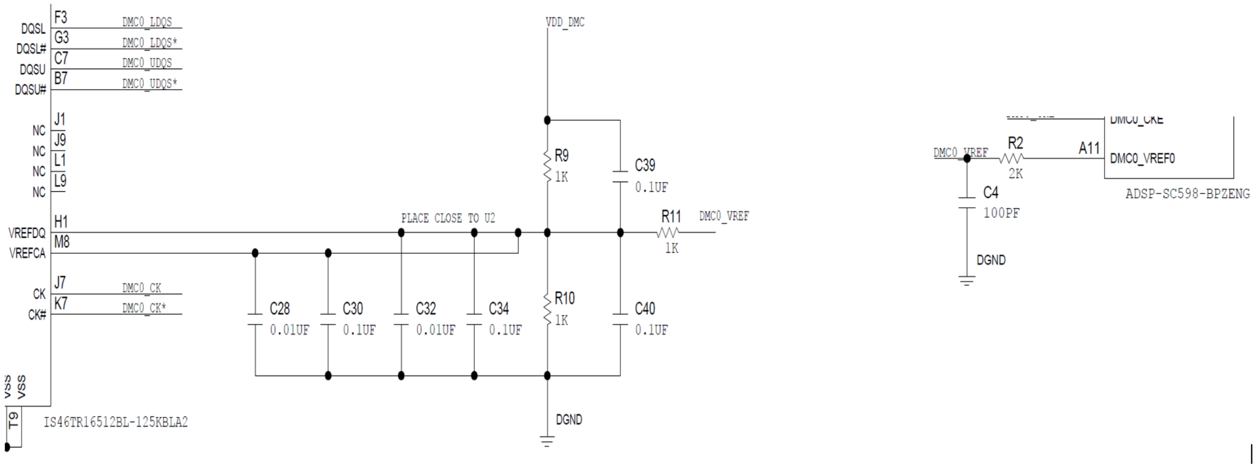

Figure 4. DMC_VREF Filtering Network

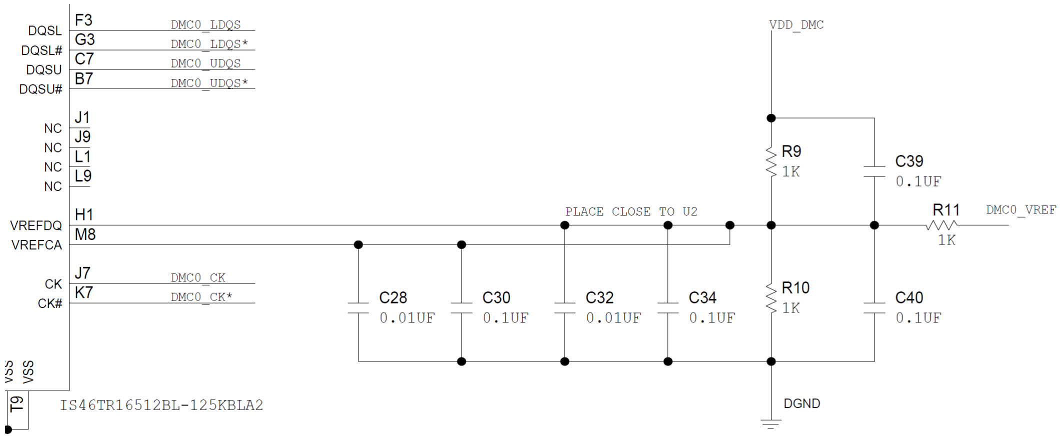

Figure 5. Recommended VREF Supply Circuit

Memory-Side Recommendations for VREF Supply

Use the following guidelines for DMC_VREF supply placement on the memory side. The requirements apply to both DDR3 and DDR3L.

- DDR3 memory has two VREF pins—VREFCA and VREFDQ. VREFCA serves as the reference for clock, address, command, and control signals. VREFDQ serves as the reference for strobe, data, and data mask signals.
- VREFCA and VREFDQ can have a common supply source but should be "STAR" routed and decoupled at the dedicated DRAM pins.
- Place two decoupling capacitors, 0.1 µF and 0.01 µF, for each VREF pin (VREFCA and VREFDQ).
- Place the 0.01 µF capacitor closer to the DRAM pin, followed by the 0.1 µF capacitor.

Keep the length from the decoupling capacitor to the DRAM supply pin as short as possible. Maintain the trace width based on the peak current requirement of the DDR. Figure 5. Recommended VREF Supply Circuit on page 5 shows the recommended VREF supply circuit for a DDR3 memory.

Routing Guidelines for other High-Speed Interfaces

Use the following recommendations for the high-speed peripherals (QSPI, Link Port, and SPORT) signal routing:

- The recommendation for maximum trace length is 4 inches.
- The trace length should be matched within +/- 3 mils, between the clock and all other signals. This ensures all signals are fulfilling the required timings.
- The clock signal should be routed 3 times the trace width, away from all other signals. This safeguards the clock signal from noise coupling.

VDD_DMC voltage, Drive Strength and ODT Recommendations

- The VDD_DMC nominal voltage shall be 1.39V for DDR3L (VDD_DMC minimum voltage is 1.34V and maximum voltage is 1.44V) and 1.5V for DDR3 (VDD_DMC minimum voltage is 1.425V and maximum voltage is 1.575V)
- Analog Devices recommends the Drive Strength for the ADSP-SC596/SC598 SHARC+ Processor operating at:
  - 900 MHz DDR clock is 70 ohms for DQ/DQS/DM/Clk, 100 ohms for ADDR/CMD, and the On-die Termination (ODT) [3] is 75 ohms.
  - 800 MHz DDR clock is 90 ohms for DQ/DQS/DM/Clk, 100 ohms for ADDR/CMD, and the ODT is 75 ohms.
  - For 667 MHz or 500 MHz operation recommended Drive Strength is 100 ohms for DQ/DQS/DM/Clk, 100 ohms for ADDR/CMD, and ODT is 75 ohms.
- Analog Devices recommends 40 ohms Drive Strength for DDR memory operating at 500 MHz, 667 MHz, 800 MHz, and 900 MHz. The ODT is 120 ohms for 500 MHz, 667 MHz, and 800 MHz DDR memory. ODT is 60 ohms for 900 MHz DDR memory.

DDR3/3L compliance testing as per JESD79-3F

The ADSP-SC596/SC598 SHARC+ processor was tested against JESD79-3F using the Tektronix DDR Analysis compliance test suite, when the board design guidelines, Drive Strength, and ODT settings are followed.

- The following compliance testing setup (Figure 6. DDR3L Compliance Testing Setup) on page 7 is used with the test suite (Figure 7. Snapshot of DDR3L Compliance Test Suite on page 7):
  - Oscilloscope - DPO77002SX, 13-70 GHz, ATI, 200 GS/s
  - Temperature forcing equipment – Thermostream ATS-545

Figure 6. DDR3L Compliance Testing Setup

- DDR Analysis Version 10.0.8.179

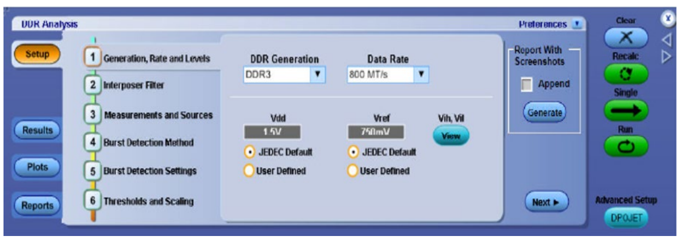

Figure 7. Snapshot of DDR3L Compliance Test Suite

- Trimode Probes – P7513A (13 GHz)
- Probe tips – P75TLRST

- When the board design guidelines or recommended Drive Strength and ODT settings are not followed, then the DDR3/3L compliance must be done on board to guarantee proper operation.
- The compliance must be done across Voltage (VDD_INT, VDD_DMC), Process, and Temperature. Of all the Process, Voltage and Temperature cases, the following cases can be prioritized:
  - SS Process corner, minimum Voltage, and minimum Temperature
  - TT Process corner, typical Voltage, and typical Temperature
  - FF Process corner, maximum Voltage, and maximum Temperature

List of compliance parameters tested:

Clock Differential

- Eye-Diagram (Figure 8)

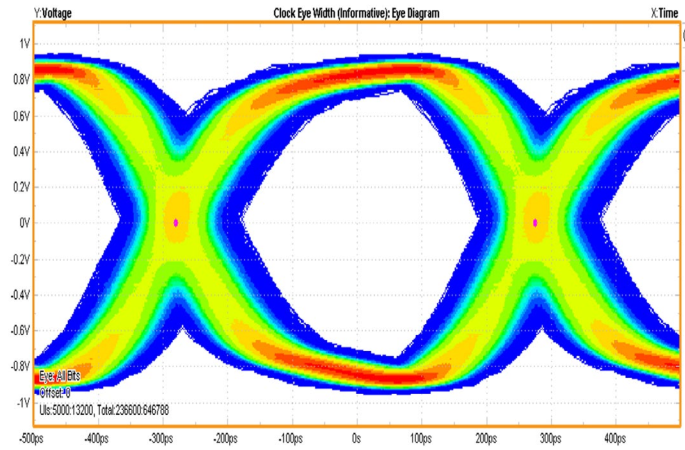

Figure 8. Snapshot Clock Differential Eye Diagram

- tCH(abs)
- tCH(avg)
- tCK(abs)
- tCK(avg)
- tCL(abs)
- tCL(avg)
- tDVAC(CK)
- tJIT(cc)
- tJIT(duty)
- tJIT(per)
- VIHdiff(AC)
- VILdiff(AC)
- InputSlew-Diff-Fall(CK)
- InputSlew-Diff-Rise(CK)
- tERR(02per)
- tERR(03per)
- tERR(04per)
- tERR(05per)
- tERR(11-50per)
- tERR(6-10per)

Clock Single ended

- AC-Overshoot(CK#)
- AC-Overshoot(CK)
- AC-OvershootArea(CK#)
- AC-OvershootArea(CK)
- AC-Undershoot(CK#)
- AC-Undershoot(CK)
- AC-UndershootArea(CK#)
- AC-UndershootArea(CK)
- Vix(ac)
- VSEH(CK#)
- VSEH(CK)
- VSEL(CK#)
- VSEL(CK)

Write Burst

- DQ/DQS Eye Diagram (Figure 9)

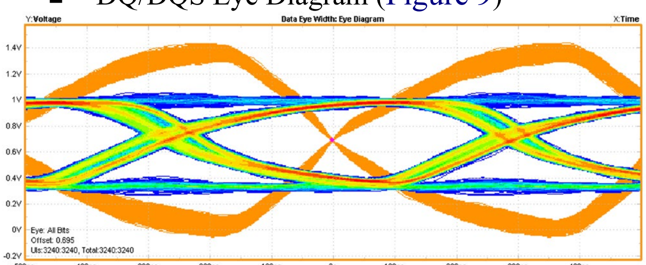

Figure 9. Snapshot Write Burst Eye Diagram

- tDIPW-High, DQ
- tDIPW-LOW, DQ
- Slew Rate-Hold-Fall(DQ)
- Slew Rate-Hold-Rise(DQ)
- Slew Rate-Setup-Fall(DQ)
- Slew Rate-Setup-Rise(DQ)
- VIHdiff(AC), DQS
- VILdiff(AC), DQS
- tDQSH, DQS
- tDQSL, DQS
- tDQSS-Diff, CK, DQS
- tDSH-Diff, CK, DQS
- tDSS-Diff, CK, DQS
- tDVAC(DQS)
- tWPRE DQS
- tWPST DQS
- tDH-Diff(base) DQ, DQS
- tDH-Diff(derated) DQ, DQS
- tDS-Diff(base) DQ, DQS
- tDS-Diff(derated) DQ, DQS
- InputSlew-Diff-Fall(DQS)
- InputSlew-Diff-Rise(DQS)
- tVAC(DQ)

Write Single ended

- Vix(ac) DQS
- VSEH(DQS#)
- VSEH(DQS)
- VSEL(DQS#)
- VSEL(DQS)

Address/Command

- Eye Diagram (Figure 10)

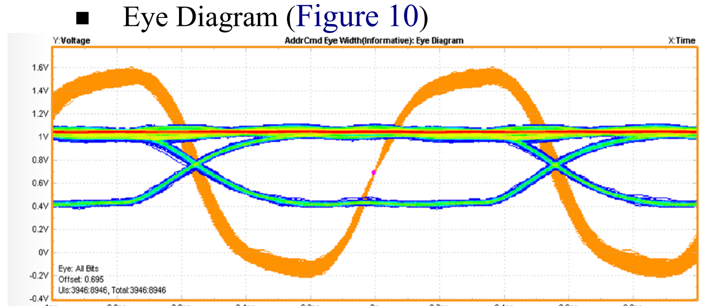

Figure 10. Snapshot Address/Command Eye Diagram

- AC-Overshoot, ADDR/CMD
- AC-OvershootArea, ADDR/CMD, CK
- AC-Undershoot, ADDR/CMD

- AC-UndershootArea, ADDR/CMD, CK
- tIPW-High, ADDR/CMD
- tIPW-Low, ADDR/CMD
- tIH(base), CK, ADDR/CMD
- tIH(derated), CK, ADDR/CMD
- tIS(base), CK, ADDR/CMD
- tIS(derated), CK, ADDR/CMD
- Slew Rate-Hold-Fall(Addr/Cmd)
- Slew Rate-Hold-Rise(Addr/Cmd)
- Slew Rate-Setup-Fall(Addr/Cmd)
- Slew Rate-Setup-Rise(Addr/Cmd)

References

[1] *ADSP-2156x Board Design Guidelines for Dynamic Memory Controller (EE-418). Rev 2, September 2020. Analog Devices, Inc.*

[2] *EV-SC598 SOM® Schematic, Rev D, March 2022. Analog Devices, Inc.*

[3] *On-die termination (ODT) is the technology where the termination resistor for impedance matching in transmission lines is located inside a semiconductor chip instead of on a printed circuit board (PCB).*

Document History

Revision	**Description**
Rev 1 – June 28, 2022 *by Deepak Huchaiah, Nishant Singh*	Initial Release (Edited on 9/20, 9/27, and 9/28/2022) (Final Version Created 10/04/2022)
Rev 2 – July 10, 2023	Remove references to ADSP-SC595