Estimating Power for ADSP-BF538/BF539 Blackfin® Processors

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Introduction

This EE-Note discusses the methodology for estimating total average power consumption of ADSP-BF538 and ADSP-BF539 Blackfin® embedded processors. It also applies to the processor models equipped with on-chip flash memory. The term *Blackfin* refers to all variations of processors addressed by this document.

Power estimates are based on characterization data measured over power supply voltage, core frequency (CCLK), and junction temperature (T_J). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using Blackfin processors. These processors feature dynamic power management control, allowing the regulation of applied core voltage (V_{DDINT}) from an external I/O source (V_{DDEXT}). The ranges for these supplies differ depending on the part being used.

The total power consumption of the Blackfin processor is the sum of the power consumed for both of the power supply domains, V_{DDINT} and V_{DDEXT}.

Please consult the following sections of the appropriate data-sheet[1][2] for details specific to discussions throughout this EE-Note:

- See the *Recommended Operating Conditions* section for details regarding V_{DDINT} and V_{DDEXT} ranges.
- See the *Timing Specifications* section for details regarding required V_{DDINT} values to support the desired CCLK.
- See the *Ordering Guide* section for a comprehensive list of the various speed and temperature grade models available for ADSP-BF538 and ADSP-BF539 Blackfin processors.

Estimating Internal Power Consumption

The total power consumption due to internal circuitry (on the V_{DDINT} supply) is the sum of the static power component and dynamic power component of the processor's core logic. The dynamic portion of the internal power depends on the instruction execution sequence, the data operands involved, and the instruction rate. The static portion of the internal power is a function of temperature and voltage; it is not related to processor activity.

Analog Devices provides current consumption figures and scaling factors for discrete dynamic activity levels. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for Blackfin processors in a given application.

Internal Power Vector Definitions

The following power vector definitions define the dynamic activity levels that apply to the internal power vectors shown in Table 1. These test vectors apply to all Blackfin processors.

- $I_{DD-IDLE}$ - V_{DDINT} supply current for idle activity. Idle activity is the core executing the `IDLE` instruction only, with no core memory accesses, no DMA, and no interrupts.
- I_{DD-NOP} - V_{DDINT} supply current for no-op activity. No-op activity is the core executing the `NOP` instruction only, with no core memory accesses, no DMA, and no interrupts. This is a useful measurement for software-implemented delay loops.
- I_{DD-APP} - V_{DDINT} supply current for a specific application's activity. This activity is the core executing an application comprised of 30% dual-MAC instructions and 70% load-store and no-op instructions. All instructions and data are located in L1 SRAM, and peripherals are not enabled.
- I_{DD-TYP} - V_{DDINT} supply current for typical activity. Typical activity is the core executing an application comprised of 75% dual-MAC instructions and 25% dual-ALU instructions. All instructions and data are located in L1 SRAM, and peripherals are not enabled. This is the test vector used for the dissipation numbers found in the data-sheet.
- $I_{DD-HIGH}$ - V_{DDINT} supply current for high activity. High activity is the core executing an application comprised entirely of dual-MAC instructions. All instructions and data are located in L1 SRAM, and peripherals are disabled.
- $I_{DD-PEAK}$ - V_{DDINT} supply current for peak activity for ADSP-BF538 processors. Peak activity is the core executing 100% dual-MAC instructions fetched from internal memory, with memory DMA moving a data pattern from L1 Data A memory to L1 Data B memory. The bit pattern toggles all bits in each access. This vector is also utilized for the ADSP-BF539 processor, however, it is not representative of a peak value as it does not utilize the dedicated MXVR DMA engine or the dedicated internal power rail for the MXVR.

The test code used to measure $I_{DD-PEAK}$ represents worst-case processor operation for ADSP-BF538 processors. This activity level is not realistic under normal application conditions.

For ADSP-BF539 processors, the MXVR peripheral contributes to the dynamic power profile when its DMA channels are powered and running in the background while these test vectors are run on the core. To represent this, the same test vectors as described above are suffixed with a trailing `–MXVR` in Table 1 to show the same test vector with the MXVR powered and running. The vectors are $I_{DD-IDLE-MXVR}$, $I_{DD-NOP-MXVR}$, $I_{DD-APP-MXVR}$, $I_{DD-TYP-MXVR}$, $I_{DD-HIGH-MXVR}$, and $I_{DD-PEAK-MXVR}$.

The test code used to measure $I_{DD-PEAK-MXVR}$ represents worst-case processor operation for ADSP-BF539 processors. This activity level is not realistic under normal application conditions.

Estimating I_{DDINT} Dynamic Current, I_{DD-DYN}

There are two steps required to estimate dynamic power consumption due to internal circuitry (i.e., on the V_{DDINT} supply). The first step is to determine the dynamic baseline current, and the second step is to determine the percentage of activity for each discrete power vector with respect to the entire application.

I_{DD} Baseline Dynamic Current, $I_{DD-BASELINE-DYN}$

The Blackfin processors' baseline dynamic current ($I_{DD-BASELINE-DYN}$) graph is shown in Figure 1. The value of $I_{DD-BASELINE-DYN}$ is derived using the I_{DD-TYP} dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DDINT} dynamic current for a specified power supply setting. Using the curve specific to the application, $I_{DD-BASELINE-DYN}$ for the V_{DDINT} power supply domain can be estimated at the CCLK of the processor in the application. For example, with V_{DDINT} at 1.2 V and CCLK at 400 MHz, the corresponding $I_{DD-BASELINE-DYN}$ for the V_{DDINT} power supply domain would be approximately 140 mA.

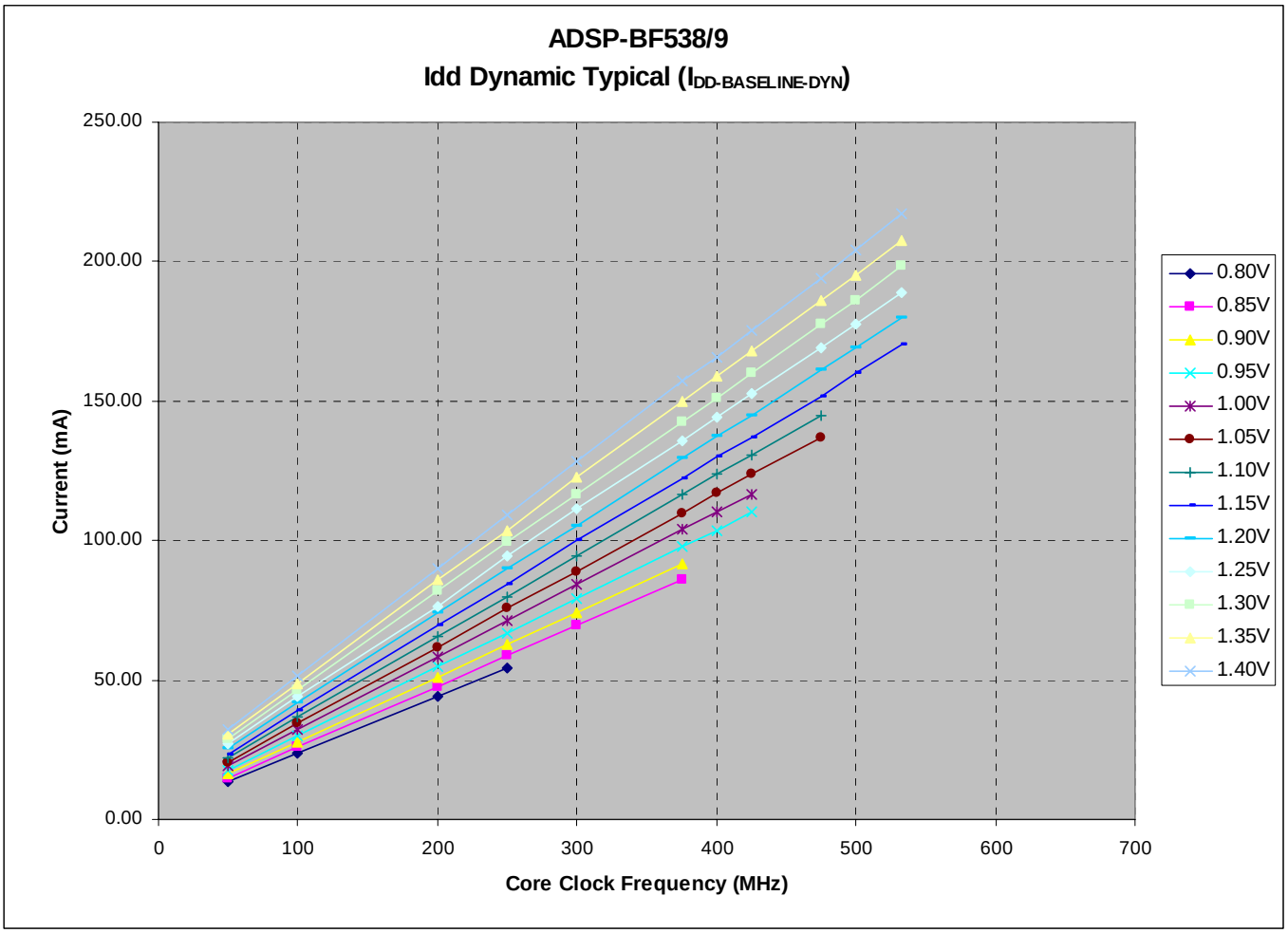

Figure 1. Baseline I_{DDINT} Dynamic Current

I_{DD} Dynamic Current Running Your Application

Table 1 lists the scaling factors for each activity level, which are used to estimate the dynamic current for each specific application. With knowledge of the program flow and an estimate of the percentage of time

spent at each activity level, system developers can use the $I_{DD-BASELINE-DYN}$ shown in Figure 1 and the corresponding activity scaling factors (ASF) from Table 1 to determine the dynamic portion of the internal current (I_{DD-DYN}) for each Blackfin processor in a system.

Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK-MXVR}$*	1.36
$I_{DD-HIGH-MXVR}$*	1.32
$I_{DD-PEAK}$	1.30
$I_{DD-HIGH}$	1.28
$I_{DD-TYP-MXVR}$*	1.07
I_{DD-TYP}	1.00
$I_{DD-APP-MXVR}$*	0.92
I_{DD-APP}	0.88
$I_{DD-NOP-MXVR}$*	0.76
I_{DD-NOP}	0.74
$I_{DD-IDLE-MXVR}$*	0.50
$I_{DD-IDLE}$	0.48

** Applies only to ADSP-BF539/ADSP-BF539F processors*

Table 1. Internal Power Vectors and Dynamic Scaling Factors

I_{DD-DYN} for a Blackfin processor in a specific application is calculated according to Equation 1a or Equation 1b, where "%" is the percentage of the overall time that the application spends in that state:

$$\begin{aligned}
&(\%\ \textit{Peak activity level} \times I_{DD-PEAK}\ \textit{ASF} \times I_{DD-BASELINE-DYN}) \\
&(\%\ \textit{High activity level} \times I_{DD-HIGH}\ \textit{ASF} \times I_{DD-BASELINE-DYN}) \\
&(\%\ \textit{Typ. activity level} \times I_{DD-TYP}\ \textit{ASF} \times I_{DD-BASELINE-DYN}) \\
&(\%\ \textit{App. activity level} \times I_{DD-APP}\ \textit{ASF} \times I_{DD-BASELINE-DYN}) \\
&(\%\ \textit{NOP activity level} \times I_{DD-NOP}\ \textit{ASF} \times I_{DD-BASELINE-DYN}) \\
+\ &(\%\ \textit{Idle activity level} \times I_{DD-IDLE}\ \textit{ASF} \times I_{DD-BASELINE-DYN}) \\
&\overline{\textit{Total Dynamic Current for } V_{DDINT}\ (I_{DD-DYN})}
\end{aligned}$$

Equation 1a. Internal Dynamic Current (I_{DD-DYN}) for ADSP-BF538 Processors

$$
\begin{aligned}
&(\%\ \textit{Peak activity level w/MXVR} \times I_{DD\text{-}PEAK\text{-}MXVR}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{High activity level w/MXVR} \times I_{DD\text{-}HIGH\text{-}MXVR}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{Typ. activity level w/MXVR} \times I_{DD\text{-}TYP\text{-}MXVR}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{App. activity level w/MXVR} \times I_{DD\text{-}APP\text{-}MXVR}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{NOP activity level w/MXVR} \times I_{DD\text{-}NOP\text{-}MXVR}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{Idle activity level w/MXVR} \times I_{DD\text{-}IDLE\text{-}MXVR}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{Peak activity level} \times I_{DD\text{-}PEAK}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{High activity level} \times I_{DD\text{-}HIGH}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{Typ. activity level} \times I_{DD\text{-}TYP}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{App. activity level} \times I_{DD\text{-}APP}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
&(\%\ \textit{NOP activity level} \times I_{DD\text{-}NOP}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})\\
+\ &(\%\ \textit{Idle activity level} \times I_{DD\text{-}IDLE}\ ASF \times I_{DD\text{-}BASELINE\text{-}DYN})
\end{aligned}
$$

$$
\textit{Total Dynamic Current for } V_{DDINT}\ (I_{DD\text{-}DYN})
$$

Equation 1b. Internal Dynamic Current ($I_{DD\text{-}DYN}$) for ADSP-BF539 Processors

For example, after profiling the application code for a particular ADSP-BF538 processor system, activity is determined to be proportioned as shown in Figure 2.

$$
\begin{aligned}
&\textit{(10\% Peak Activity Level)}\\
&\textit{(20\% High Activity Level)}\\
&\textit{(50\% Typ. Activity Level)}\\
&\textit{(10\% App. Activity Level)}\\
&\textit{(10\% NOP Activity Level)}\\
+\ &\textit{(0\% Idle Activity Level)}
\end{aligned}
$$

$$
\textit{100\% Activity}
$$

Figure 2. Internal System Activity Levels for an ADSP-BF538 Blackfin Processor System

Using the ASF provided for each activity level in Table 1 (and with V_{DDINT} at 1.2 V and CCLK at 400 MHz), a value for $I_{DD\text{-}DYN}$ consumption of a single processor can be estimated as follows:

$$
\begin{aligned}
&\textit{(10\% x } \mathbf{1.30} \textit{ x 140)}\\
&\textit{(20\% x } \mathbf{1.28} \textit{ x 140)}\\
&\textit{(50\% x } \mathbf{1.00} \textit{ x 140)}\\
&\textit{(10\% x } \mathbf{0.88} \textit{ x 140)}\\
&\textit{(10\% x } \mathbf{0.74} \textit{ x 140)}\\
+\ &\textit{(0\% x } \mathbf{0.41} \textit{ x 140)}
\end{aligned}
$$

$$
I_{DD\text{-}DYN} = 146.72\ mA = \sim 147\ mA
$$

Figure 3. Internal Dynamic Current Estimation for ADSP-BF538 Blackfin Processor System

The total estimated dynamic current on the V_{DDINT} power supply in this ADSP-BF538 Blackfin processor example is ~147 mA.

For ADSP-BF539 systems, the profiling of the application code must consider when the MXVR peripheral is running. Percentages spent in each possible application state would still add up to 100% activity, as defined in Figure 2 above, but there are six additional defined states for ADSP-BF539

applications. Similarly, these additional six states would be added to Figure 3 as well when computing the total internal dynamic current estimation.

Estimating I_{DDINT} Static Current, $I_{DD\text{-}DEEPSLEEP}$

Deep Sleep mode for Blackfin processors is when power is applied to the core and L1 memories, but all clocks are turned off. In this mode, the $I_{DD\text{-}DEEPSLEEP}$ measurement can be taken, which is the baseline static component of overall average dissipation. The $I_{DD\text{-}DEEPSLEEP}$ current graph for the Blackfin processors is shown in Figure 4. The static current on the V_{DDINT} power supply domain is a function of junction temperature (T_J) and voltage, but it is ***not*** a function of frequency or activity level.

Therefore, unlike the dynamic portion of the internal current, the static current need not be calculated for each discrete activity level or power vector. Using the static current curve corresponding to the application (i.e., at specific V_{DDINT}), $I_{DD\text{-}DEEPSLEEP}$ can be estimated vs. T_J of the Blackfin processor.

Appendix A discusses the methodology for estimating T_J. This process involves knowing the total power profile for the processor; therefore, this process will be iterative to arrive at a final calculation for expected power dissipation.

For example, in an application with V_{DDINT} at 1.2 V and a Blackfin processor at a T_J of +100°C, the corresponding $I_{DD\text{-}DEEPSLEEP}$ for the V_{DDINT} power domain would be approximately 360 mA.

The static power of the Blackfin processor is constant for a given voltage and temperature. Therefore, it is simply added to the total estimated dynamic current when calculating the total power consumption due to the internal circuitry of the Blackfin processor. Note that the $I_{DD\text{-}DEEPSLEEP}$ currents shown in Figure 4 represent the worse-case static current as measured across the wafer fabrication process.

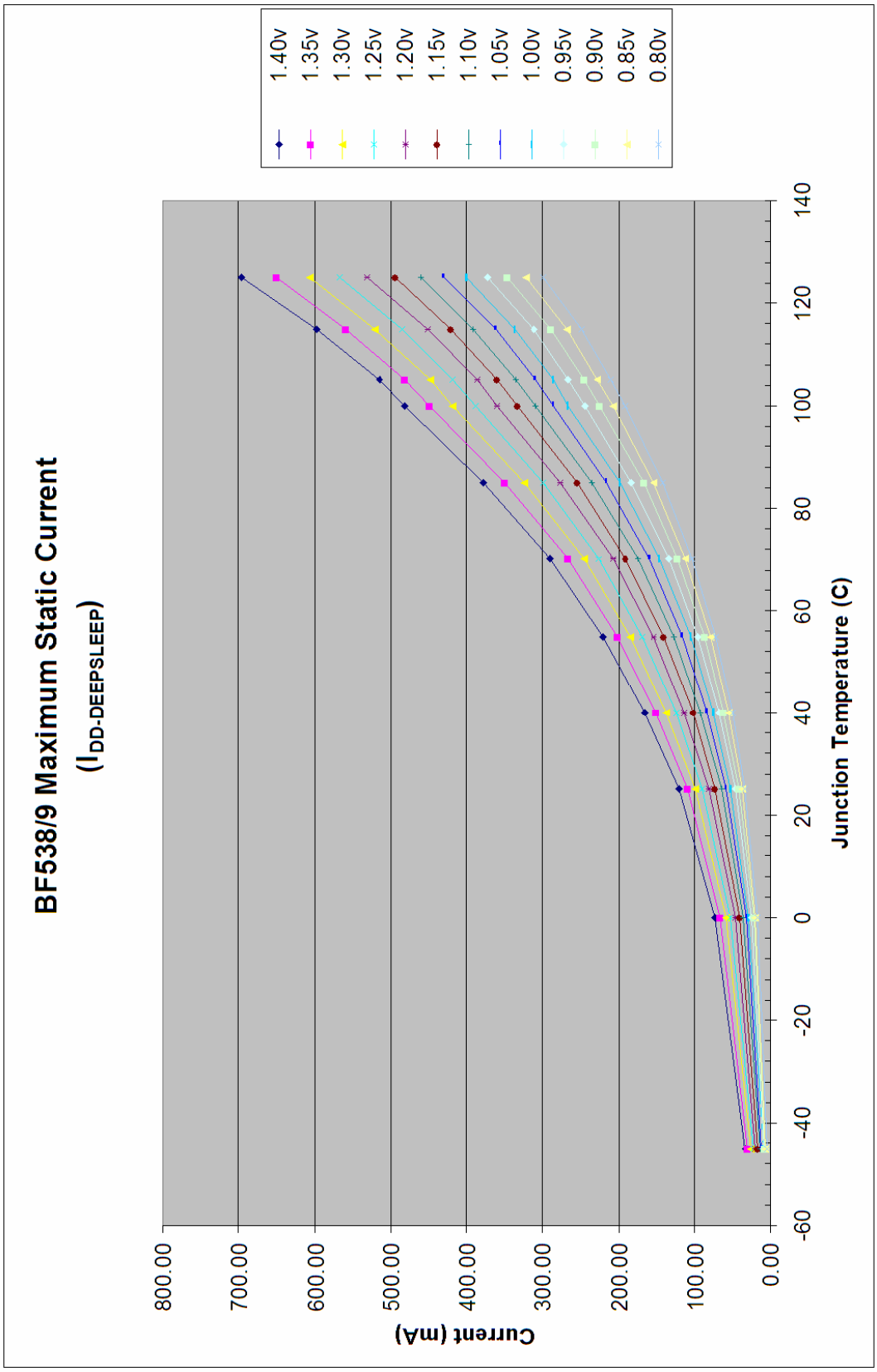

Figure 4. $I_{DD\_DEEPSLEEP}$ Static Current

Estimating Total I_{DDINT} Current

The total current consumption due to the internal core circuitry (I_{DDINT}) is the sum of the dynamic current component and the static current component, as shown in Equation 2.

$$I_{DDINT} = I_{DD\text{-}DYN} + I_{DD\text{-}DEEPSLEEP}$$

Equation 2. Internal Core Current (I_{DDINT}) Calculation

Continuing with the example of the Blackfin processor operating at 1.2 V and 400 MHz (and with the code as profiled), assume that the resulting T_J is estimated to be +100°C. The total internal current consumed by the processor core under these conditions would be:

$$I_{DDINT} = 140 + 360 = 500\ mA$$

Equation 3. I_{DDINT} Estimation

Total Estimated Internal Power, P_{DDINT}

The resulting internal power consumption (P_{DDINT}) is given by Equation 4.

$$P_{DDINT} = V_{DDINT}\ x\ I_{DDINT}$$

Equation 4. Internal Power (P_{DDINT}) Calculation

Using Equation 4, the total estimated internal power consumed by the processor in the application described in this example would be:

$$P_{DDINT} = 1.20V\ x\ 500\ mA = 600\ mW$$

Equation 5. P_{DDINT} Estimation (High-Performance)

Estimating External Power Consumption

External power consumption (on the V_{DDEXT} supply) is dependent on the enabled peripherals in a given system. Each unique group of peripheral pins contributes to a piece of the overall external power, based upon several parameters:

- *O* - The number of output pins that switch during each cycle
- *f* - The maximum frequency at which the output pins can switch
- V_{DDEXT} - The voltage swing of the output pins
- C_L - The load capacitance of the output pins
- *U* - The utilization factor (the percentage of time that the peripheral is on and running)

In addition to the input capacitance of each device connected to an output, the total capacitance (C_L) should include the capacitance of the processor pin itself (C_{OUT}), which is driving the load.

Equation 6 shows how to calculate the average external current (I_{DDEXT}) using the above parameters:

$$I_{DDEXT} = O \ x \ f/2 \ x \ V_{DDEXT} \ x \ C_L \ x \ U$$

Equation 6. External Current (I_{DDEXT}) Calculation

The worst-case external pin power scenario occurs when the load capacitor charges and discharges continuously, requiring the pin to toggle each cycle. Since the state of the pin can change only once per cycle, the maximum toggling frequency is `f/2`. In terms of supply power, the worst-case V_{DDEXT} value is 3.6 V. Table 2 contains data for a realistic example of a PPI application, which runs several peripherals simultaneously. Actual results may vary, but again, the intent of this document is to help designers size the power supplies.

Estimated average external power consumption (P_{DDEXT}) can be calculated as follows.

$$P_{DDEXT} = V_{DDEXT} \ x \ I_{DDEXT}$$

Equation 7. External Power (P_{DDEXT}) Calculation

Using the sample Blackfin system configuration in Figure 5, the external current and, therefore, the external power consumption can be estimated.

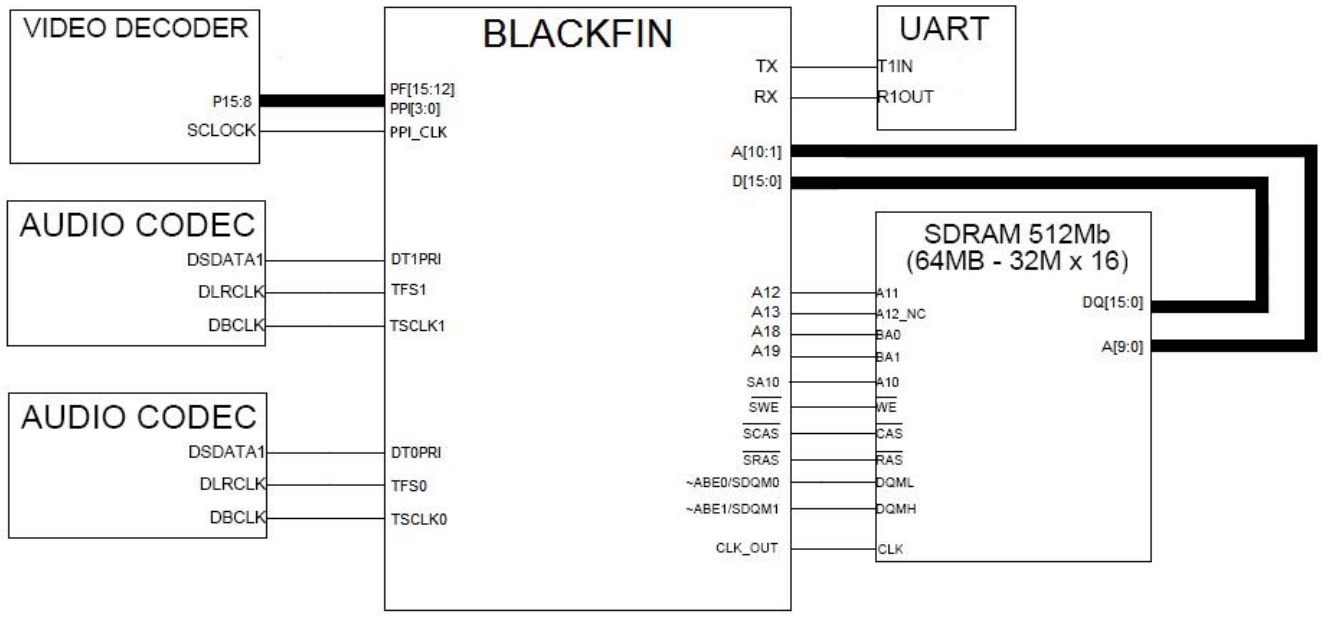

Figure 5. Blackfin System Sample Configuration

I_{DDEXT} (Equation 6) can be calculated for each class of pins that can drive, as shown in Table 2.

Peripheral	Freq (Hz)	# of pins	C/pin (F)	Toggle Ratio	Util	Vddext (V)	Pout @ 3.6V (mW)
PPI	27.00E+06	9	30.00E-12	1	1.00	3.6	47.24
SPORT0	4.00E+06	2	30.00E-12	1	1.00	3.6	1.56
SPORT1	4.00E+06	2	30.00E-12	1	1.00	3.6	1.56
UART	115.00E+03	2	30.00E-12	1	0.25	3.6	0.01
SDRAM	133.33E+06	36	30.00E-12	0.25	0.50	3.6	116.35
Total External Power Dissipation @ 3.6 V (est. mW)							166.71

Table 2. Sample Calculation For Total Average External Power

In the above example, the total average external power consumption is estimated to be ~165 mW. This number was obtained with the parameters listed in Table 2 by applying Equation 8. The chosen operating frequencies are reasonable for each of the peripherals, including the maximum allowed SDRAM frequency of 133.33 MHz. This model assumes that each output pin changes state every clock cycle, which is a worst-case model, except in the case of the SDRAM (because the number of output pins transitioning each clock cycle will be less than the maximum number of output pins). Table 2 was taken from the *External Power Spreadsheet*[3], which is associated with this EE-Note. It contains calculations for four sample systems. The reader can tailor this spreadsheet to the application, adding or deleting rows as necessary. Since the equation provides results in Watts (W), an additional multiplier of 1000 in the spreadsheet converts results into mW.

This equation is a more theoretically accurate version of the one used in the spreadsheet:

$$\overline{P}_{ext} = V_{DDext}{}^2 \cdot \sum_{All-Output-Pins} C_L \cdot \overline{f}$$

Equation 8. Alternate External Power (P_{DDEXT}) Calculation

Rather than estimating average external power dissipated in each *peripheral*, the estimate applies to each *individual output pin*, based on the pin's load capacitance and average toggling frequency. The voltage swing is uniform across all output pins within the V_{DDEXT} supply domain, so it is multiplied by the summation of the dynamic charge changes on each output.

Using the PPI data in Table 2, nine output pins change every cycle at an average frequency of 27 MHz. Since toggling between on-to-off and off-to-on requires two cycles, F_{AVG} (13.5 MHz) is half the PPI clock. Since each pin changes at the same rate and the pin capacitance is presumed to be the same, the summation is simply nine times the value of any one PPI pin. Applying Equation 8:

$$\begin{aligned} P_{EXT\_AVG} &= V_{DDEXT}{}^2 * 9 \text{ pins} * (F_{AVG} * C_L) \\ &= (3.6)^2 * 9 * 13.5e6 * 30e\text{-}12 \\ &= 12.96 * 0.003645 \\ &= 0.0472392W \\ &= 47.239mW \end{aligned}$$

As can be seen, the value derived using this equation is the same as the value estimated in Table 2. This model obtains the same estimate on a per-pin basis rather than a per-peripheral basis.

In addition to the peripheral pins, there are two other output pins on Blackfin processors that will contribute to the V_{DDEXT} supply domain power profile if the system uses a crystal to provide the CLKIN signal to the processor. In this case, the ADSP-BF538/BF539 processors drive the XTAL output pin when the PLL is active. The output drive frequency will be exactly the CLKIN rate, and the pin capacitance value can be obtained from the data-sheet. Note that the voltage swing will likely be less than V_{DDEXT} for most crystals, and using V_{DDEXT} in computations would be a worst-case model in terms of profiling power dissipation. Similarly, the same concepts apply for the MXI and MXO pins on the ADSP-BF539 Blackfin processor for the MXVR oscillator.

For those processor models equipped with one, the on-chip flash memory will contribute to the V_{DDEXT} supply domain power profile as well. Please see the appropriate Spansion Known Good Die data-sheet supplement[4][5] for details regarding power dissipation of the memory die.

Finally, designers must be mindful of power supply efficiency when sizing the V_{DDEXT} supply. *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)*[6] describes the internal voltage regulator.

Real-Time Clock (RTC) Power Consumption

The final source of total power consumption comes from the optional third power domain, the Real-Time Clock (RTC) power domain (V_{DDRTC}), which is a specified value. The RTC can be powered between 2.25 V and 3.6 V. For a worst-case analysis, a supply voltage of 3.6 V yields a current draw, I_{DDRTC}, of 30 µA to 50 µA for a range of ambient temperature from 25 °C to 85 °C. For the sake of including this number in the final power consumption estimate, the power dissipated in the RTC domain, P_{DDRTC} is:

$$P_{DDRTC} = V_{DDRTC} \; x \; I_{DDRTC}$$

Equation 9. Total Power (P_{DDRTC}) Calculation

Knowing this value helps in selecting a battery as a potential power source for the RTC. The RTC can be used to take the Blackfin processor out of any low-power operating mode. Having a battery supply V_{DDRTC} allows the removal of the V_{DDINT} and V_{DDEXT} supplies, thus significantly reducing total average power consumption. As a worst-case example, P_{DDEXT} is 180 µW, which is the product of the maximized V_{DDRTC} (3.6 V) and the high end of the I_{DDEXT} range (50 µA) provided in the data sheet.

Total Power Consumption

For a given system, total power consumption is the sum of its individual components - power consumed by internal circuitry, power consumed due to switching I/O pins, and power consumed by the RTC circuitry, as follows:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT} + P_{DDRTC}$$

Equation 10. Total Power (P_{TOTAL}) Calculation

Where :

P_{DDINT} = Internal power consumption as defined by Equation 4

P_{DDEXT} = External power consumption as defined by Equation 7

P_{DDRTC} = RTC power consumption as defined by Equation 9

For example, assuming that the processor in Figure 5 is operating under the conditions detailed in the example (the processor operating at 1.2 V, 400 MHz, and code as profiled in Figure 2), and also assuming that the resulting T_J has been estimated to be +100°C (see Appendix A for estimating T_J), the total estimated power consumed for the high-performance processor would be:

$$P_{TOTAL} = 600\ mW + 166.71\ mW + 0.18\ mW = \sim 767\ mW$$

Figure 6. Total Power (P_{TOTAL}) Calculation for Sample Shown in Figure While Running Code Described in Equation 5

Conclusion

Several variables affect the power requirements of an embedded system. Measurements published in the Blackfin processor data sheets are indicative of typical parts running under typical conditions. However, these numbers do not reflect the actual numbers that may occur for a given processor under non-typical conditions. In addition to the type of silicon that the customer could have, the ambient temperature, core and system frequencies, supply voltages, pin capacitances, power modes, application code, and peripheral utilization contribute to the average total power that may be dissipated.

The average power estimates obtained from methods described in this EE-Note indicate how much the Blackfin processor loads a power source over time. These estimates are useful in terms of expected power dissipation within a system, but designs must support worst-case conditions under which the application can be run. Do not use this average power estimation to size the power supply, as the power supply must support peak requirements.

Appendix A

For Blackfin processors, the total power budget is limited by the maximum allowed junction temperature (T_J) of the device. Please see the processor data sheet for the maximum T_J specification.

To guarantee correct operation, ensure that T_J does not exceed the maximum T_J specification. Use the following equation to determine T_J of the device while on the application's printed circuit board (PCB):

$$T_J = T_T + (P_{TOTAL} \times \psi_{JT})$$

Equation 11. Junction Temperature (T_J) Calculation

Where:

T_T = Package temperature (°C) measured at the top center of the package

P_{TOTAL} = Total power consumption (W) as defined in Equation 10

ψ_{JT} = Junction-to-top (of package) characterization parameter (°C/W)

Under natural convection, ψ_{JT} for a thin plastic package is relatively low. This means that under natural convection conditions, the typical T_J is just a little higher than the temperature at the top-center of the package (T_T). The die is physically separated from the surface of the package by only a thin region of plastic mold compound. Unless the top of the package is forcibly cooled by significant airflow, there will be very little difference between T_T and T_J. However, note that ψ_{JT} is affected by airflow and values for ψ_{JT} under various airflow conditions, and PCB design configurations are listed in the *Thermal Characteristics* section of the Blackfin processor data sheets for the 316-ball mini-BGA package.

The *Thermal Characteristics* section of the respective data sheet also provides thermal resistance (θ_{JA}) values. Data sheet values for θ_{JA} are provided for PCB design considerations only and are not recommended for verifying T_J on an actual application PCB.

Industrial applications of the mini-BGA package require thermal vias to an embedded ground plane on the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

References

[1] *ADSP-BF538/ADSP-BF538F Blackfin Embedded Processor Data Sheet.* Rev. 0, May 2007. Analog Devices, Inc.

[2] *ADSP-BF539/ADSP-BF539F Blackfin Embedded Processor Data Sheet.* Rev. 0, May 2007. Analog Devices, Inc.

[3] *External Power Spreadsheet.* Associated file with *Estimating Power for ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Processors (EE-229).* September 2006. Analog Devices, Inc.

[4] *S29AL008D Known Good Die Datasheet Supplement*. Rev. A, Amendment 3. June 22, 2005. Spansion, LLC.

[5] *S29AL004D Known Good Die Datasheet Supplement*. Rev. A, Amendment 3. May 3, 2006. Spansion, LLC.

[6] *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228).* Rev 1, February 2005. Analog Devices, Inc.

Document History

Revision	Description
Rev 2 – July 12, 2007 by Joe B.	Updated to new format. Includes full power characterization data
Rev 1 – October 9, 2006 by Joe B.	Initial release