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USB OTG Interface for ADSP-BF533 Blackfin® Processors

Contributed by Daniel Zhao   *Rev 1 – March 13, 2006*

Introduction

Connectivity is an essential part of nearly every electronic system. Today, an increasing number of mobile consumer electronics products, such as portable digital assistants (PDAs), mobile phones, digital cameras, and portable storage devices use the Universal Serial Bus (USB) interface to exchange data with host PCs. While increased user convenience and functionality could be achieved if these products communicate with each other directly, the USB 2.0 specification makes this difficult to achieve. The USB standard was recently enhanced to include On-The-Go (OTG) functionality, enabling point-to-point data exchange between mobile products. New products compliant with OTG specifications may support both traditional host-based (PC) and device-to-device connectivity.

OTG dual-role devices must support both limited-host and peripheral modes. For peripheral mode, full-speed operation is required and high-speed is optional. In limited-host mode, full-speed operation is required, and low- and high-speeds are optional.

For most applications, the full-speed or the high-speed is sufficient to transport user data between a host and device, or between two devices. USB connectivity is performed by a USB controller, but it also requires a processor capable of controlling the USB processing with the associated protocol and signal processing tasks.

The Blackfin® family of processors provides a high-performance, power-efficient processor choice for today's most demanding convergent signal processing applications. With Blackfin performance, applications can now perform greater signal processing tasks without significantly increasing their system cost. This EE-Note discusses a glueless interface between a USB OTG controller and an ADSP-BF533 Blackfin processor. It also describes software requirements for host mode and slave mode operations. A schematic of the connection is also provided.

Device Selection

USB controllers are currently available from a wide variety of vendors. For this note, the ISP1362 from Philips was selected as the USB OTG controller. The ISP1362 is a single-chip USB host controller (HC), device controller (DC), and OTG controller. The HC portion of the ISP1362 complies with USB specification 2.0, supporting data transfer at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s). The DC portion of the ISP1362 also complies with USB specification 2.0, supporting data transfer at full-speed (12 Mbit/s). The OTG controller is fully compliant with the OTG supplement to the *USB 2.0 Specification* [1]. The target applications of the ISP1362 are embedded systems and portable devices. It has a 16-bit parallel data bus for interfacing to the processor in addition to separate I/O addresses.

USB OTG Interface

The ISP1362 has two USB ports: port 1 and port 2. Port 1 can be configured in hardware to function as a downstream port, an upstream port, or an OTG port. Port 2 can be used only as a downstream port. When port 1 is configured in OTG mode, it can be used as an OTG dual-role device. As a host, the ISP1362 can support all four types of transfers (interrupt, control, bulk, and isochronous) at full- or low-speed. As a device, the controller can be programmed to any of the four transfer types. The OTG mode can be set in the USB OTG daughter board via jumpers.

The ISP1362 provides the programmed I/O (PIO) mode for external processors to access internal control registers and memory buffers. This space includes four I/O ports or memory locations of a processor.

The ADSP-BF533 processor can read/write to the internal control registers and memory of the ISP1362 through the PIO operating mode. Figure 1 shows the connections required between the ISP1362 and ADSP-BF533 processor.

The ISP1362 has a 16-bit data bus, so it is well-suited to connect to the ADSP-BF533 processor. The ISP1362 also provides two interrupt signals to the ADSP-BF533 processor. One is from the DC, and the second is from the host HC.
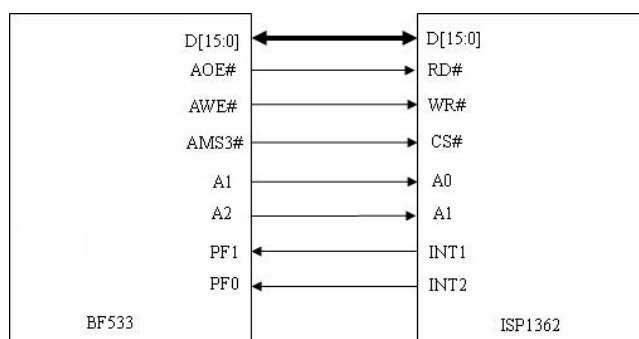

Figure 1. PIO Mode BF533/ISP1362 Interface

Hardware

The schematics for the USB OTG daughter board can be found in the ZIP file associated with this EE-Note. Figure 2 shows a picture of the actual hardware.
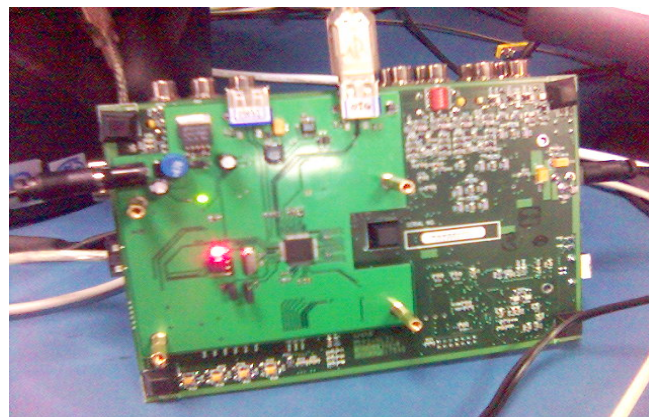

Figure 2. Photo of Board

Slave Mode Firmware

Designers must implement peripheral firmware before data can be transferred with the USB host (PC). The USB 2.0 specification defines a series of protocols related to the format and timing of the data transmission between the two devices. To be certified as USB-compliant, a device must pass an automated set of tests that check responses to a comprehensive suite of requests. Chapter 9 of the USB specification lays out the details for these requests. The host operates a device using the device's control endpoint 0. When successfully responding to these requests, the USB device can be recognized by the host and can communicate with the host by programmable endpoints. A host driver for the device, as well as host software, is needed before the Blackfin processor can communicate with the USB device.

Host Mode Firmware

The host mode firmware is more complex than slave mode because the master itself must

enumerate (get the device descriptor etc.) many kinds of USB devices successfully. The USB 2.0 specification provides more details about the procedure.

After successfully enumerating the devices, the master can get the device ID and device type. For example, the master knows which USB-compliant device is plugged into the USB OTG socket (e.g., HID device, mass storage device, etc.). Designers must implement related protocols before starting communication with the USB device.

Schematics

Schematics are provided in a ZIP file that is associated with this EE-Note.

Conclusion

Although the ADSP-BF533 Blackfin processor does not have a USB controller, external USB controllers can be used directly without any glue logic.

References

[1]   *Universal Serial Bus Specification.* Rev 2.0, April 27, 2000. Compaq Computer Corp., Hewlett-Packard Co., Intel Corp., Lucent Technologies Inc., Microsoft Corp., NEC Corp., Koninklijke Philips Electronics N.V.

[2]   *ADSP-BF533 Blackfin Embedded Processor Data Sheet.* Rev. B. Analog Devices, Inc.

[3]   *ISP1362 USB OTG Controller Data Sheet,* Rev.03. Philips Electronics.

[4]   *ADSP-BF533 Hardware Reference Manual.* Rev. 2.0, May 2004. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – March 13, 2006 *by Daniel Zhao*	Initial version