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APPLICATION NOTE

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Designing an Inverting Buck Boost Using the ADP2300 and ADP2301 Switching Regulators

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INTRODUCTION

Designers of dc-to-dc converters need versatile switching controllers and regulators that allow them to solve as many power management challenges as possible. Analog Devices, Inc., power management ICs provide this versatility and can reduce complexity, time to market, and system cost, and increase design robustness. The ADP2300 and ADP2301 (ADP230x) switching regulators from Analog Devices can provide asynchronous buck functionality from 20 V_{IN} down to 0.8 V_{OUT} at up to 1.2 A of output current at switching frequencies of 700 kHz or 1.4 MHz. The implementation of the buck topology is well-documented in the ADP230x data sheet and supported by the ADP230x Buck Designer Tool, an extension of the Analog Devices ADIsimPower dc-to-dc voltage regulator design tool.

Although targeted for voltage step-down applications, the versatility of the ADP230x family allows it to realize an inverting buck boost topology without additional cost, component count, or size. DC-to-dc voltage inverters are commonly needed to create negative voltages from a positive intermediate system voltage to power amplifiers, analog-to-digital and digital-to-analog converters, comparators, and other analog circuitry. This application note explores how to implement the ADP230x in an asynchronous inverting buck boost topology to generate negative voltages from positive power supplies.

INVERTING BUCK BOOST TOPOLOGY BASICS

The simplified inverting buck boost topology is shown in Figure 1. The topology consists of an inductor, two power switches operating out of phase from one another, and input and output capacitors. Figure 2 and Figure 3 show the current flow diagrams during the on time and off time, respectively. During the on time, the primary switch (Q_P) is conducting and current is flowing from the input and charging the inductor (L1) while the output capacitor (C_{OUT}) provides energy to the load (R_{LOAD}). During the off time, the secondary switch (D_S) is conducting and current is flowing through the inductor to the load and the output capacitor. Because this is an inverting topology, the current flows from ground to V_{OUT}, which is negative, through the load.

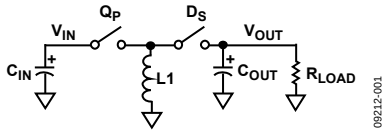

Figure 1. Inverting Buck Boost

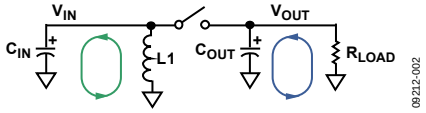

Figure 2. Current-Flow Diagram—On Time—Q_P Closed and D_S Open

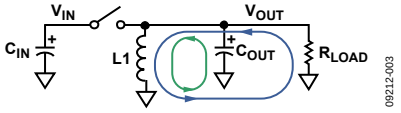

Figure 3. Current-Flow Diagram—Off Time—Q_P Open and D_S Closed

Applying the principles of inductor volt-second balance and capacitor charge balance on a lossless system, one finds the steady state dc conversion ratio specified in Equation 1 and the dc value of the inductor current in continuous conduction mode (CCM) specified in Equation 2.

$$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D} \quad (1)$$

$$IL1_{DC} = \frac{I_{OUT}}{1-D} \quad (2)$$

The inductor current also has an ac component (ΔIL1), which is calculated in Equation 3 and shown graphically in Figure 5.

$$\Delta IL1 = \frac{V_{IN} \times D}{L1 \times f_{SW}} \quad (3)$$

where f_{SW} is the fixed switching frequency of the power converter.

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REVISION HISTORY

9/10—Rev. 0 to Rev. A

Changes to Equation 2 and Equation 3 1
Changed ΔIL to ΔIL1 Throughout 1
Changes to Figure 5 and Figure 6 3
Changes to Equation 6, Equation 7, Equation 8, Equation 9, and Equation 10 4
Changed ESR to ESR_{COUT} 4
Changes to Equation 13, Equation 14, Dgespc 5* Equation 15, Cos_rgml 16, and Equation 16 5

8/10—Revision 0: Initial Version

IMPLEMENTATION WITH THE ADP230x

The inverting buck boost topology is implemented with the ADP230x switching regulator with a slight reconfiguration of the buck implementation. One of the two main significant circuit reconfigurations requires that the GND pin of the IC and the feedback resistor ($R_{FB}2$) connect to the negative output voltage node and not to system ground (see Figure 4). The other major reconfiguration requires swapping the inductor and the secondary switch locations in the buck circuit.

The primary switch (Q_P) is internal to the regulator whereas the secondary switch (D_S) is external and implemented with a diode.

By referencing the IC to the negative output voltage, the voltage polarity across all pins of the IC appears positive with reference to the GND pin. It is important to understand that the input voltage plus the absolute value of the output voltage is now seen by the IC between the VIN and GND pins when the converter is operating. According to the data sheet, the maximum voltage rating between V_{IN} and GND of the ADP230x is 20 V. Thus, the V_{IN} and V_{OUT} relationship must satisfy Equation 4.

$$20\ V \le V_{IN} + |V_{OUT}| \quad (4)$$

The ADP2300 employs a switching frequency (f_{sw}) of 700 kHz whereas the ADP2301 employs a switching frequency of 1.4 MHz. Generally, lower switching frequency results in higher efficiency and a larger design.

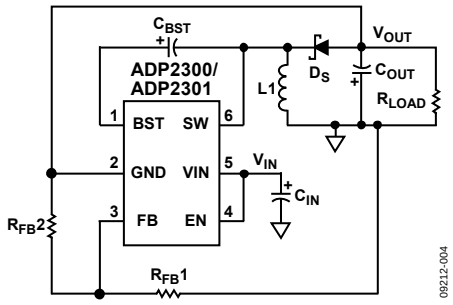

Figure 4. Inverting Buck Boost Topology As Implemented with the ADP230x

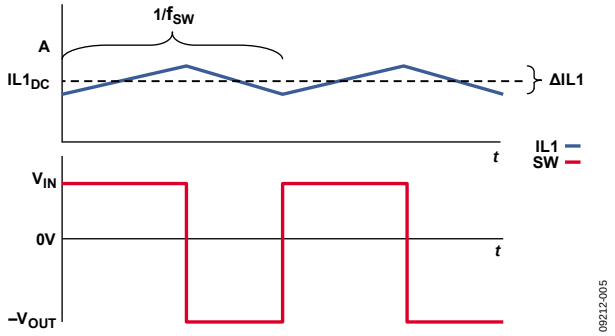

Figure 5. Ideal Current and Voltage Waveforms

DIODE SELECTION

The average current in the diode is the output current of the converter, so an appropriately sized diode should be selected. The lower the forward voltage drop of the diode is, the higher degree of efficiency is attained. The diode dc blocking rating should be greater than the input voltage plus the absolute value of the output voltage. Schottky barrier diodes are recommended for their relatively low reverse recovery time and low forward voltage drop.

After the power diode is selected, the forward voltage drop specification (V_f) at the relevant forward current can be used to modify the duty cycle equation for a higher accuracy calculation.

$$D = \frac{V_f - V_{OUT}}{V_{IN} - V_{OUT} + V_f} \quad (5)$$

INDUCTOR SELECTION

The selection of the inductor and the output capacitor has both large-signal and small-signal repercussions, and the values of both of these parts are inherently interwoven. Following the procedure set in Equation 6 through Equation 14 ensures the resultant circuit is a robust design that meets both large-signal requirements and is small-signal stable.

The peak inductor current (Ipk) is calculated by adding the dc component and half of the peak-to-peak inductor current ripple, as shown in Equation 6. Select an inductor with a saturation current greater than this value. Note that the dc component of the inductor current and the peak-to-peak inductor current ripple are proportional to the input voltage, so calculate the peak inductor current at the maximum input voltage (V_{INmax}). The peak inductor current is also the peak current in the internal primary power switch, which is the sense element used to determine whether to induce current limit. To avoid premature current limit, the peak inductor current should not exceed 1.5 A. Taking into account this maximum inductor current, the application space of the ADP230x in the inverting buck boost topology for common input voltages is shown in Figure 6 with the assumption that the peak-to-peak inductor current ripple in the inductor is 40% of the dc inductor current.

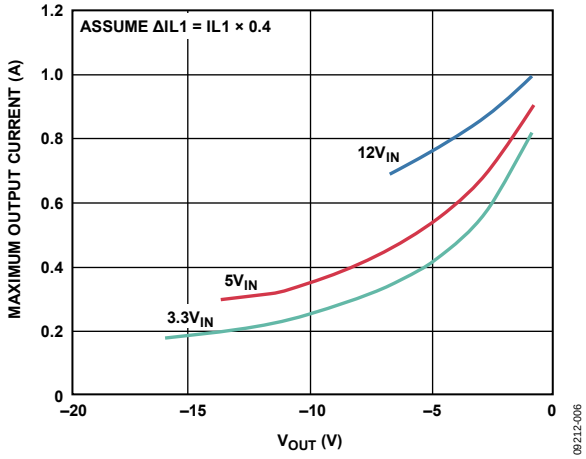

Figure 6. Approximate Application Space for Common Input Voltages

$$Ipk = IL1_{DC} + \frac{\Delta IL1}{2} \quad (6)$$

The ADP230x employs a classic peak current mode architecture that increases its versatility and performance in many respects. It also requires slope compensation to avoid subharmonic oscillations. Slope compensation is internally set inside the IC and constrains the inductor value for any given application, as specified in Equation 7. Selecting an inductor such that it obeys the inequality ensures that the quality factor of the sampling poles associated with current mode control stays between 0.25 and 1.25, resulting in a stable control loop across the full input voltage range (see "A New Small-Signal Model for Current-Mode Control" by Ridley in the References section).

$$\frac{V_{IN\,min}}{\left(\frac{|V_{OUT}|}{12}+1\right)\times 10^6 \times x}\times \left[\frac{1}{1.25\pi(1-D_{V_{IN\min}})}+\frac{0.5}{(1-D_{V_{INmin}})}-1\right] \le L1 \le \frac{V_{IN\,max}}{\left(\frac{|V_{OUT}|}{12}+1\right)\times 10^6 \times x}\times \left[\frac{1}{0.25\pi(1-D_{V_{IN\,max}})}+\frac{0.5}{(1-D_{V_{INmax}})}-1\right] \quad (7)$$

where x = 1 for the ADP2300 and x = 2 for the ADP2301.

Another consideration when selecting the inductor is its influence on the location of the right-half-plane-zero (RHPZ) in the small-signal transfer function. A shown in Equation 8, the inductor value is inversely proportional to the frequency of the RHPZ, and the higher the frequency of the RHPZ is, the higher the maximum potential converter bandwidth becomes.

$$f_z = \frac{(1-D)^2 R_{LOAD\,min}}{2\pi DL1} \quad (8)$$

The inductor value also influences the peak-to-peak output voltage ripple, as shown in the Output Capacitor Selection section.

OUTPUT CAPACITOR SELECTION

As shown in the current flow diagrams (see Figure 2 and Figure 3), output current is discontinuous in the inverting buck boost topology. This requires that the output capacitor supply energy to the load during the on time when energy stored in the inductor is increasing. During the off time, the inductor is delivering energy to both the load and the output capacitor. The polarity of the current through the output capacitor changes when the converter switches from the on time to the off time, as shown in Figure 7. The output capacitor and its equivalent series resistance (ESR_{COUT}) in combination with the inductor value and load current dictate the peak-to-peak output voltage ripple (see Equation 9). This equation suggests that the peak voltage deviation due to charge depletion on the output capacitor and the peak voltage across the ESR occurs at the same time. This is not necessarily true, but it is an excellent predictor for low ESR capacitors, which is most common in the relevant application space.

$$\Delta V_{ripple} \approx \frac{(IL1_{DC} - I_{OUT\,max})(1-D)}{f_{SW}\times C_{OUT}} + (IL1_{DC} + \frac{\Delta IL1}{2})\times ESR \quad (9)$$

If the frequency of the RHPZ is sufficiently low, it dictates the minimum amount of output capacitance needed to ensure small-signal stability across the full load range, as seen in Equation 10 and Equation 11.

$$C_{OUT\,min} = \frac{(1+D)\sqrt{\left[\frac{(1-D)\times R_{LOAD\,min}}{|V_{OUT}|(1+D)f_m}\right]^2 \times \left[1+1.54\times 10^{-8} f_m{}^2\right]\times t - 1}}{2\pi f_m R_{LOAD\,min}} \quad (10)$$

where:

$$f_m = \text{Minimum}\left(\frac{f_z}{10}, \frac{f_{sw}}{15}\right) \quad (11)$$

$t = 1.96 \times 10^{10}$ for the ADP2300 and $t = 7.84 \times 10^{10}$ for the ADP2301.

Equation 10 is not in a low entropy form, but the lack of simplicity to accurately calculate this parameter may be the reason there is a scarcity of documentation published regarding how much capacitance is necessary for small-signal stability with switching regulators operating in the inverting buck boost topology. The derivation of this equation is based on the simple model of the buck boost topology for current programmed control derived in the *Fundamentals of Power Electronics* by Erickson and Maksimović (see the References section) with the ADP230x internal parameters appropriately applied.

The low frequency pole due to the output capacitor, resistive load, and the duty cycle must be close to the compensation zero frequency internally set in the ADP230x as specified in Equation 12 to ensure adequate phase margin.

$$4\text{ kHz} \le \frac{(1+D)}{R_{LOAD\,min}\times C_{OUT}} \le 12\text{ kHz} \quad (12)$$

It is possible that the minimum capacitance value dictated by Equation 10 is higher than the maximum capacitance dictated by Equation 12. If this situation arises, reduce the selected inductance while staying within the bounds set by Equation 7 and check the relationships of the minimum and maximum capacitance value targets again. This may be an iterative process.

The output capacitance's ESR introduces a zero in the small-signal transfer function. The location of this zero should not violate the following inequality:

$$\frac{1}{2\pi \times ESR_{COUT} \times C_{OUT}} \geq f_m \times 10 \quad (13)$$

The discontinuous nature of the output current suggests that the rms current in the output capacitor can be high. A capacitor with an rms current rating greater than that calculated in Equation 14 should be selected.

$$C_{OUT\,I\,rms} = \sqrt{I_{OUT}{}^2 D + (1-D) \times \left[(IL1_{DC} - I_{OUT})^2 + \frac{1}{3}\left(\frac{\Delta IL1}{2}\right)^2 \right]} \quad (14)$$

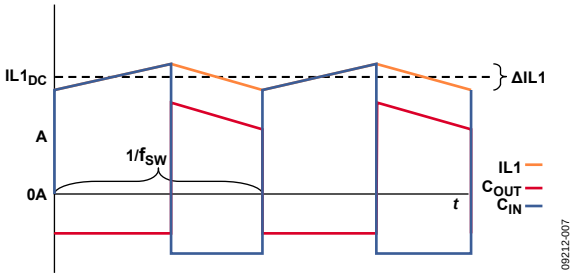

Figure 7. Ideal Current Waveforms for Inductor, C_{OUT}, and C_{IN}

The equations in this application note use one of many methodologies to ensure small-signal stability of the converter. Other approaches can be used but the approach outlined previously ensures that the converter is stable in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) of operation (see the Discontinuous Mode of Operation section).

INPUT CAPACITOR SELECTION

As with the output current, the input current is discontinuous in the inverting buck boost topology. Assuming that the input voltage deviation due to the energy depletion of the input capacitor during the on time cannot be greater than 5% of the input voltage, Equation 15 calculates the minimum input capacitance to meet the hold-up requirement. This equation assumes that a high impedance source is powering the switcher. Additionally, Equation 16 specifies the rms rating required on the input capacitor with the same assumption.

$$\Delta V_{IN} = V_{IN} \times 0.05 = \left[IL1_{DC} + \frac{\Delta IL1}{2} \right] ESR_{CIN} + \frac{IL1_{DC} D}{C_{IN} f_{SW}} \quad (15)$$

Where ESRCIN is the equivalent series resistance of the input capacitor.

$$C_{IN\,rms} = \sqrt{D\left[\frac{(IL1_{DC} D)}{(1-D)}\right]^2 \times (1-D)\left[IL1_{DC}{}^2 + \frac{1}{3}\left[\frac{\Delta IL1}{2}\right]^2 \right]} \quad (16)$$

Although the majority of the capacitance on the input voltage rail is referenced to ground, an additional input decoupling capacitor placed from the input voltage to the output voltage can reduce output voltage ripple and improve transient response. Quantifying this effect is complicated because it requires system-level knowledge and analysis on the impedance looking away from the input of the switcher. Practical experience shows that most designs benefit with faster transient response and lower output voltage ripple by having an appropriately rated 2.2 µF MLCC for C_{IN2} (shown in Figure 8). If the circuit is noticeably susceptible to noise, it may be necessary to include this capacitor in the final design.

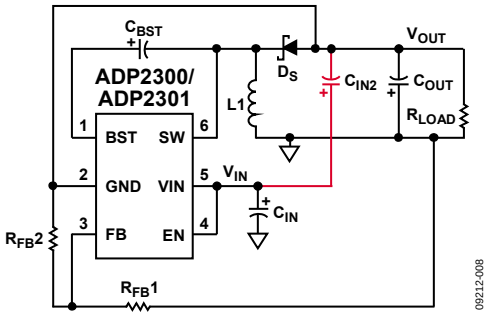

Figure 8. Inverting Buck Boost Topology with V_{IN} to V_{OUT} Connected Capacitor

DISCONTINUOUS MODE OF OPERATION

Because the inverting buck boost topology is implemented with a unidirectional secondary power switch (Ds), it is possible for the converter to enter into DCM operation at light loads. In DCM, there is a period of the switching cycle when neither of the power switches conduct, resulting in a fundamentally different converter. As specified in Equation 16, if the reduced output loading results in a dc inductor current that is less than half of the peak-to-peak inductor current (ΔIL1), the converter enters DCM. It is necessary to design the circuit to accommodate for this operation because loads can often go idle, resulting in very little output current. Occasionally, converters are designed such that they always operate in DCM even at full loading. Although the rms currents in the power components are likely significant in such a converter, the RHPZ is no longer present in the small-signal analysis, which maximizes the potential bandwidth of the converter. The procedure to design an exclusively DCM converter across the full load range is not covered in this application note, but it is important to be aware of the possibility.

$$I_{OUT} \leq \frac{\Delta IL1}{2}(1-D) \quad (16)$$

LEVEL SHIFTING THE ENABLE SIGNAL

The ADP230x has an EN pin to enable and disable the converter. In the inverting buck-boost design, the IC is referenced to the negative output voltage instead of ground. It is entirely possible that if the EN pin were connected to system ground with the intention of disabling the converter, the ADP230x may still be switching.

If the enable functionality is needed, the circuit shown in Figure 9 can be used to level shift the enable signal to the negative output voltage. Note that the precision enable feature of the ADP230x is lost when a level shifting circuit is used. If the enable functionality is not needed, no level shifting is necessary. In this case, simply connect the EN pin to the input voltage, as shown in Figure 4.

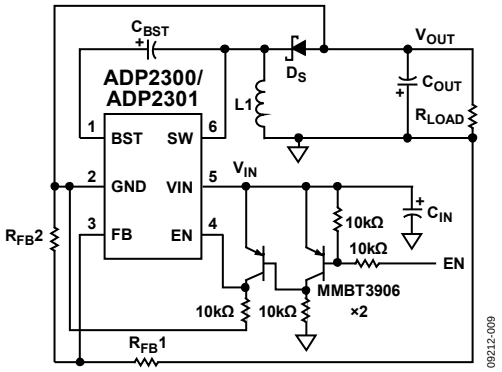

Figure 9. Level Shifting Circuit for the Enable Input

CONCLUSION

Implementation of the ADP230x in the inverting topology can be as simple, inexpensive, and small as the buck implementation. Documentation is relatively sparse on how to design an inverting buck boost that meets large-signal requirements and is small-signal stable, but by following the design equations in this application note, the designer can ensure a robust design that satisfies both requirements.

REFERENCES

Erickson, Robert and Dragan Maksimović. 2001. *Fundamentals of Power Electronics.* Chapter 12, Section 3. Norwell, MA: Kluwer Academic Publishers.

Ridley, Raymond. 1990. "A New Small-Signal Model for Current-Mode Control". Ph.D. Dissertation, Virginia Polytechnic Institute and State University.

RELATED LINKS

Table 1.

Resource	Description
ADP2300	Product page, 1.5 A peak switch current, 20 V, 700 kHz nonsynchronous switching regulator
ADP2301	Product page, 1.5 A peak switch current, 20 V, 1.4 MHz nonsynchronous switching regulator
ADP2300/ADP2301 Buck Designer Tool	Excel-based buck design tool
ADIsimPower	Web-based dc-to-dc voltage regulator design tool

APPENDIX—REFERENCE DESIGNS

Figure 8 is the schematic corresponding to all reference designs.

Reference Design 1: 5 V_{IN}, −12 V_{OUT}, I_{OUT} = 200 mA

Table 2. Bill of Materials for Reference Design 1

Qty.	Designator	Part Number	Manufacturer	Value	Package	Description
1	U1	ADP2300	Analog Devices	700 kHz	6-lead TSOT	Current mode regulator
1	L1	LPS4414-822	Coilcraft	8.2 µH	4.3 mm × 4.3 mm × 1.4 mm	Primary power inductor
2	C_{IN}	C2012X5R1C475K	TDK	4.7 µF/16 V/X5R	0805	MLCC/V_{IN} to GND input capacitor
1	C_{IN2}	C3216X7R1E225K	TDK	2.2 µF/25 V/X7R	1206	MLCC/V_{IN} to V_{OUT} capacitor
3	C_{OUT}	C2012X5R1C475K	TDK	4.7 µF/16 V/X5R	0805	MLCC/output capacitor
1	C_{BST}	C0805C104K5RACTU	Kemet	100 nF/50 V/X7R	0805	Charge pump capacitor
1	D_S	B0530W	Diodes, Inc	Schottky barrier	SOD-123	Power switch
1	$R_{FB}1$	E96 1% tolerance	Vishay	140 kΩ		Resistor feedback divider
1	$R_{FB}2$	E96 1% tolerance	Vishay	10 kΩ		Resistor feedback divider

Reference Design 2: 3.3 V_{IN}, −5 V_{OUT}, I_{OUT} = 250 mA

Table 3. Bill of Materials for Reference Design 2

Qty.	Designator	Part Number	Manufacturer	Value	Package	Comment
1	U1	ADP2301	Analog Devices	1.4 MHz	6-lead TSOT	Current mode regulator
1	L1	EPL2010-222	Coilcraft	2.2 µH	2 mm × 1.9 mm × 1 mm	Primary power inductor
2	C_{IN}	C2012X5R1C475K	TDK	4.7 µF/16 V/X5R	0805	MLCC/V_{IN} to GND input capacitor
1	C_{IN2}	C2012X5R1C475K	TDK	4.7 µF/16 V/X5R	0805	MLCC/V_{IN} to V_{OUT} capacitor
2	C_{OUT}	C3216X7R1C106M	TDK	10 µF/16 V/X5R	1206	MLCC/output capacitor
1	C_{BST}	C0805C104K5RACTU	Kemet	100 nF/50 V/X7R	0805	Charge pump capacitor
1	D_S	B0530W	Diodes Inc	Schottky barrier	SOD-123	Power switch
1	$R_{FB}1$	E96 1% Tolerance	Vishay	14.7 kΩ		Resistor feedback divider
1	$R_{FB}2$	E96 1% Tolerance	Vishay	2.8 kΩ		Resistor feedback divider

Reference Design 3: 12 V_{IN}, −5 V_{OUT}, I_{OUT} = 250 mA

Table 4. Bill of Materials for Reference Design 3

Qty.	Designator	Part Number	Manufacturer	Value	Package	Description
1	U1	ADP2300	Analog Devices	700 kHz	6-lead TSOT	Current mode regulator
1	L1	LPS4414-822	Coilcraft	8.2 µH	4.3 mm × 4.3 mm × 1.4 mm	Primary power inductor
1	C_{IN}	C2012X5R1C475K	TDK	4.7 µF/16 V/X5R	0805	MLCC/V_{IN} to GND input capacitor
1	C_{IN2}	C3216X7R1E225K	TDK	2.2 µF/25 V/X7R	1206	MLCC/V_{IN} to V_{OUT} capacitor
2	C_{OUT}	C3216X7R1C106M	TDK	10 µF/16 V/X5R	1206	MLCC/output capacitor
1	C_{BST}	C0805C104K5RACTU	Kemet	100 nF/50 V/X7R	0805	Charge pump capacitor
1	D_S	B0530W	Diodes, Inc	Schottky barrier	SOD-123	Power switch
1	$R_{FB}1$	E96 1% Tolerance	Vishay	14.7 kΩ		Resistor feedback divider
1	$R_{FB}2$	E96 1% Tolerance	Vishay	2.8 kΩ		Resistor feedback divider

Reference Design 4: 5 V_{IN}, −5 V_{OUT}, I_{OUT} = 250 mA

Table 5. Bill of Materials for Reference Design 4

Qty.	Designator	Part Number	Manufacturer	Value	Package	Description
1	U1	ADP2300	Analog Devices	700 kHz	6-lead TSOT	Current mode regulator
1	L1	LPS3015-472	Coilcraft	4.7 µH	3 mm × 3 mm × 1.5 mm	Primary power inductor
2	C_{IN}	C2012X5R1C475K	TDK	4.7 µF/16 V/X5R	0805	MLCC/V_{IN} to GND input capacitor
1	C_{IN2}	C2012X5R1C475K	TDK	4.7 µF/16 V/X5R	0805	MLCC/V_{IN} to V_{OUT} capacitor
2	C_{OUT}	C3216X7R1C106M	TDK	10 µF/16 V/X5R	1206	MLCC/output capacitor
1	C_{BST}	C0805C104K5RACTU	Kemet	100 nF/50 V/X7R	0805	Charge pump capacitor
1	D_S	B0530W	Diodes, Inc	Schottky barrier	SOD-123	Power switch
1	$R_{FB}1$	E96 1% tolerance	Vishay	14.7 kΩ		Resistor feedback divider
1	$R_{FB}2$	E96 1% tolerance	Vishay	2.8 kΩ		Resistor feedback divider