Application Note

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New Features of the 71M6543F/H and 71M6543G/GH

Introduction

This application note describes the new features offered by the Teridian 71M6543F/H and 71M6543G/GH. Most of these features will also apply to its companion ICs, the single-phase 71M6541D/F and 71M6542F.

What is the 71M6543F/H/G/GH?

The new 71M6543F/H/G/GH can be thought of as a major upgrade to the 71M6513 poly-phase metering IC with features from the 71M6533, such as differential analog inputs, a fourth current input, enhanced clock system, etc., battery modes, but with the 64 KB or 128 KB flash memory space from the 71M651x and 71M653x families. However, several features that were added go well beyond those of the 71M6533 and make the 71M6543F/H/G/GH a powerful solution for any poly-phase meter.

The 71M6543F/H/G/GH will be shipped as a regular device with 0.5% accuracy over temperature (71M6543F/G) or as a temperature-trimmed device (71M6543H/GH) with 0.1% accuracy over temperature.

The enhancements offered by the 71M6543F/H/G/GH can be categorized as functional, parametric, and packaging-related, and they will be briefly explained in this document. Detailed information is available in the Target Data Sheet (TDS71M6543).

Functional Enhancements

A variety of functional enhancements were implemented with the 71M6543F/H/G/GH. These enhancements are described in this section.

Analog Inputs

Input Signal Pins

The 71M6543F/H/G/GH contains 11 analog signal input pins. Differential signal pairs are available for IA, IB, IC, and, the fourth channel, ID, which may be used to measure neutral current in poly-phase systems. When in differential mode, the pins IAP/IAN, IBP/IBN, ICP/ICN, and IDP/IDN are connected to the sensors. These inputs may be used in single-ended or differential modes, and mixed modes are possible.

Pre-Amplifier

A selectable gain of 1 or 8 is available for the IA input. The gain functions with both single-ended and differential modes. *The primary use for this low-noise pre-amplifier is to gain up low-level signals such as those generated by shunt resistor sensors.*

71M6xxx Isolation Interface

Optionally, the current inputs can be configured individually to interface to the Teridian 71M6xxx Isolation Sensor devices. In this case, the input becomes a digital communication interface compatible with the 71M6xxx, complete with pulse generator for supplying operating current to the 71M6xxx.

When using Teridian 71M6xxx Isolation Sensor devices, non-isolating sensors, such as shunt resistors, can be connected to the inputs of the 71M6543F/H via a combination of pulse transformers and the 71M6xxx Isolated Sensors. The 71M6xxx establishes a 2-way communication with the 71M6543F/H, supplying current data and auxiliary information such as sensor temperature via a serial data stream.

A total of three 71M6xxx Isolated Sensors can be supported by the 71M6543F/H/G/GH. When remote interface x is enabled, two analog current inputs IAnP and IAnN become the digital InR and InRN interface to the remote sensor.

Each 71M6xxx Isolated Sensor consists of the following building blocks:

- Power supply for power pulses received from the 71M6543F/H/G/GH
- Communication interface
- Pre-amplifier with gain of 4, 8, 16 or 32, depending on nominal current
- Delta-Sigma ADC Converter with precision bandgap reference (chopping amplifier)
- Temperature sensor
- Fuse system containing part-specific information

A sample configuration is shown in Figure 1. *The advantage of this feature is that it makes it possible to use low-cost non-isolating sensors, such as shunt resistors, in a poly-phase system by interfacing the sensors via three 71M6xxx Isolation Interfaces and low-cost pulse transformers. The electrical specifications of the pulse transformers are not critical since these transformers only carry digital signals below 1 MHz, which makes it possible to use low-cost parts.*

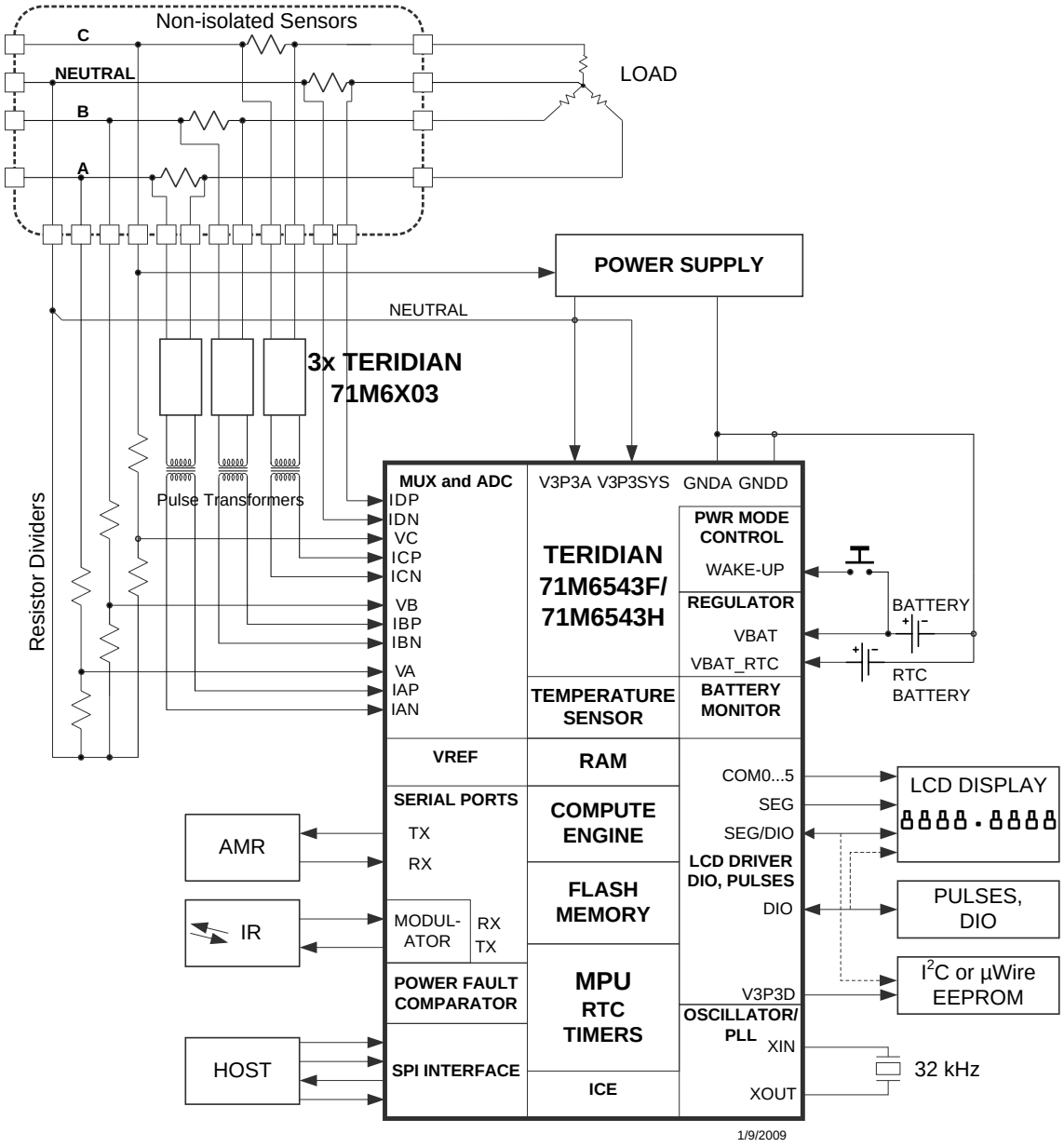

Figure 1: Interfacing Non-Isolating Sensors to the 71M6543F/H/G/GH

Temperature Sensor

The temperature sensor has been designed as a completely independent component that does not require involvement of the ADC to get a temperature measurement. After issuing a "start temperature measurement" command, the MPU has access to the die temperature almost immediately. *This scheme avoids the "alternate multiplexer cycles" used in the previous meter IC families.* Consequently, temperature compensation is based on calculations performed in the MPU, while the actual application of gain adjustment is still done by the CE.

An even more important aspect is that the temperature sensor is operational in mission mode and all battery modes including sleep mode and LCD mode, *which enables the IC to perform temperature compensation of the RTC based on the crystal properties without any MPU involvement.*

The sampling mode used in previous metering ICs made it necessary to omit current samples during temperature or battery measurement, which required valuable CE cycles for the interpolation of samples and for the averaging of temperature data (one measurements with positive chop polarity had to be added to another measurement with negative polarity), as well as MPU cycles for controlling the *CHOP_E* register. *The 71M6543F/H/G/GH saves CE and MPU bandwidth by providing a hardware-base mechanism for measuring of and compensating for temperature.*

Clock System

PLL

The PLL can run at full speed or at ¼ speed, which translates to 4.92 MHz or 1.228 MHz MPU clock speed (when *MPU_DIV* is set to 0).

ADC Clock

The ADC can be operated at nominal clock speed (4.92 MHz) or at ½ clock speed (2.4576 MHz). *The latter mode can help to preserve power.*

RTC

The RTC in the 71M6543F/H/G/GH is similar to the RTC in the 71M653x metering ICs, but offers several enhancements, especially over the 71M652x and 71M651x:

- Read and write operations are facilitated with so-called shadow registers. *This eliminates the sequential read operations necessary in the 71M651x, 71M652x, and 71M653x RTCs.*
- As in the 71M653x, a sub-second register with 1/256 seconds resolution is available.
- The readings from the temperature sensor can be used to automatically compensate the RTC for temperature-dependent variations of the crystal frequency. This feature functions without direct involvement of the MPU and is also available in BRN, LCD, and SLP modes. *This feature is a major improvement over the 71M651x, 71M652x, and 71M653x, which allowed temperature compensation only in mission mode. With the 71M6543F/H/G/GH, high RTC accuracy can be achieved over long time periods of battery operation.*
- The RTC can interrupt the MPU every second or every minute, when requested.
- The RTC can interrupt the MPU when the minute register or the hours register reach predetermined counts. *This feature is similar to an alarm clock and helps to offload the MPU.*

Battery Modes

Two Battery Pins

The 71M6543F/H/G/GH has two battery pins, VBAT and VBAT_RTC. VBAT supports the battery modes (BRN, LCD, SLP) whereas VBAT_RTC supports the oscillator, non-volatile RAM, and RTC. *That way, the integrity of non-volatile RAM and RTC is still maintained even after the battery connected to VBAT has run out of charge.*

Furthermore, various interconnections inside the IC supply the RTC in the absence of batteries. For example, applying 3.3 VDC to the V3P3SYS pin will supply current to the RTC, even when no voltage is present at the VBAT_RTC pin. *This is an improvement over the 71M653x, where a drained battery could result in loss of RTC data if a connection (via a diode) to V3P3SYS was not provided.*

Non-volatile RAM space has been extended to 128 bytes (as compared to 8 bytes in the 71M653x), which is a very useful feature for holding temporary variables.

Internal V1 divider

In the 71M651x, 71M652x, and 71M653x families of metering devices, an external resistor divider provides the reference voltage that is fed to the IC via the V1 pin. This voltage is then internally compared to VBIAS, and an automatic transition to BRN mode occurs when V1 < VBIAS.

The 71M6543F/H/G/GH replaces this design with two internal comparators that measure the voltage applied to V3P3A (the analog power supply).

- If V3P3A falls below 3.0 VDC but is still above 2.8 VDC, the 71M6543F/H/G/GH is alerted that power quality is not good enough for analog measurements, but still OK for digital operation. It is up to MPU code to decide how the device behaves in this situation. Saving billing data would be a typical task performed by a 71M6543F/H/G/GH in an electricity meter.
- If V3P3A falls below 2.8 VDC, the 71M6543F/H/G/GH is automatically forced to brownout (BRN) mode. In this mode, the MPU still performs at the clock speed that it had in mission mode. This enables the MPU to take care of data saving or communications operations with unlimited speed. If desired, the MPU code can reduce the MPU clock speed by writing to the I/O RAM register *MPU_DIV[7:0]* and thus reduce the current drawn from the battery connected to the VBAT pin.

The hardware watchdog timer (WDT) is disabled whenever the ICE_E pin is pulled high.

This implementation saves the V1 pin (for DIO), saves external components (resistor divider plus capacitor), and makes power-mode transitions more transparent.

Full MPU speed possible in BRN mode

As stated above, the MPU is capable of executing at 4.92 MHz in BRN mode, if desired. The MPU clock speed may also be reduced under MPU control to save power.

This feature makes it possible to execute speed-critical actions, such as saving of billing data, communicating with modems (AMR) etc. during BRN mode.

Orderly Shutdown at Low Battery Voltages

The voltage at VBAT needs to be maintained at above 2.0 VDC in battery modes to maintain reliable operation. Another internal comparator reflects the state of the battery voltage. When in BRN mode, the 71M6543F/H/G/GH will be forced to a "hold" mode (reset) 122 µs after VBAT < 2.0 VDC. The MPU may also put the 71M6543F/H/G/GH into SLP mode.

When waking up from SLP mode, and when VBAT is < 2.0 VDC, the 71M6543F/H/G/GH will enter BRN mode and will then forced to stay in the "hold" mode until either system power is restored or the voltage at VBAT rises above 2.0 VDC.

The battery condition (VBAT < 2.0 VDC) will be reflected in a non-volatile flag which enables the MPU to determine that this event happened.

Low voltage at the VBAT pin will not affect the oscillator, RTC, or contents of non-volatile RAM, since these circuits are powered by the VBAT_RTC pin.

Wake-Up Events

With respect to the 71M652x, a variety of events have been added for the 71M6543F/H/G/GH that cause a wakeup from SLP mode. Events triggering a wakeup are:

- Wake-up timer timeout.
- Pushbutton (PB) is activated.
- A rising edge on SEGDIO4, SEGDIO52 or SEGDIO55.
- Activity on the RX or OPT_RX pins.

Each event has its own enable flag in I/O RAM space. Event flags that reflect the hardware conditions enable the MPU to determine the exact cause of the wakeup.

This feature provides more flexibility for the meter designer when compared to the limited wake-up events (PB and wake-timer) events offered by the 71M652x and 71M653x.

Battery Monitor

The battery monitor uses the same internal circuit that measures the temperature. Again, the ADC is not involved in battery measurements.

In MSN mode, a 100 µA depassivation load can be applied to the selected battery (*TEMP_BSEL*) by setting the *BCURR* bit. Battery impedance can be measured by taking a battery measurement with and without *BCURR*. Regardless of *BCURR*, the battery load is never applied in BRN, LCD, and SLP modes.

The battery monitor of the 71M6543F/H/G/GH offers a major improvement for the meter designer over the simple battery voltage detector of the 71M652X and 71M653X.

DIO Pins

Most I/O pins are configurable as either segment drivers or DIO pins. Each DIO pin can be an input or an output. The inflexible separation between LCD and DIO pins (*LCD_NUM*) used in the 71M651x and 71M652x was eliminated in the 71M6543 (and also in the 71M653x).

Many pins have secondary or tertiary functions, providing great flexibility when configuring the device.

The I/O RAM register *PORT_E* has to be 1 for SEGDIO0 – SEGDIO15 to function as DIO pins. Since the 71M6543F/H/G/GH wakes up from a reset or power-down with *PORT_E* = 0, any glitches from DIO pins are suppressed.

Having total flexibility in configuring I/O pins for DIO or LCD functions offers a major advantage to the meter designer.

LCD System

The segment driver pins of the 71M6543F/H/G/GH can drive LCDs with up to 6 multiplexed commons. With a maximum of 56 LCD pins available, a total of 336 display segments can be driven.

An on-chip charge pump enables the 71M6543F/H/G/GH to drive LCD segments with up to 5 VDC. By comparison, the 71M651x series of metering ICs can operate a charge pump implemented with external components (two capacitors, one diode). *The 71M6543F/H/G/GH implements the charge pump without external components and saves the VLDRV pin used on the 71M651x.*

Furthermore, LCD contrast adjustment is possible using an internal LCD DAC.

The new I/O RAM registers *LCD_ON* and *LCD_BLANK* allow all segments to be switched on or off without having to change the contents of the LCD memory. A similar I/O RAM register, *LCD_CLR*, allows the MPU to clear all segment memory with one single command. *These two features save valuable MPU cycles and code space that would otherwise be spent clearing and writing to the I/O RAM locations that control the segments.*

Two TMUXOUT Ports

Two test output pins with selectable sources are now available (TMUXOUT and TMUX2OUT). These two pins are shared with regular LCD segment functions. *Extensive diagnostic capabilities are provided by the two TMUXOUT ports.*

EEPROM Interface

As the 71M651x, 71M652x, and 71M653x, the 71M6543F/H/G/GH supports EEPROMs or other external devices connected via 2-wire and 3-wire interfaces. In addition to that, the 71M6543 F/H/G/GH supports a 3-wired interface compatible with µ-Wire or SPI with separate DI and DO pins.

The added interface capabilities offer more freedom for the meter designer in selecting interface devices.

SPI Interface

The slave SPI interface available in the 71M653x is also available in the 71M6543F/H/G/GH. However, the SPI clock speed available for the 71M6543F/H/G/GH was increased to 10 MHz by changing the protocol slightly: The address field is now preceding the command field. A status byte was added as part of the command sequence.

Both single-byte and multi-byte transactions are possible.

Two new SPI operation modes offer enhancements over the 71M653x:

- SPI safe mode: This mode restricts the write access by the external host to a field of 16 RAM addresses. RAM used by MPU and CE is protected from unauthorized or erratic access, which is a useful feature for AFE applications.
- SFM Mode: In this mode, the MPU is halted, and the external host has access to the flash memory. No access to I/O RAM or XRAM is possible in this mode.

The new SPI interface offers the meter designer speed enhancements and another route for flash-programming while also providing flash security.

CE

The CE of the 71M6543F/H/G/GH has four interrupts for signaling conditions to the MPU:

- CE_BUSY
- XFER_BUSY
- XPULSE
- YPULSE

The added interrupts XPULSE and YPULSE can be configured to interrupt the MPU and indicate sag failures or other significant events. Additionally, these signals can be connected directly to DIO pins to provide direct outputs for the CE.

These enhancements improve the efficiency of the MPU code.

Parametric Enhancements

The main parametric enhancements that come with the 71M6543F/H/G/GH are:

- MSN (mission) mode power supply is in the range of 13 mW.
- SPI clock speed is 10 MHz.

Improved Pin-Out

The XIN and XOUT pins are located at the corner of the LQFP-100 package at positions 75 and 76. Pins 74-73, as well as pins 77-78 are “NC”, which provides ample clearance around the XIN and XOUT pins (see Figure 2). This feature is aimed at improving the resistance of the sensitive oscillator circuit to PCB surface contamination and moisture. It may also benefit production processes that avoid conformal coating.

The new location of the crystal pins combined with the flexibility for configuring I/O pins offer great freedom for the PCB designer and help create PCB layouts that are optimized for signal flow and EMC.

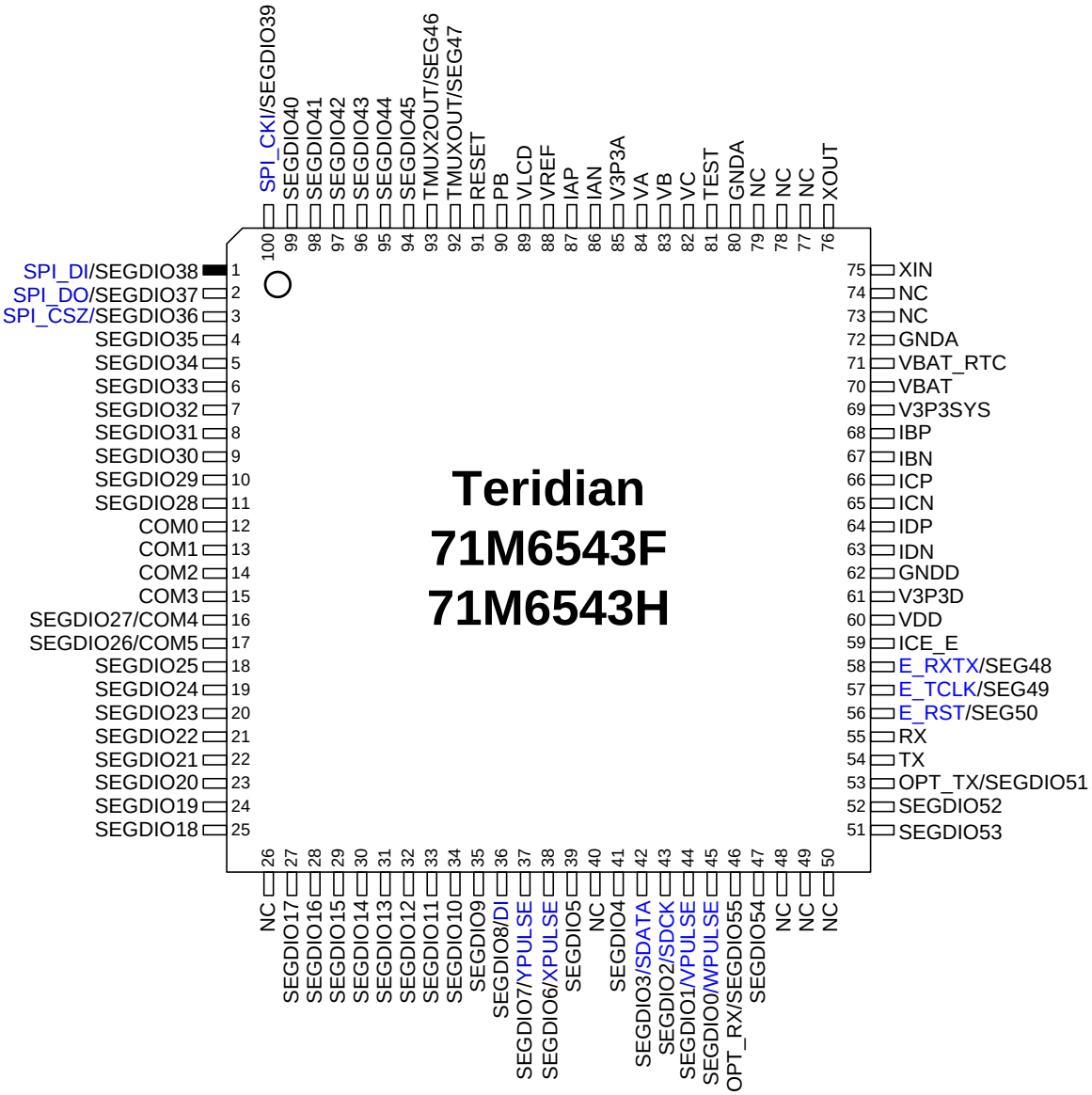

Figure 2: 71M6543F/H/G/GH Pin-Out

Revision History

Revision	Date	Description
Rev. 1.0	1/16/2009	First publication.
Rev. 1.1	6/27/2011	Added references to 71M6543G/GH, 71M6541D/F, and 71M6542F. Removed reference to preliminary data sheet.

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