MAX20710 PMBus APPLICATION NOTE

1.0 MAX20710 PMBus Interface Overview

The MAX20710 fully integrated switching regulators include a serial bus (PMBus™) that supports advanced regulator monitoring and control capabilities. This application note covers the MAX20710 silicon that reports F as the revision through the PMBus manufacturing revision command. The PMBus interface supports a subset of the PMBus 1.2 and SMBus 2.0 specifications. More information about these specifications can be found at www.pmbus.org and www.smbus.org. The following PMBus features are supported:

- Static PMBus Address programming with external resistors
- Compliant with high-power SMBus DC specification (3.1.3)
- Support PMBus protocols
- Write byte/word (5.5.4)
- Read byte/word (5.5.5)
- Send byte (5.5.2)
- Block read
- Packet error checking mechanism support (5.4)
- SMBALERT# signal

1.1 Monitoring Functions

The following monitoring functions are available through the MAX20710 PMBus interface:

- Various fault status
- Parameters programmed using R_SEL configuration resistors
- Input Voltage
- Output voltage
- Junction temperature
- Output current

1.2 Control Functions

- Overtemperature fault thresholds
- Output current fault threshold
- Output voltage command
- Output voltage minimum and maximum thresholds
- Operation–on and off configuration
- Regulation to power-good delay timing
- Soft-start timing
- Frequency
- Overcurrent protection mode
- Internal gain values
- Output voltage command ramping rate

2.0 MAX20710 PMBus Protocol

2.1 Write/Read Format

The MAX20710 PMBus interface supports single-byte, dual-byte (word) register read and write, block read, as well as send byte protocols. Table 1 through Table 6 show the format used for all supported operations. Note that packet error checking can be used on any transaction. Table 7 shows the MAX20710 PMBus command codes. A 0x0h written to write protect register (Reg_10h) disables the WRITE_PROTECT feature and 0x20h turns on the write protect to all registers except the OPERATION and VOUT_COMMAND registers.

Table 1. Read Byte Format

1	7	1	1	8	1	1	7	1	1	8	1	1
S	PMBus Address	W	ACK	Command	ACK	S	PMBus Address	R	ACK	Data Byte	ACK	P

Table 2. Write Byte Format

1	7	1	1	8	1	8	1	1
S	PMBus Address	W	ACK	Command	ACK	Data Byte	ACK	P

Table 3. Read Word Format

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	PMBus Address	W	ACK	Command	ACK	S	PMBus Address	R	ACK	Data Byte Low	ACK	Data Byte High	ACK	P

Table 4. Write Word Format

1	7	1	1	8	1	8	1	8	1	1
S	PMBus Address	W	ACK	Command	ACK	Data Byte Low	ACK	Data Byte High	ACK	P

Table 5. Send Byte Format

1	7	1	1	8	1	1
S	PMBus Address	W	ACK	Data Byte	ACK	P

Table 6. Block Read Format

1	7	1	1	8	1	1	7	1	1	8	1	1
S	PMBus Address	W	ACK	Command	ACK	S	PMBus Address	R	ACK	Byte Count = N	ACK	P
				8	1	8		1		8	1	1
				Data Byte 1	ACK	Data Byte 2		ACK	·····	Data Byte N	ACK	P

Table 1–6 Legend

S = Start condition: Clock and data lines initially high
Data transitions low while clock is high
clock transitions low

P = Stop Condition: Clock and data lines initially low
Clock transitions high while data is low
Data transitions high

R = Read bit (logic-high)

W = Write bit (logic-low)

Command = Relevant MAX20710 PMBus register

ACK = Acknowledge (logic-low)

NACK = Not acknowledge (logic-high)

Note 1: Shaded area in Tabled 1–6 are driven by the MAX20710. Unshaded areas are driven by bus host.

2: Packet Error Check (PEC) may be used in conjunction with these commands.

3: The PEC is a CRC-8 error checking byte, calculated on all the message bytes.

4: The OEN signal does not need to be high to communicate over the PMBus interface.

Table 7. MAX20710 PMBus Command Codes

COMMAND CODE	DEC	COMMAND NAME	TYPE	WIDTH	DEFAULT	LOW BYTE								HIGH BYTE							
01h	1	OPERATION	RW	1	00h	OE_INT	0	0	0	0	0	0	0								
02h	2	ON_OFF_CONFIG	RO	1	1Fh	0	0	0	1	1	1	1	1								
03h	3	CLEAR_FAULTS	WO	0																	
10h	16	WRITE_PROTECT	RW	1	20h			Prot_ Enable													
1Bh	27	SMBALERT_MASK	RW	2	NA	alert-mask [7]	alert-mask [6]	alert-mask [5]	alert-mask [4]	alert-mask [3]	alert-mask [2]	alert-mask [1]	alert-mask [0]	alert-mask [15]	alert-mask [14]	alert-mask [13]	alert-mask [12]	alert-mask [11]	alert-mask [10]	alert-mask [9]	alert-mask [8]
20h	32	VOUT_MODE	RO	1	17h	0	0	0	1	0	1	1	1								
21h	33	VOUT_COMMAND	RW	2	C_SELA	vdac[7]	vdac[6]	vdac[5]	vdac[4]	vdac[3]	vdac[2]	vdac[1]	vdac[0]	0	0	0	0	0	0	vdac[9]	vdac[8]
24h	36	VOUT_MAX	RW	2	0280h	vmax[7]	vmax[6]	vmax[5]	vmax[4]	vmax[3]	vmax[2]	vmax[1]	vmax[0]	0	0	0	0	0	0	vmax[9]	vmax[8]
78h	120	STATUS_BYTE	RO	1	00h	BUSY	OFF#	VOUT_ OV_FA ULT	IOUT_O C_FAULT	VIN_UV _FAULT	TEM-PERA-TURE	CML	NA								
79h	121	STATUS_WORD	RO	2	0000h	BUSY	OFF#	VOUT_ OV_FA ULT	IOUT_O C_FAULT	VIN_UV _FAULT	TEM-PERA-TURE	CML	NA	VOUT	IOUT/ POUT	INPUT	MFR_ SPE-CIFIC	POWE R_GO OD#	0	0	0
7Ah	122	STATUS_VOUT	RO	1	00h	ovp_flt	0	0	uvp_flt	voutma x_flt	0	0	0								
7Bh	123	STATUS_IOUT	RO	1	00h	ocp_flt	0	0	0	0	0	0	0								
7Ch	124	STATUS_INPUT	RO	1	00h	reserved	0	0	fuvlo_flt	fuvlo_flt	0	0	0								
7Dh	125	STATUS_TEMPERATURE	RO	1	00h	otp_flt	0	0	0	0	0	0	0								
7Eh	126	STATUS_CML	RO	1	00h	invalid/ unsup-ported cmd	invalid/ unsup-ported data	incor-rect PEC	0	0	0	other comm fault	0								
80h	128	STATUS_MFR_SPECIFIC	RO	1	00h	voutmin_ flt	sealr_flt	radc_flt	auvlo_flt	boost-fault	vxshort flt	vsn_vs p_flt	ldo_off								
88h	136	READ_VIN	RO	2	N/A	Vinadc_ ave [7]	Vinadc_ ave [6]	Vinadc_ ave [5]	Vinadc_a ve [4]	Vinadc_ ave [3]	Vinadc_ ave [2]	Vinadc_ ave [1]	Vinadc ave [0]	0	0	0	0	0	0	Vinadc ave [9]	Vinadc_ ave [8]
8Bh	139	READ_VOUT	RO	2	N/A	vadc_av e[7]	vadc_a ve[6]	vadc_a ve[5]	vadc_av e[4]	vadc_a ve[3]	vadc_a ve[2]	vadc_a ve[1]	vadc_a ve[0]	0	0	0	0	0	0	vadc_a ve[9]	vadc_av e[8]
8Ch	140	READ_IOUT	RO	2	N/A	iadc_ave [7]	iadc_av e[6]	iadc_av e[5]	iadc_ave [4]	iadc_av e[3]	iadc_av e[2]	iadc_av e[1]	iadc_av e[0]	0	0	0	0	0	0	iadc_av e[9]	iadc_ave [8]
8Dh	141	READ_TEMPERATURE_1	RO	2	N/A	tadc_ave [7]	tadc_av e[6]	tadc_av e[5]	tadc_ave [4]	tadc_av e[3]	tadc_av e[2]	tadc_av e[1]	tadc_av e[0]	0	0	0	0	0	0	tadc_av e[9]	tadc_ave [8]
99h	153	MFR_ID	BLK	5	N/A	ASCII "MAXIM" (hex codes 56h, 4Ch, 54h, 52h)															
9Bh	155	MFR_REVISION	BLK	1	N/A	ASCII "F" (hex code 31h)															
D1h	209	MFR_VOUT_MIN	RW	2	0133h	vmin[7]	vmin[6]	vmin[5]	vmin[4]	vmin[3]	vmin[2]	vmin[1]	vmin[0]	0	0	0	0	0	0	vmin [9]	vmin [8]
D2h	210	MFR_DEVSET1	RW	2	2061h	0	OCP[1]	OCP[0]	FSW[2]	FSW[1]	FSW[0]	TSAT [1]	TSAT [0]	0	RGAI N[1]	RGAI N[0]	OTP[1]	OTP[0]	0	VBOOT [1]	VBOOT [0]
D3h	211	MFR_DEVSET2	RW	2	03A6h	VRATE [1]	VRATE [0]	HICCU P_EN	reserved	reserve d	reserve d	SFT-START[1]	SFT-START[0]	0	0	0	0	0	IMAX[2]	IMAX[1]	IMAX[0]

* **RW** = Read Write, **RO** = Read Only, **WO** = Write Only, **BLK** = Block Read

* V_{BOOT}[1:0] values in MFR_DEVSET1 is programmed by external capacitor (C_SELA) and equal to binary value 00b here representing V_{BOOT} = 0.65V.

2.2 Configuring the MAX20710 Address

MAX20710 PMBus address is set via R_SELA. Eight unique addresses are possible, as shown in Table 8.

Table 8. MAX20710 PMBus Address Byte

PMBus ADDRESS (PMAD)	CONSTANT/VARIABLE
<6>(MSB)	Constant = 1
<5>	Constant = 0
<4>	Constant = 1
<3>	Constant = 0
<2>	R_SELA_bit2
<1>	R_SELA_bit1
<0>	R_SELA_bit0

3.0 Status Reporting

The MAX20710 supports the status registers shown in Figure 1. The CLEAR_FAULTS command is used to clear any fault bits that have been set, and clear the device's SMALERT pin output. The CLEAR_FAULTS command does not cause a unit that has been latched off for a fault condition to restart. To restart after a latched fault, power must be cycled. If the fault is still present after power is cycled, the fault bit is set again.

The STATUS_BYTE contains the most important faults and warnings. The STATUS_WORD contains two bytes of information. The low byte of the STATUS_WORD is the same as the STATUS_BYTE, and the high byte contains additional information about the status of the device.

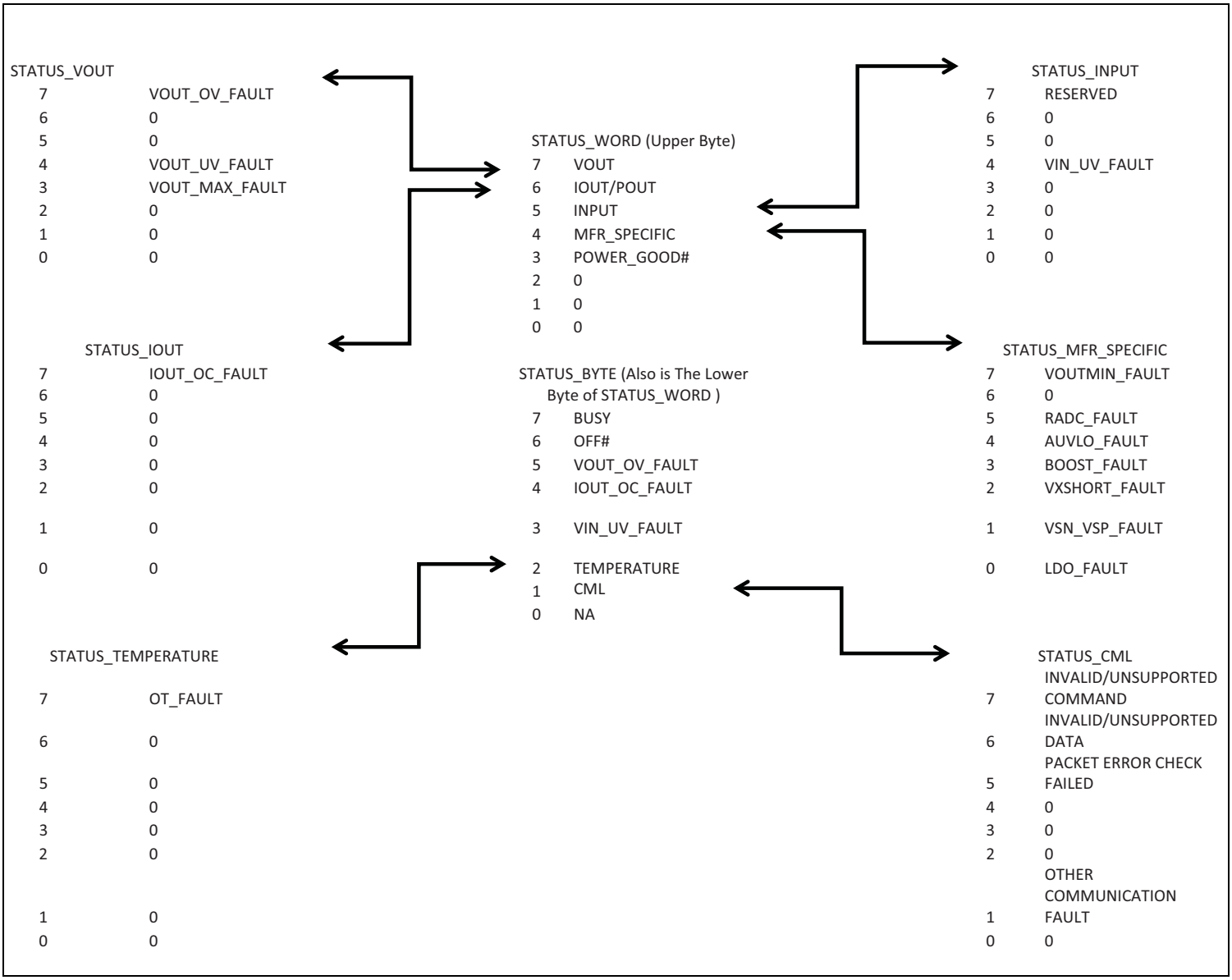

Figure 1. Summary of Status Registers

Table 9. STATUS_WORD

	BIT NUMBER	STATUS BIT NAME	MEANING
Low	7	BUSY	A fault is asserted because the device was busy and unable to respond.
	6	OFF#	This bit is asserted if the unit is providing power to the output, regardless of the reason, including simply not being enabled.
	5	VOUT_OV_Fault	An output overvoltage fault has occurred.
	4	IOUT_OC_Fault	An output overcurrent fault has occurred.
	3	VIN_UV_Fault	An input under voltage fault has occurred.
	2	Temperature	A temperature fault has occurred.
	1	CML	A communications, memory or logic fault has occurred.
	0	N/A	N/A
High	7	V_{OUT}	An output voltage fault has occurred.
	6	I_{OUT}/ P_{OUT}	An output current fault has occurred.
	5	Input	An input voltage, input current, or input power fault has occurred.
	4	MFR_SPECIFIC	A manufacturer specific fault or warning has occurred.
	3	Power_Good#	If this bit is set, power is not good.
	2	N/A	N/A
	1	N/A	N/A
	0	N/A	N/A

4.0 Control

4.1 Operation ON and OFF Configuration

The OPERATION command is used to turn on (0x80h) and turn off (0x0h) with OE pin low, as determined by the ON_OFF_CONFIG, which is fixed at 0x1Fh.

4.2 Output Voltage Control

The following registers are used for output voltage related configuration settings. All of the formats are in linear mode with N = -9 which is indicated in V_{OUT} Mode register (Reg_20h) value of 0x17h. The output voltage command (Reg_21h) and other output voltage related commands are a 2-bit unsigned variable. The output voltage formulas follow:

Equation 1

$$\frac{V_{OUT}}{V} = \text{Reg\_21h<bit 15-0>} \bullet 2^{-9}$$

Equation 2

$$\frac{V_{OUT\ MAX}}{V} = \text{Reg\_24h<bit 15-0>} \bullet 2^{-9}$$

Equation 3

$$\frac{V_{OUT\ \text{Min}}}{V} = \text{Reg\_D1h<bit 15-0>} \bullet 2^{-9}$$

4.3 Configuration Registers

PGMA and PGMB configuration resistors and capacitors are used to configure PMBus address, soft start timing, boot voltage overcurrent protection limit, internal gain setting and frequency. There are two PMBus registers, MFR_DEVSET1 and MFR_DEVSET2 that can be used to check and override these settings. The other system parameters that can be changed by these two configuration registers include regulation to power good delay timing, overtemperature protection limit, output voltage command ramping rate, and overcurrent protection mode. Note that the override parameters revert back to default values once power is cycled.

Table 10. PGMA (R_SELA)

NO.	R (kΩ)	SS TIME (ms)	SLAVE ADDRESS (1010_xxx)
1	1.78	3	PMBus Slave Address 1010 000b
2	2.67	3	PMBus Slave Address 1010 001b
3	4.02	3	PMBus Slave Address 1010 010b
4	6.04	3	PMBus Slave Address 1010 011b
5	9.09	3	PMBus Slave Address 1010 100b
6	13.3	3	PMBus Slave Address 1010 101b
7	20	3	PMBus Slave Address 1010 110b
8	30.9	3	PMBus Slave Address 1010 111b
9	46.4	1.5	PMBus Slave Address 1010 000b
10	71.5	1.5	PMBus Slave Address 1010 001b
11	107	1.5	PMBus Slave Address 1010 010b
12	162	1.5	PMBus Slave Address 1010 011b

MFR_DEVSET2 (Reg_D3h<bit 1-0>) is used to program the soft-start timing as shown in Table 11.

Table 11. Soft Start Timing

SS_SEL[1:0]	SOFT-START (ms)
00b	0.75
01b	1.5
10b	3
11b	6

MFR_DEVSET1 (Reg_D2h<bit 9-8>) is used to read the boot voltage as shown in Table 12.

Table 12. Boot Voltage

V_{BOOT}_SEL[1:0]	V_{BOOT} VOLTAGE (V)
00b	0.6484
01b	0.8984
10b	1.0
11b	N/A

4.4 Other System Parameters

4.4.1 Overcurrent Protection

Overcurrent protection MFR_DEVSET1 (Reg_D2h <bit 6-5>) is used to set the positive and negative overcurrent inception and clamp level as shown in Table 13.

Table 13. OCP Settings

OCP[1:0]	OCP Setting
00b	Setting 0
01b	Setting 1
10b	Setting 2
11b	Setting 3

4.4.2 Temperature Control

MFR_DEVSET1 (Reg_D2h<bit 12-11>) is used to program the over temperature trigger level as shown in Table 14.

Table 14. Overtemperature Shutdown Limit

OTP_SEL[1:0]	OVERTEMPERATURE (°C)
00b	150
01b	130
10b	N/A
11b	N/A

4.4.3 Internal Gain Setting

MFR_DEVSET1 (Reg_D2h<bit 14-13>) is used to program the internal gain setting as shown in Table 15.

Table 15. Internal Gain Setting

GAIN[1:0]	R_{GAIN} (mΩ)
00b	0.9
01b	3.6
10b	1.8
11b	7.2

4.4.4 Boot Voltage to Output Voltage Command Ramp Rate

MFR_DEVSET2 (Reg_D3h<bit 7-6>) is used to program the boot voltage to output voltage command ramp rate as shown in Table 16.

Table 16. Output Voltage Ramping Rate

V_{RATE}_SEL[1:0]	V_{RATE} (mV/µs)
00b	4
01b	2
10b	1
11b	N/A

4.4.5 Frequency

MFR_DEVSET1 (Reg_D2h<bit 4-2>) is used to program the switching frequency as shown in Table 17.

Table 17. Frequency Register

FREQ_SEL[2:0]	FREQ (kHz)
000b	400
001b	500
010b/011b	600
100b	700
101b	800
110b/111b	900

4.4.6 Regulation to Power Good Delay Timing

MFR_DEVSET1 (Reg_D2h<bit 1-0>) is used to program the t_{STAT} time, as shown in Table 18.

Table 18. t_{STAT} Register

TSTAT_SEL[1:0]	t_{STAT} TIME (µs)
00b	2000
01b	125
10b	62.5
11b	32

4.4.7 Output Current Overcurrent Mode

MFR_DEVSET2 (Reg_D3h<bit 5>) is used to program the output current overcurrent mode as shown in Table 19.

Table 19. Overcurrent Protection Mode

CODE (BINARY)	OCP MODE
0b	Constant Current
1b	Hiccup

4.4.8 Read Telemetry Selection

MFR_DEVSET2 (Reg_D3h<bit 13>) is used to turn off read telemetry and MFR_DEVSET2 (Reg_D3h<bit 12-11>) is used to select the monitoring parameters as shown in Table 20.

Table 20. Read Telemetry Selection

TELEM_FRC_EN	TELEM_MODE[1:0]	MODE
0b	00b-11b	All
1b	00b	V_{OUT} only
1b	01b	V_{IN} only
1b	10b	Temp only
1b	11b	I_{OUT} only

5.0 Read Telemetry

The MAX20710 provides reporting of junction temperature, output current, and output voltage.

5.1 Read Output Current

Read I_{OUT} returns the output current in amperes. The data is in PMBus DIRECT format with R = -1, m and b, as defined below.

Equation 4

$$\text{Read } I_{OUT} = \frac{(\text{Reg\_8Ch<bit 15-0>} \bullet 10^{-R} - b)}{m} + a \bullet (T_J - 50)(Amps)$$

where:

$m = 153 + 5.61 \bullet D$

$b = 4976 - 131 \bullet D$

$D = \frac{V_{OUT}}{V_{IN}}$

a = 0.013

T_J = Junction temperature reading in °C

5.2 Read Temperature

Read Temp returns the junction temperature in °C. The data is in PMBus DIRECT format with m = 21, b = 5887 and R = -1.

Equation 5

$$\text{Read Temp} = \frac{(\text{Reg\_8Dh<bit 15-0>} \bullet 10^{-R} - b)}{m}(^{\circ}C)$$

5.3 Read Output Voltage

Read V_{OUT} returns the output voltage in volts. The data is in PMBus LINEAR format, with N = -9.

Equation 6

$$\text{Read } V_{OUT} = \text{Reg\_8Bh<bit 9-0>} \bullet 2^{N} \text{ (volts)}$$

5.4 Read Input Voltage

Read V_{IN} returns the input voltage in volts. The data is in PMBus DIRECT format with m = 3609, b = 0, R = -2.

Equation 7

$$\text{Read } V_{IN} = \frac{(\text{Reg\_88h<bit 15-0>} \bullet 10^{-R} - b)}{m} \text{ (volts)}$$

6.0 ARA Read/PMBus Alert

The MAX20710 supports alert response address (ARA) protocol as described in the SMBus 2.0 specification. Refer to SMBus 2.0 Specification Appendix A for more details.

6.1 PMBus Alert Pin

MAX20710 SMALERT pin supports the SMBALERT# signal described in the SMBus 2.0 specification. The fault conditions that will assert the alert line low are as follows.

- Any bits different from 0 and not masked by SMBALERT_MASK command pull low SMALERT pin in STATUS_CML.
- Any bits different from 0 and not masked by SMBALERT_MASK command pull low SMALERT pin in STATUS_VOUT.
- Any bits different from 0 and not masked by SMBALERT_MASK command pull low SMALERT pin in STATUS_IOUT.
- Any bits different from 0 and not masked by SMBALERT_MASK command pull low SMALERT pin in STATUS_TEMPERATURE.
- Any bits different from 0 and not masked by SMBALERT_MASK command pull low SMALERT pin in STATUS_MFR_SPECIFIC.
- Any bits different from 0 and not masked by SMBALERT_MASK command pull low SMALERT pin in STATUS_Input.
- PMBus message lasts longer than expected.

SMBALERT_MASK register is used to prevent a warning or fault condition from asserting the SMALERT pin. The command format (write word) used to block a status bit or bits from causing the SMALERT pin to be asserted is shown in Table 21. The bits in the mask byte align with the bits in the corresponding status register.

Table 21. SMBALERT_MASK Command Packet Format

1	7	1	1	8	1	8	1	8	1	1
S	PMBus Address	W	ACK	SMBALERT_MASK Command Code	ACK	Status_x Command Code	ACK	Mask Byte	ACK	P

The two ways to release the SMALERT pin are:

- CLEAR_FAULTS command
- ARA (refer to SMBus Specification 2.0)

APPLICATION NOTE 6140

MAX20710 PMBus Application Note

APPLICATION NOTE 6140 REVISION HISTORY

REVISION	DESCRIPTION	DATE
0	Initial Data Sheet	7/16

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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