The Design of the Inverting Buck/Boost Converter Topology

by Enrico Reineri

ABSTRACT

The inverting buck/boost converter topology is an often mysterious and misunderstood category of DC-DC converters. This document attempts to remove any misconception around the circuit by providing a step-by-step design procedure with equations, schematics, simulations, and considerations to ensure that the circuit is properly designed.

INTRODUCTION

The inverting buck/boost topology is useful for converting a positive input to a negative output. It is an alternative to the Ćuk topology when a compact solution is desired. The inverting buck/boost topology converts an input voltage to either a lower voltage (buck mode) or higher voltage (boost mode). However, unlike the Ćuk topology, the inverting buck/boost converter produces more noise at the output. Therefore, it generates more electromagnetic content. The inverting buck/boost converter is often derived from the buck converter by swapping output and ground references. Therefore, it is often improperly labeled inverting as if it is the only topology that can invert an input or inverting buck as if it is the only topology that can invert and step down to a negative output. The reality is that the inverting buck/boost topology, like the Ćuk topology, can invert but it can also step down or step up a voltage. The inverting buck/boost converter can be asynchronous if a diode is used and synchronous if the diode is replaced with a metal-oxide semiconductor field-effect transistor (MOSFET), which provides higher efficiency. The inverting buck/boost converter topology is generally used for applications that require up to 150 W.

OPERATION

The operation of the inverting buck/boost converter is shown in Figure 1 and in Figure 2.

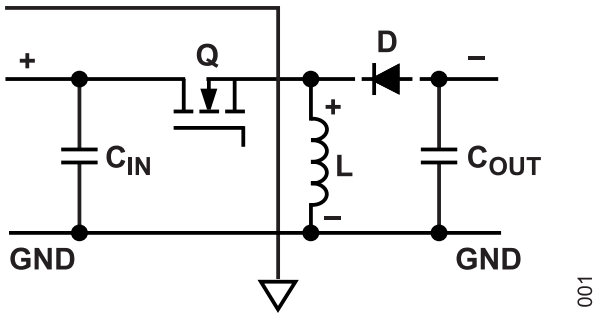


Figure 1. On-Time State

During the on-time state, the MOSFET is on and the diode is off. The inductor is energized by the input.

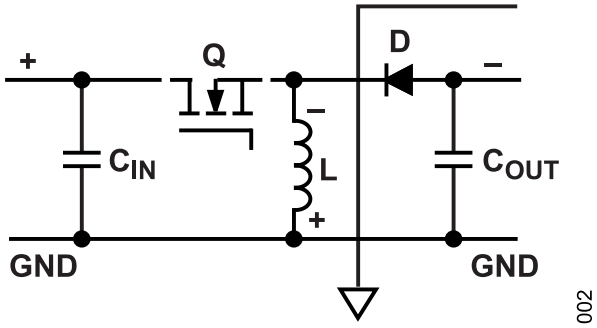


Figure 2. Off-Time State

During the off-time state, the MOSFET is off and the diode is on. The inductor is de-energized by the load at the output.

The operation for Figure 1 and Figure 2 uses a diode, which makes the circuit asynchronous. The diode can be replaced with a MOSFET, which makes the circuit synchronous.

TABLE OF CONTENTS

REVISION HISTORY

5/2024—Revision 0: Initial Version

DESIGN APPROACH

To properly design the inverting buck/boost converter, it is important to consider the operation at each extreme of the input voltage: high line (highest input voltage) and low line (lowest input voltage). Inductance and output capacitance are functions of several parameters. This document describes the conditions that yield the minimum inductance and minimum output capacitance to satisfy the specifications for a target application. The process is sequential. Therefore, designing across the input voltage range allows the engineer to take into account all the critical parameters that allow proper operation.

DESIGN SPECIFICATIONS

The specifications for the inverting buck/boost converter are as follows:

$V_{IN(MAX)}$ = 72 V

$V_{IN(MIN)}$ = 36 V

V_{OUT} = −48 V

I_{OUT} = 2 A

f_S = 350 kHz

ΔI_{OUT_TRA}(25%) = 500 mA

ΔV_{OUT_SS}(1%) = 480 mV

ΔV_{OUT_TRA}(1%) = 480 mV

DESIGN OBJECTIVES

The objective of this document is to provide guidance through an entire design cycle. For example, consider the targets listed in the Design Specifications section for a specific application, such as a telecommunication platform, where −48 V outputs are not uncommon. It is assumed that a high voltage, high power, and high efficiency solution is required. Because the output of the inverting buck/boost converter is −48 V, the converter is in buck mode when the input voltage is between +72 V and +48 V and it is in boost mode when the input voltage is between +36 V and +48 V. Both buck and boost modes are presented and repetition is intentional for additional clarity. Some numbers are rounded up or down.

BUCK MODE DESIGN PROCEDURE

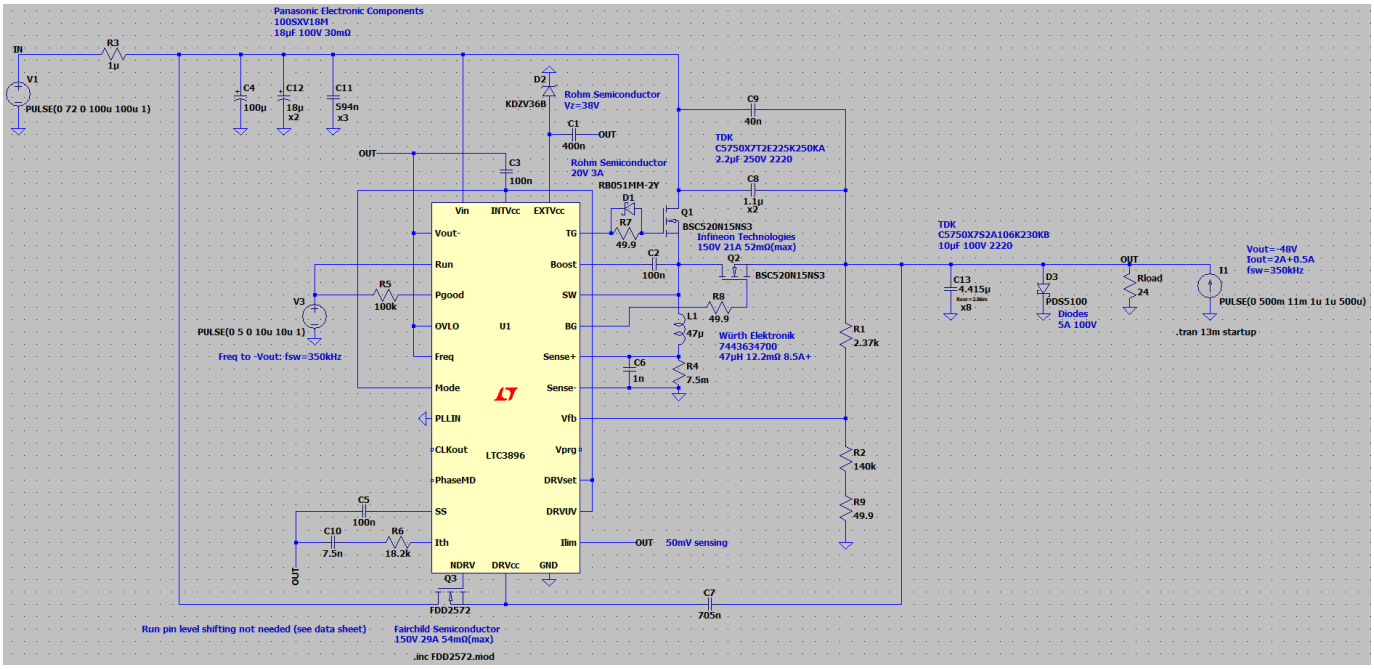


Figure 3. LTC3896 Inverting Buck/Boost Converter in Buck Mode (+72 V to −48 V Conversion)

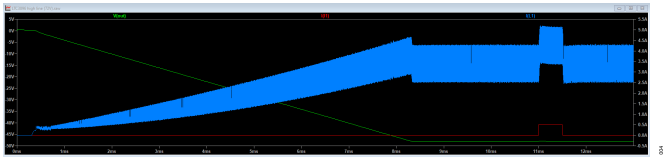


Figure 4. Waveforms at Startup (V_{IN} = 72 V)

The following example uses the LTC3896 controller IC and shows continuous conduction mode (CCM) operation in buck mode, which is the condition when the output voltage is lower than the input voltage. Figure 3 shows the circuit and Figure 4 shows the startup at high line.

The output power is calculated as follows:

$$P_{OUT} = |V_{OUT}| \times I_{OUT} = |-48\ \text{V}| \times 2\ \text{A} = 96\ \text{W} \quad (1)$$

The current through the inductor is the sum of the input current through the top MOSFET and the output current through the bottom MOSFET. Unlike the buck topology, which is rated by the output current, the inverting buck/boost topology is rated by the peak current through the MOSFET in an asynchronous converter or the top MOSFET in the synchronous counterpart.

The average input current is the average current through the top MOSFET.

$$I_{IN(MIN)} = \frac{P_{OUT}}{V_{IN(MAX)} \times \eta} = \frac{96\ \text{W}}{72\ \text{V} \times 0.95} = 1.404\ \text{A} \quad (2)$$

where η is the estimated efficiency in buck mode.

The average current through the top MOSFET during the on-time state is equal to the average current through the inductor and the average current through the bottom MOSFET during the off-time state.

$$I_{SW(AVE)} = I_{Q1(AVE)[ON]} = I_{L(AVE)} = I_{Q2(AVE)[OFF]} = I_{IN(MIN)} + I_{OUT} = 1.404\ \text{A} + 2\ \text{A} = 3.404\ \text{A} \quad (3)$$

The maximum current ripple through the inductor is calculated as follows:

$$\Delta I_{L(MAX)} = \Delta I_L(\%) \times I_{L(AVE)} = 0.55 \times 3.404\ \text{A} = 1.872\ \text{A} \quad (4)$$

where 0.55 is equivalent to a 55% inductor current ripple. This current swing is a function of the average current through the inductor and, depending on current levels for the application and inductor saturation currents, it typically ranges between 40% and 80%.

The top MOSFET used in the circuit is an Infineon Technologies BSC520N15NS3, 150 V, 21 A transistor which has a maximum $R_{DS(ON)}$ of 52 mΩ. An average of 3.404 A flows through it during the on-time state. Therefore, the voltage drop across the device is calculated as follows:

$$V_{Q1} = I_{L(AVE)} \times R_{DS(ON)} = 3.404\ \text{A} \times 52\ \text{mΩ} = 177\ \text{mV} \quad (5)$$

$$V_{IN(MAX)} - V_{Q1} = 72\ \text{V} - 177\ \text{mV} = 71.823\ \text{V} \quad (6)$$

The minimum duty cycle is as follows:

$$D_{MIN} = \frac{|V_{OUT}| + V_{Q2}}{|V_{OUT}| + V_{Q2} + (V_{IN(MAX)} - V_{Q1})} = \frac{48\ \text{V} + 0.177\ \text{V}}{48\ \text{V} + 0.177\ \text{V} + 71.823\ \text{V}} = 0.401 \quad (7)$$

where V_{Q2} is the voltage drop across the bottom BSC520N15NS3 MOSFET with 3.404 A of current through it.

$$1 - D_{MIN} = 1 - 0.401 = 0.599 \quad (8)$$

The period is as follows:

$$T_S = \frac{1}{f_S} = \frac{1}{350\ \text{kHz}} = 2.857\ \mu\text{s} \quad (9)$$

On-time and off-time are calculated as follows:

$$t_{ON(MIN)} = D_{MIN} \times T_S = 0.401 \times 2.857\ \mu\text{s} = 1.147\ \mu\text{s} \quad (10)$$

$$t_{OFF(MAX)} = \left(1 - D_{MIN}\right) \times T_S = 0.599 \times 2.857\ \mu\text{s} = 1.710\ \mu\text{s} \quad (11)$$

The minimum inductance can be calculated at high line, which is when the voltage across the top MOSFET is largest, the duty cycle is smallest and the on-time is smallest.

$$L \geq \frac{\left(V_{IN(MAX)} - V_{Q1}\right) \times D_{MIN}}{f_S \times \Delta I_{L(MAX)}} = \frac{71.823\ \text{V} \times 0.401}{350\ \text{kHz} \times 1.872\ \text{A}} = 44\ \mu\text{H} \rightarrow 47\ \mu\text{H} \quad (12)$$

A Würth Elektronik 7443634700, 47 µH, 12.2 mΩ inductor is selected.

The load resistance is calculated as follows:

$$R_L = \frac{V_{OUT}}{I_{OUT}} = \frac{|-48\ \text{V}|}{2\ \text{A}} = 24\ \Omega \quad (13)$$

The minimum output capacitance for steady state at high line is calculated as follows:

$$C_{OUT} \geq \frac{|V_{OUT}| \times t_{ON(MIN)}}{R_L \times \Delta V_{OUT_{SS}}} = \frac{48\ \text{V} \times 1.147\ \mu\text{s}}{24\ \Omega \times 480\ \text{mV}} = 4.779\ \mu\text{F} \quad (14)$$

However, to compensate for any sudden increase or decrease of load current at the output, additional capacitance is needed.

The inverting buck/boost converter has a unique feature called the right half plane zero (RHPZ). It is part of its transfer function and it limits the bandwidth of the converter. Its lower frequency occurs at low line and maximum load, which results in the largest duty cycle and the smallest load resistance. However, when the converter operates in buck mode with the highest input voltage (smallest duty cycle), the RHPZ moves to a higher frequency and it is located at:

$$f_{RHPZ} = \frac{R_L \times (1 - D_{MIN})^2}{2 \times \pi \times L \times D_{MIN}} = \frac{24\ \Omega \times 0.599^2}{2 \times \pi \times 47\ \mu\text{H} \times 0.401} = 72.7\ \text{kHz} \quad (15)$$

To ensure the stability of the inverting buck/boost converter, it is recommended to reduce its bandwidth to 25% to 33% of the RHPZ location.

$$f_c = \frac{1}{4} \times f_{RHPZ} = \frac{1}{4} \times 72.7\ \text{kHz} = 18.1\ \text{kHz} \quad (16)$$

The minimum output capacitance for a 25% load transient and 1% overshoot/undershoot is calculated with as follows:

$$C_{OUT} \geq \frac{\Delta I_{OUT_{TRA}}}{2 \times \pi \times f_C \times \Delta V_{OUT_{TRA}}} = \frac{500\ \text{mA}}{2 \times \pi \times 18.1\ \text{kHz} \times 480\ \text{mV}} = 9.2\ \mu\text{F} \rightarrow 8 \times 10\ \mu\text{F (nominal)} \rightarrow 8 \times 4.415\ \mu\text{F (effective)} \quad (17)$$

Eight TDK C5750X7S2A106K230KB, 10 µF, 100 V, 2220 ceramic capacitors, which derate to 4.415 µF at 48 V DC, are used in parallel at the output to reduce the impedance. Unfortunately, due to the output being −48 V, high-voltage capacitors must be selected. In addition, the capacitors must provide a sufficient amount of capacitance under bias. Therefore, eight relatively large ceramic capacitors are used (2220). This choice is a tradeoff between solution size and output ripple voltage. Using a hybrid solution, such as electrolytic and ceramic capacitors, is also an option and a single electrolytic capacitor in combination with a single ceramic capacitor can be used. However, because electrolytic capacitors feature a relatively high equivalent series resistance (ESR) and equivalent series inductance (ESL), the hybrid option increases the output ripple voltage at the switching frequency in the steady state.

The maximum ripple current through the inductor, shown in Figure 5, is calculated as follows:

$$\Delta I_{L(MAX)} = \frac{V_L \times \Delta t}{L} = \frac{\left(|V_{OUT}| + V_{Q2}\right) \times t_{OFF(MAX)}}{L} = \frac{(48\ \text{V} + 0.177\ \text{V}) \times 1.710\ \mu\text{s}}{47\ \mu\text{H}} = 1.753\ \text{A} \quad (18)$$

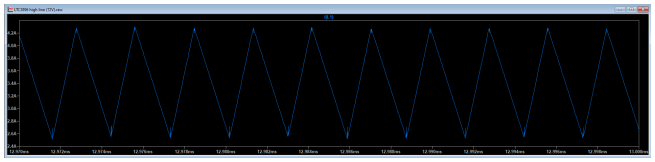


Figure 5. Inductor Ripple Current (V_{IN} = 72 V)

The current through the inductor is the sum of the input current through the top MOSFET and the output current through the bottom MOSFET.

The peak current through the top MOSFET, inductor, and bottom MOSFET is calculated by the following:

$$I_{SW(PEAK)} = I_{IN(MIN)} + I_{OUT} + \frac{1}{2}\Delta I_{L(MAX)} = \frac{P_{OUT}}{V_{IN(MAX)} \times \eta} + I_{OUT} + \frac{1}{2} \times \Delta I_{L(MAX)} = \frac{96\ \text{W}}{72\ \text{V} \times 0.95} + 2\ \text{A} + \frac{1}{2} \times 1.753\ \text{A} = 4.280\ \text{A} \quad (19)$$

The current through the top MOSFET has a trapezoidal shape and its RMS value is calculated by the following:

$$I_{Q1(MAX)[RMS]} = \sqrt{\left(I_{SW(AVE)}^2 + \frac{\Delta I_{L(MAX)}^2}{12}\right) \times D_{MIN}} = \sqrt{\left((3.404\ \text{A})^2 + \frac{(1.753\ \text{A})^2}{12}\right) \times 0.401} = 2.180\ \text{A} \quad (20)$$

The RMS current for the bottom MOSFET can be calculated in the same way using Equation 20 but replacing D_{MIN} with 1 − D_{MIN}.

The RMS current is the root mean square of the input DC and AC currents multiplied by the duty cycle.

The output ripple voltage is a combination of two terms.

$$\Delta V_{OUT} = \Delta V_C + \Delta V_{ESR} \quad (21)$$

The first term is produced by the capacitive component of the output capacitor.

$$\Delta V_{C(MAX)} = \frac{1}{C_{OUT}} \times I_{OUT} \times t_{ON(MIN)} = \frac{1}{35.32\ \mu F} \times 2\ A \times 1.147\ \mu s = 65.0\ mV \quad (22)$$

The second term is produced by the resistive component of the output capacitor, the ESR.

$$\Delta V_{ESR} = \left(\frac{I_{OUT}}{1 - D_{MIN}} + \frac{1}{2} \times \Delta I_{L(MAX)}\right) \times ESR = \left(\frac{2\ A}{0.599} + \frac{1}{2} \times 1.753\ A\right) \times 358\ \mu\Omega = 1.5\ mV \quad (23)$$

where 358 µΩ is the combined ESR at the switching frequency of the output capacitors.

Combining the terms gives the total output ripple voltage, which is shown in Figure 6.

$$\Delta V_{OUT(MAX)} = \Delta V_{C(MAX)} + \Delta V_{ESR(MAX)} = 65.0\ mV + 1.5\ mV = 66.5\ mV \quad (24)$$

Either the first term or the second term can dominate over the other.

If ΔV_C dominates over ΔV_{ESR}, the output looks triangular.

If ΔV_{ESR} dominates over ΔV_C, the output looks trapezoidal.

In this case, ΔV_C is larger than ΔV_{ESR}. Therefore, the output looks triangular.

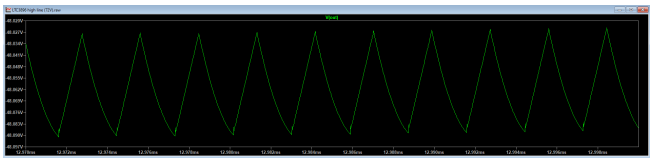


Figure 6. Output Ripple Voltage (V_{IN} = 72 V)

The RMS output ripple current through the capacitor has a trapezoidal shape.

$$I_{COUT[RMS]} = I_{OUT} \times \sqrt{\frac{D_{MIN}}{1 - D_{MIN}}} = 2\ A \times \sqrt{\frac{0.401}{0.599}} = 1.638\ A \quad (25)$$

Therefore, a set of eight capacitors with a combined RMS current rating of at least 1.638 A must be selected.

The overshoot/undershoot at high line is shown in Figure 7 and it is estimated by the following:

$$\Delta V_{OUT_{TRA}} = \frac{\Delta I_{OUT_{TRA}}}{2 \times \pi \times f_C \times C_{OUT}} = \frac{500\ mA}{2 \times \pi \times 18.1\ kHz \times 35.32\ \mu F} = 124\ mV \quad (26)$$

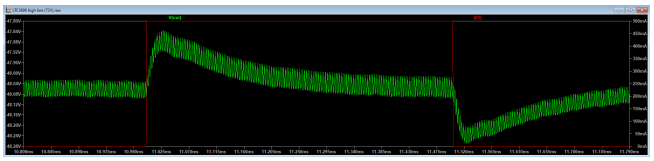


Figure 7. Load Regulation for 2 A → 2.5 A →2 A (V_{IN} = 72 V)

BOOST MODE DESIGN PROCEDURE

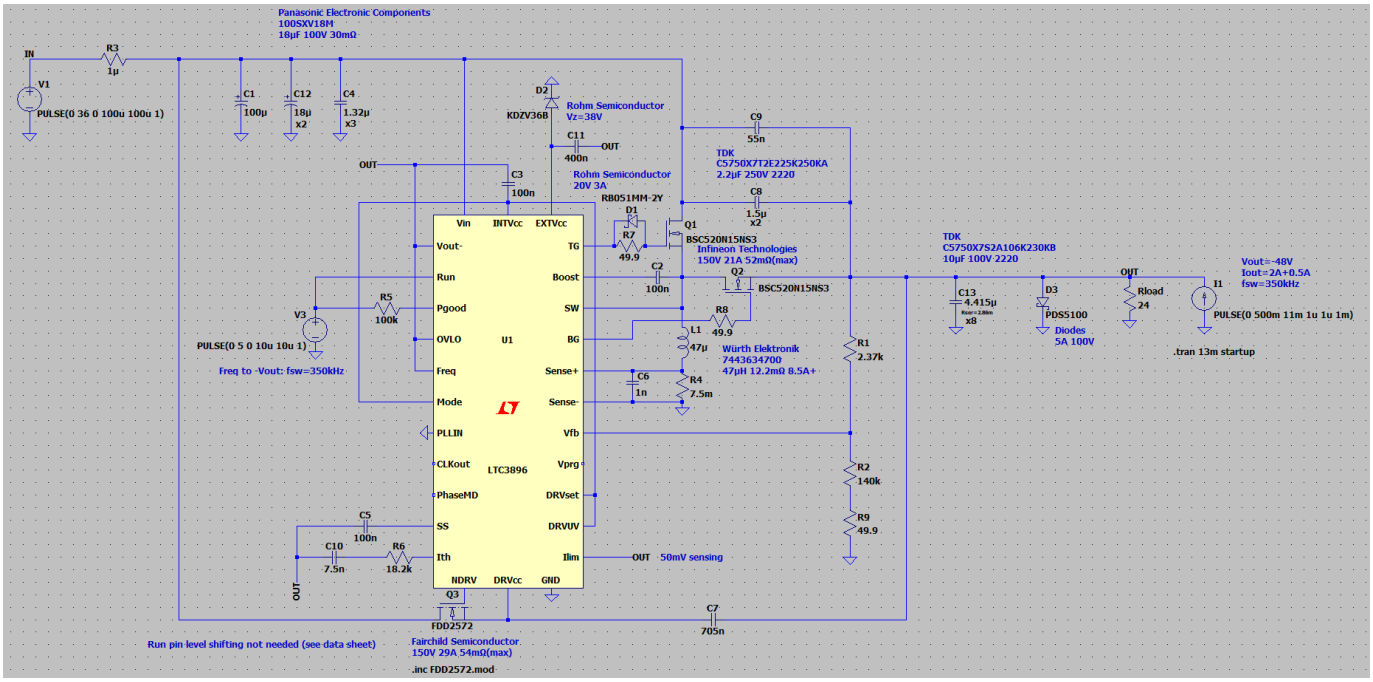


Figure 8. LTC3896 Inverting Buck/Boost Converter in Boost Mode (+36 V to −48 V Conversion)

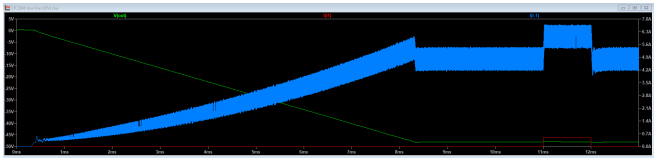


Figure 9. Waveforms at Startup (V_{IN} = 36 V)

The following example uses the LTC3896 controller IC and shows CCM operation in boost mode which is the condition when the output voltage is higher than the input voltage. Figure 8 shows the circuit and Figure 9 shows the startup at low line.

The output power is calculated as follows:

$$P_{OUT} = |V_{OUT}| \times I_{OUT} = |-48\text{ V}| \times 2\text{ A} = 96\text{ W} \quad (27)$$

The current through the inductor is the sum of the input current through the top MOSFET and the output current through the bottom MOSFET.

The average input current is the average current through the top MOSFET.

$$I_{IN(MAX)} = \frac{P_{OUT}}{V \times \eta} = \frac{96\text{ W}}{36\text{ V} \times 0.95} = 2.807\text{ A} \quad (28)$$

where η is the estimated efficiency in boost mode.

The average current through the top MOSFET during the on-time state is equal to the average current through the inductor and the average current through the bottom MOSFET during the off-time state.

$$I_{SW(AVE)} = I_{Q1(AVE)}[ON] = I_{L(AVE)} = I_{Q2(AVE)}[OFF] = I_{IN(MAX)} + I_{OUT} = 2.807\text{ A} + 2\text{ A} = 4.807\text{ A} \quad (29)$$

The maximum current ripple through the inductor is calculated as follows:

$$\Delta I_{L(MAX)} = \Delta I_L(\%) \times I_{L(AVE)} = 0.55 \times 4.807\text{ A} = 2.644\text{ A} \quad (30)$$

The top MOSFET used in the circuit is an Infineon Technologies BSC520N15NS3, 150 V, 21 A transistor which has a maximum $R_{DS(ON)}$ of 52 mΩ. An average of 4.807 A flows through it during the on-time. Therefore, the voltage drop across the device is as follows:

$$V_{Q1} = I_{L(AVE)} \times R_{DS(ON)} = 4.807\text{ A} \times 52\text{ mΩ} = 250\text{ mV} \quad (31)$$

$$V_{IN(MIN)} - V_{Q1} = 36\text{ V} - 250\text{ mV} = 35.750\text{ V} \quad (32)$$

The maximum duty cycle is as follows:

$$D_{MAX} = \frac{|V_{OUT}| + V_{Q2}}{|V_{OUT}| + V_{Q2} + (V_{IN(MIN)} - V_{Q1})} = \frac{48\text{ V} + 0.250\text{ V}}{48\text{ V} + 0.250\text{ V} + 35.750\text{ V}} = 0.574 \quad (33)$$

where V_{Q2} is the voltage drop across the bottom BSC520N15NS3 MOSFET with 4.807 A of current through it.

$$1 - D_{MAX} = 1 - 0.574 = 0.426 \quad (34)$$

The period is as follows:

$$T_S = \frac{1}{f_S} = \frac{1}{350\text{ kHz}} = 2.857\text{ µs} \quad (35)$$

On-time and off-time are as follows:

$$t_{ON(MAX)} = D_{MAX} \times T_S = 0.574 \times 2.857\ \mu s = 1.641\ \mu s \quad (36)$$

$$t_{OFF(MIN)} = \left(1 - D_{MAX}\right) \times T_S = 0.426 \times 2.857\ \mu s = 1.216\ \mu s \quad (37)$$

The minimum inductance can be calculated at low line, which is when the voltage across the top MOSFET is smallest, the duty cycle is largest and the on-time is largest.

$$L \geq \frac{\left(V_{IN(MIN)} - V_{Q1}\right) \times D_{MAX}}{f_S \times \Delta I_{L(MAX)}} = \frac{35.750\ V \times 0.574}{350\ kHz \times 2.644\ A} = 22.2\ \mu H \rightarrow 47\ \mu H \quad (38)$$

A Würth Elektronik 7443634700, 47 µH, 12.2 mΩ inductor is imposed to satisfy the inductance requirement for the high line condition.

The load resistance is as follows:

$$R_L = \frac{V_{OUT}}{I_{OUT}} = \frac{|-48\ V|}{2\ A} = 24\ \Omega \quad (39)$$

The minimum output capacitance for steady state at low line is as follows:

$$C_{OUT} \geq \frac{|V_{OUT}| \times t_{ON(MAX)}}{R_L \times \Delta V_{OUT}} = \frac{48\ V \times 1.641\ \mu s}{24\ \Omega \times 480\ mV} = 6.838\ \mu F \quad (40)$$

However, to compensate for any sudden increase or decrease of load current at the output, additional capacitance is needed.

The inverting buck/boost converter features an RHPZ. It is part of its transfer function and it limits the bandwidth of the converter. Its lower frequency occurs at low line and maximum load, which results in the largest duty cycle and the smallest load resistance.

$$f_{RHPZ} = \frac{R_L \times (1 - D_{MAX})^2}{2 \times \pi \times L \times D_{MAX}} = \frac{24\ \Omega \times 0.426^2}{2 \times \pi \times 47\ \mu H \times 0.574} = 25.6\ kHz \quad (41)$$

To ensure the stability of the inverting buck/boost converter, it is recommended to reduce its bandwidth to 25% to 33% of the RHPZ location.

$$f_c = \frac{1}{4} \times f_{RHPZ} = \frac{1}{4} \times 25.6\ kHz = 6.4\ kHz \quad (42)$$

The minimum output capacitance for a 25% load transient and 1% overshoot/undershoot is given by the following:

$$C_{OUT} \geq \frac{\Delta I_{OUT_{TRA}}}{2 \times \pi \times f_c \times \Delta V_{OUT_{TRA}}} = \frac{500\ mA}{2 \times \pi \times 6.4\ kHz \times 480\ mV} = 26.0\ \mu F \rightarrow 8 \times 10\ \mu F\ (nominal) \rightarrow 8 \times 4.415\ \mu F\ (effective) \quad (43)$$

Eight TDK C5750X7S2A106K230KB, 10 µF, 100 V, 2220 ceramic capacitors, which derate to 4.415 µF at 48 V, are used at the output.

Therefore, an effective capacitance of 35.32 µF is selected to satisfy the low line condition.

The minimum ripple current through the inductor, shown in Figure 10, is given by the following:

$$\Delta I_{L(MIN)} = \frac{V_L \times \Delta t}{L} = \frac{\left(|V_{OUT}| + V_{Q2}\right) \times t_{OFF(MIN)}}{L} = \frac{(48\ V + 0.250\ V) \times 1.216\ \mu s}{47\ \mu H} = 1.248\ A \quad (44)$$

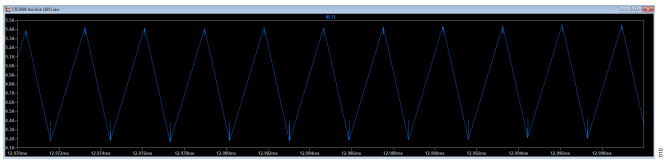


Figure 10. Inductor Ripple Current (V_{IN} = 36 V)

The current through the inductor is the sum of the input current through the top MOSFET and the output current through the bottom MOSFET.

The peak current through the top MOSFET, inductor, and bottom MOSFET is given by the following:

$$I_{SW(PEAK)} = I_{IN(MAX)} + I_{OUT} + \frac{1}{2} \times \Delta I_{L(MIN)} = \frac{P_{OUT}}{V_{IN(MIN)} \times \eta} + I_{OUT} + \frac{1}{2} \times \Delta I_{L(MIN)} = \frac{96\ W}{36\ V \times 0.95} + 2\ A + \frac{1}{2} \times 1.248\ A = 5.431\ A \quad (45)$$

The current through the top MOSFET has a trapezoidal shape and its RMS value is given by the following:

$$I_{Q1(MAX)[RMS]} = \sqrt{\left(I_{SW\ (AVE)}^2 + \frac{\Delta I_{L(MIN)}^2}{12}\right) \times D_{MAX}} = \sqrt{\left((4.807\ A)^2 + \frac{(1.248\ A)^2}{12}\right) \times 0.574} = 3.653\ A \quad (46)$$

The RMS current for the bottom MOSFET can be calculated in the same way by using Equation 46 but replacing D_{MAX} with 1 − D_{MAX}.

The RMS current is the root mean square of the input DC and AC currents multiplied by the duty cycle.

The output ripple voltage is a combination of two terms.

$$\Delta V_{OUT} = \Delta V_C + \Delta V_{ESR} \quad (47)$$

The first term is produced by the capacitive component of the output capacitor.

$$\Delta V_{C(MAX)} = \frac{1}{C_{OUT}} \times I_{OUT} \times t_{ON(MAX)} = \frac{1}{35.32\ \mu F} \times 2\ A \times 1.641\ \mu s = 92.9\ mV \quad (48)$$

The second term is produced by the resistive component of the output capacitor.

$$\Delta V_{ESR} = \left(\frac{I_{OUT}}{1 - D_{MAX}} + \frac{1}{2} \times \Delta I_{L(MIN)}\right) \times ESR$$
$$= \left(\frac{2\text{ A}}{0.426} + \frac{1}{2} \times 1.248\text{ A}\right) \times 358\ \mu\Omega = 1.9\text{ mV} \quad (49)$$

where 358 µΩ is the combined ESR at the switching frequency of the output capacitors.

Combining the terms gives the total output ripple voltage, which is shown in Figure 11.

$$\Delta V_{OUT(MAX)} = \Delta V_{C(MAX)} + \Delta V_{ESR(MAX)}$$
$$= 92.9\text{ mV} + 1.9\text{ mV} = 94.8\text{ mV} \quad (50)$$

Either the first term or the second term can dominate over the other.

If ΔV_C dominates over ΔV_{ESR}, the output looks triangular.

If ΔV_{ESR} dominates over ΔV_C, the output looks trapezoidal.

In this case, ΔV_C is larger than ΔV_{ESR}. Therefore, the output looks triangular.

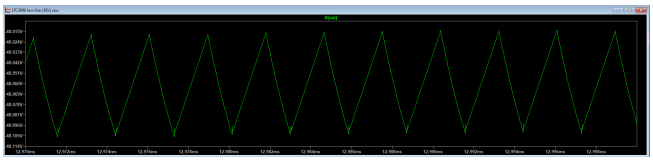


Figure 11. Output Ripple Voltage (V_{IN} = 36 V)

The RMS output ripple current through the capacitor has a trapezoidal shape.

$$I_{COUT[RMS]} = I_{OUT} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 2\text{ A} \times \sqrt{\frac{0.574}{0.426}}$$
$$= 2.323\text{ A} \quad (51)$$

Therefore, a set of eight capacitors with a combined RMS current rating of at least 2.323 A must be selected.

The overshoot/undershoot at low line is shown in Figure 12 and it is estimated by the following:

$$\Delta V_{OUT_{TRA}} = \frac{\Delta I_{OUT_{TRA}}}{2 \times \pi \times f_C \times C_{OUT}} = \frac{500\text{ mA}}{2 \times \pi \times 6.4\text{ kHz} \times 35.32\ \mu\text{F}}$$
$$= 352\text{ mV} \quad (52)$$

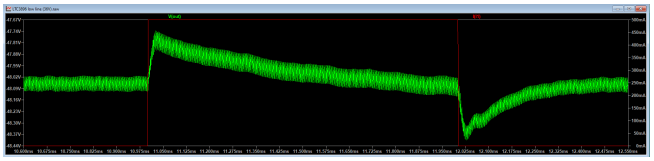


Figure 12. Load Regulation for 2 A → 2.5 A → 2 A (V_{IN} = 36 V)

LTPOWERCAD

If an LTpowerCAD model for an IC in the inverting buck/boost configuration is available, the software helps the designer to produce a design, and tuning of the circuit that meet the requirements listed in the Design Specifications section. Based on the desired crossover, the software suggests a resistor/capacitor combination used for the compensator to achieve an appropriate dynamic load regulation response. However, LTpowerCAD models are not always available. At the time of the writing of this document, the LTC3896 is supported in LTpowerCAD. Figure 13 and Figure 14 show an example for the LTC3896 design discussed in this document.

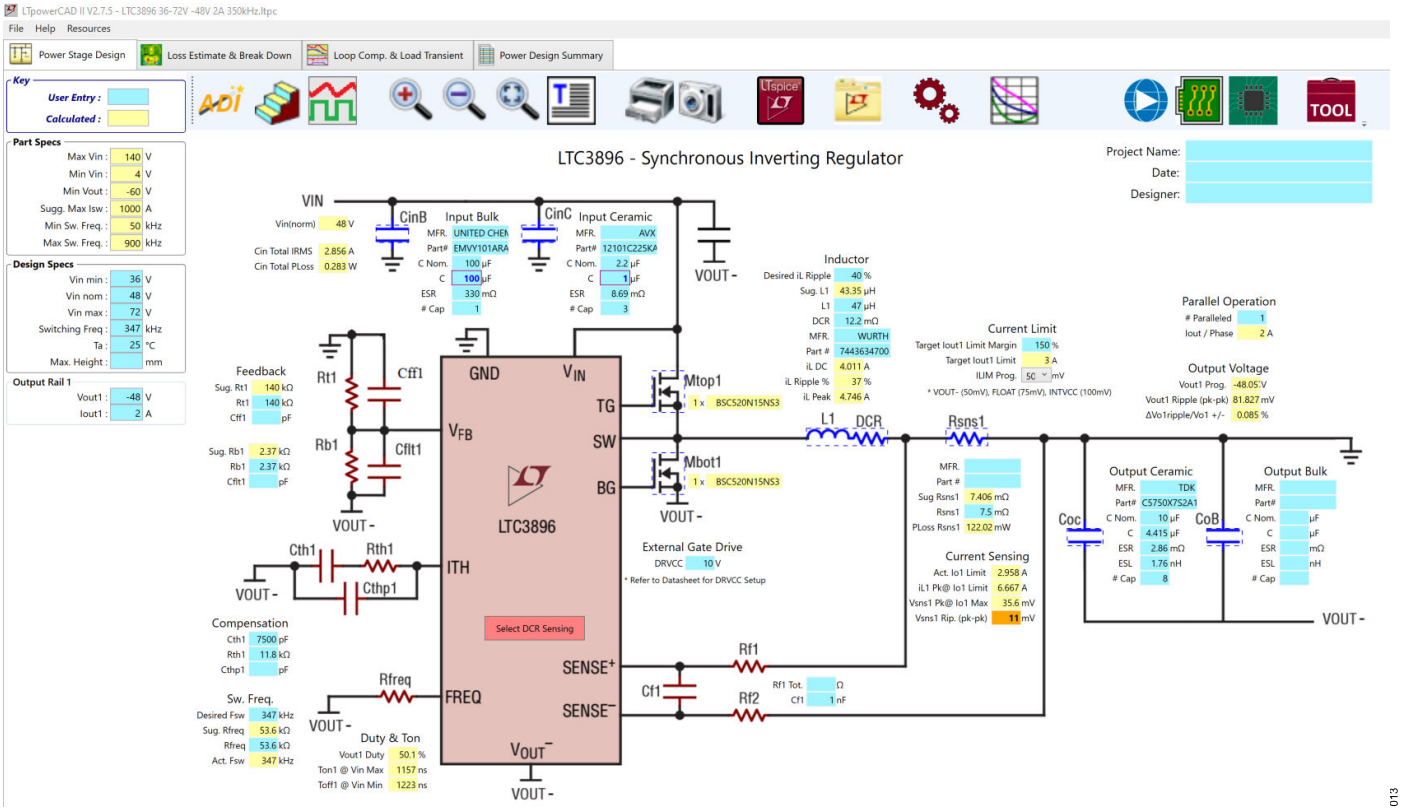


Figure 13. LTpowerCAD Setup for the LTC3896 (First Tab Features Design)

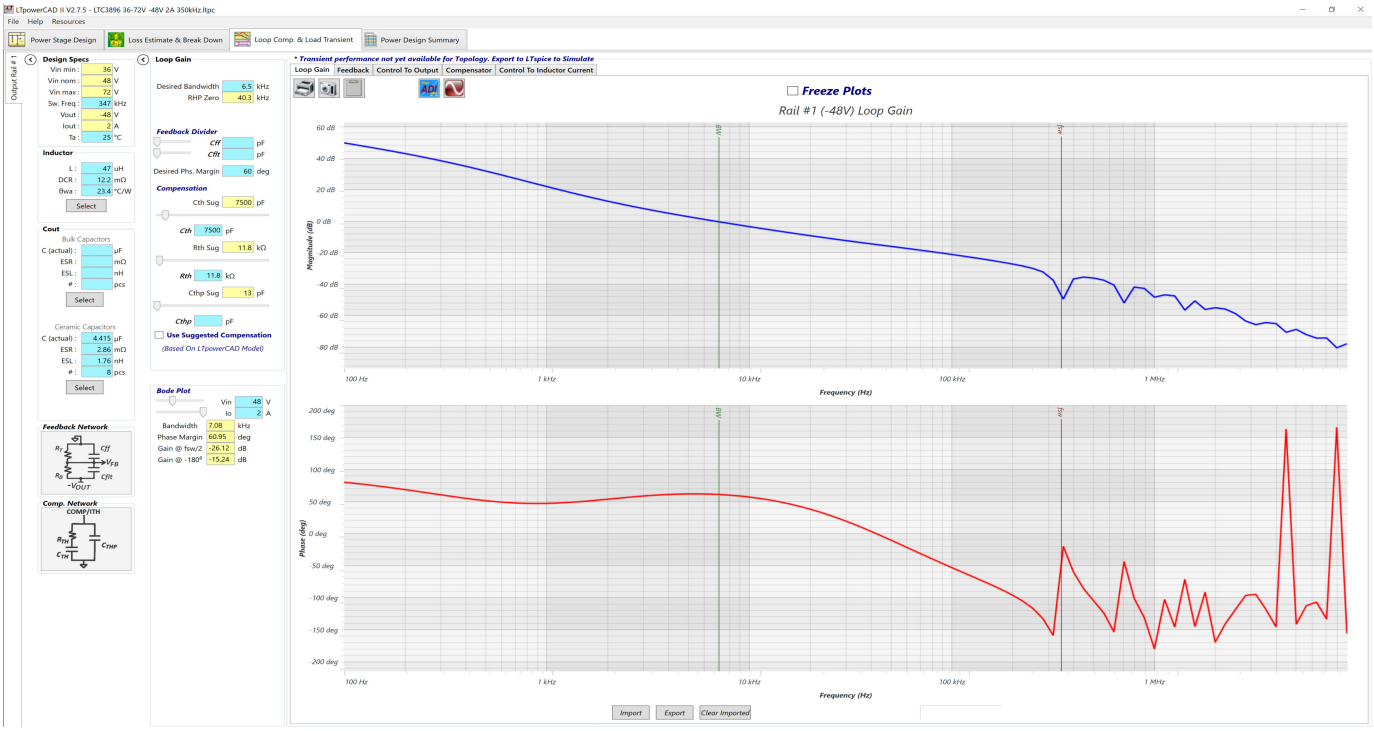


Figure 14. LTpowerCAD Setup for the LTC3896 (Third Tab Features Compensation)

LTSPICE

LTspice models are available for a majority of Analog Devices, Inc., switch-mode power supplies (SMPSs) and they are useful for a first approximation in the time and the frequency domains. Setting up the converter directly in LTspice can lead to recursive and time-consuming simulations. An LTspice simulation allows approximate bandwidth of the converter. A parametric sweep of the resistor/capacitor combination used for the compensator at specific input and output conditions can be performed to further tune the loop.

COMPENSATION

Unless internally compensated, most inverting buck/boost circuits require external compensation. This translates to a compensator that typically includes an operational transconductance amplifier (OTA), current-mode control (CMC) and Type II compensation. Whether through software or mathematics, the end goal of compensation is to select a resistor/capacitor pair which produces a zero that allows acceptable stability over the input voltage range.

If neither LTpowerCAD nor LTspice can be used, mathematics is the only option.

When it comes to compensation, the recommended approach is to calculate the lowest location of the RHPZ which occurs at low line.

$$f_{RHPZ} = \frac{R_L \times (1 - D_{MAX})^2}{2 \times \pi \times L \times D_{MAX}} = \frac{24\ \Omega \times 0.426^2}{2 \times \pi \times 47\ \mu H \times 0.574} = 25.6\ \text{kHz} \quad (53)$$

Next, assume a crossover around ¼ of the RHPZ.

$$f_c = \frac{1}{4} \times f_{RHPZ} = \frac{1}{4} \times 25.6\ \text{kHz} = 6.4\ \text{kHz} \quad (54)$$

Then, place a zero at 10% to 30% of the potential crossover.

$$f_{zEA(TARGET)} = 0.3 \times f_c = 0.3 \times 6.4\ \text{kHz} = 1.92\ \text{kHz} \quad (55)$$

Finally, select the values of R_C and C_C to insert the zero for the error amplifier.

$$f_{zEA(ACTUAL)} = \frac{1}{2 \times \pi \times R_C \times C_C} = \frac{1}{2 \times \pi \times 11.8\ \text{k}\Omega \times 7.5\ \text{nF}} = 1.798\ \text{kHz} \quad (56)$$

Although not always necessary, a pole can be placed to cancel the RHPZ of the zero produced by the output capacitors or to suppress noise.

The final choice for the location of the zero is made at low line where the bandwidth is smallest. A Bode plot can reveal whether the R_C and C_C combination is optimal. After testing the LTC3896 at the bench, the optimal choice of R_C is 18.2 kΩ and C_C remained 7.5 nF. Therefore, the zero at 1.166 kHz is near 18% of the initial estimated bandwidth (6.4 kHz) or near 20% of the actual bandwidth (5.779 kHz).

NOTES

The following is a series of observations that the designer must consider before building the inverting buck/boost circuit:

- The inductance is calculated at high line, whereas the capacitance at the output is calculated at low line.
- The maximum ripple current through the inductor occurs at high line, whereas the maximum ripple voltage at the output occurs at low line.
- The circuit is designed at each extreme of the input voltage range. To meet current and voltage ripple requirements, use a 47 µH inductor and 35.32 µF of effective capacitance at the output.
- It is customary to add a small high-frequency capacitor from the positive input to the negative output to compensate for the top MOSFET switching.
- If the design is asynchronous, the voltage drop across the bottom MOSFET, V_{Q2}, can be replaced by V_D, the equivalent drop across the diode for a specific average current.

TEST DATA

This section presents results for the LTC3896 inverting buck/boost circuit captured at the bench at low line and high line. R7, D1, and R8 are not added to the printed circuit board (PCB).

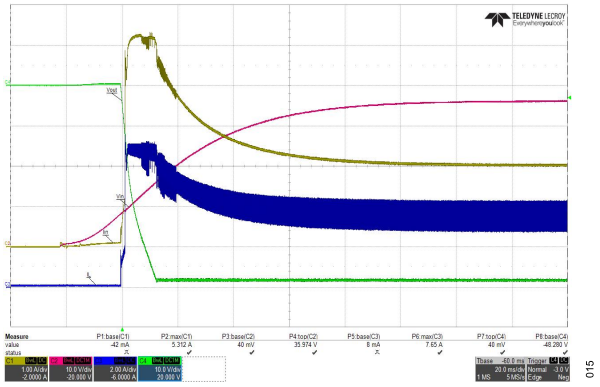


Figure 15. Startup, V_{IN} = +36 V, V_{OUT} = −48 V, I_{OUT} = 1.5 A

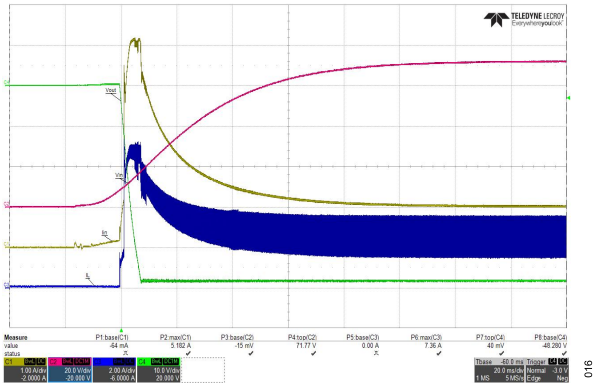


Figure 18. Startup, V_{IN} = +72 V, V_{OUT} = −48 V, I_{OUT} = 1.5 A

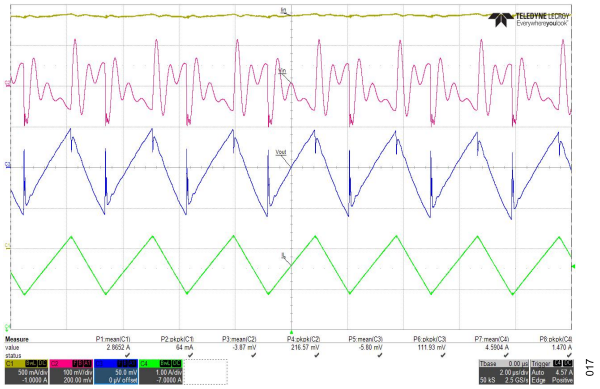


Figure 16. Steady State, V_{IN} = +36 V, V_{OUT} = −48 V, I_{OUT} = 2 A

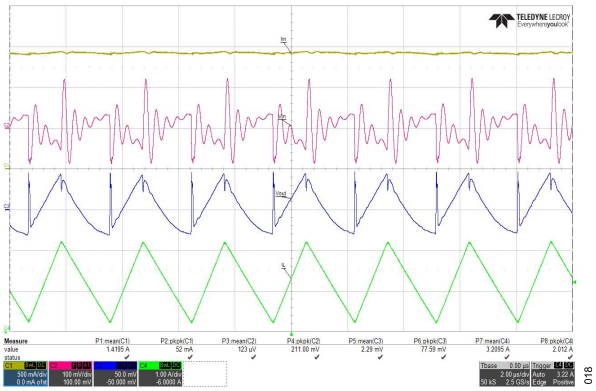


Figure 19. Steady State, V_{IN} = +72 V, V_{OUT} = −48 V, I_{OUT} = 2 A

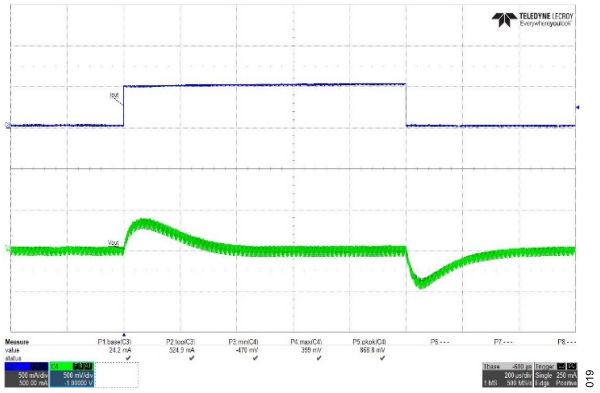


Figure 17. Load Regulation, V_{IN} = +36 V, V_{OUT} = −48 V, I_{OUT} = 2 A (DC) + 0.5 A (AC)

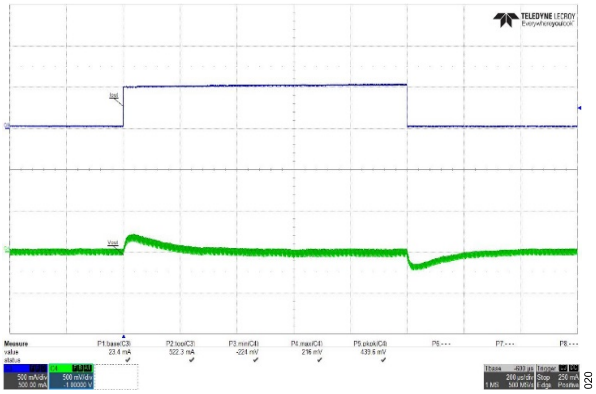
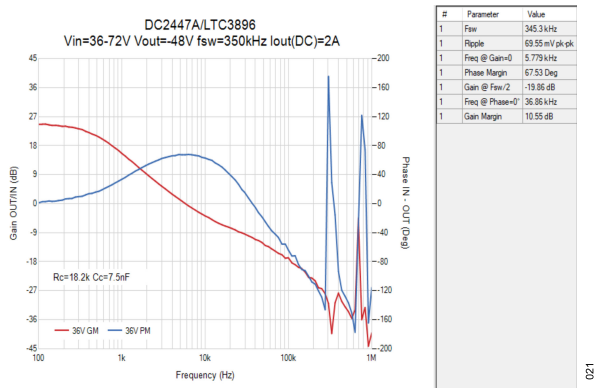


Figure 20. Load Regulation, V_{IN} = +72 V, V_{OUT} = −48 V, I_{OUT} = 2 A (DC) + 0.5 A (AC)



#	Parameter	Value
1	Fsw	345.3 kHz
1	Ripple	69.55 mV pk-pk
1	Freq @ Gain=0	5.779 kHz
1	Phase Margin	67.53 Deg
1	Gain @ Fsw/2	-19.86 dB
1	Freq @ Phase=0°	36.86 kHz
1	Gain Margin	10.55 dB

Figure 21. Loop Analysis, V_{IN} = +36 V, V_{OUT} = −48 V, I_{OUT} = 2 A

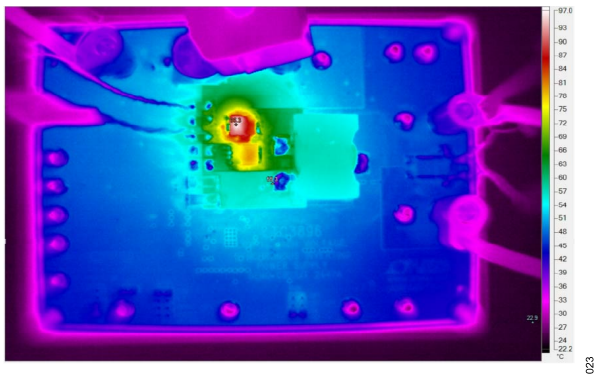
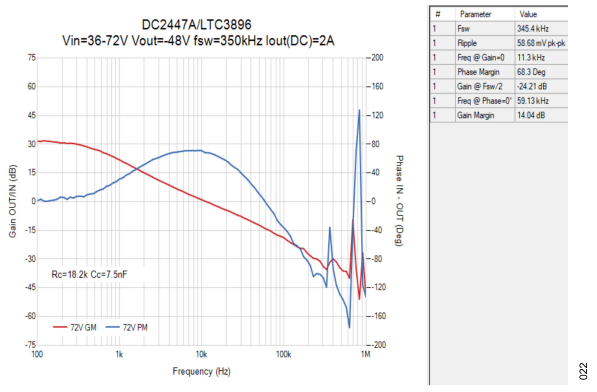


Figure 22. Thermal Analysis, V_{IN} = +36 V, V_{OUT} = −48 V, I_{OUT} = 2 A (No Air Flow)



#	Parameter	Value
1	Fsw	345.4 kHz
1	Ripple	58.68 mV pk-pk
1	Freq @ Gain=0	11.3 kHz
1	Phase Margin	68.3 Deg
1	Gain @ Fsw/2	-24.21 dB
1	Freq @ Phase=0°	59.13 kHz
1	Gain Margin	14.04 dB

Figure 23. Loop Analysis, V_{IN} = +72 V, V_{OUT} = −48 V, I_{OUT} = 2 A

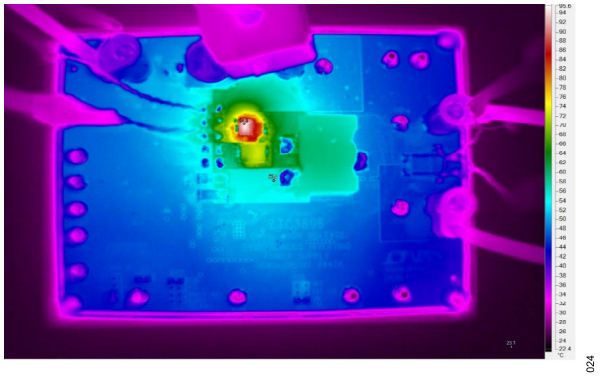


Figure 24. Thermal Analysis, V_{IN} = +72 V, V_{OUT} = −48 V, I_{OUT} = 2 A (No Air Flow)

CONSIDERATIONS

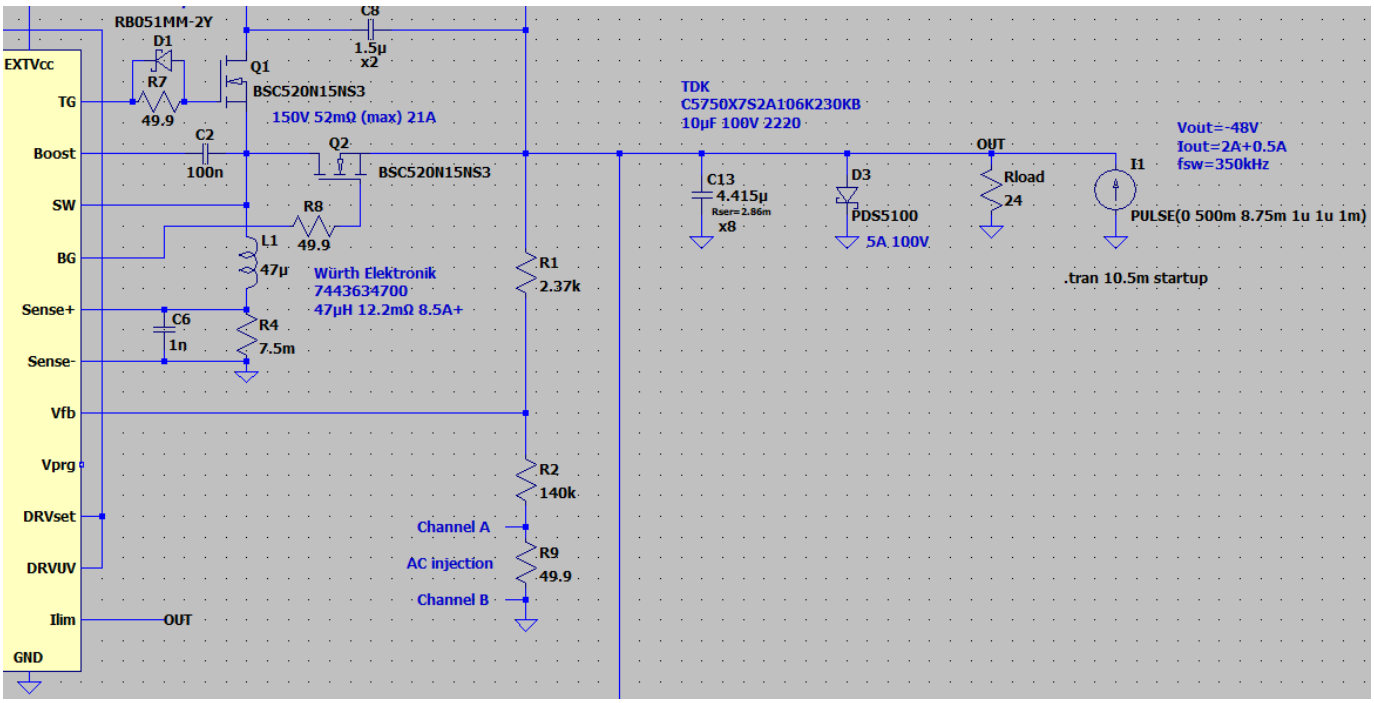


Figure 25. R9 Is Used for AC Injection to Generate Bode Plots

The following considerations must be made when designing an inverting buck/boost converter:

- Proper components selection. The voltage rating for the input/output capacitors must be appropriate to compensate for the bias applied to them. The voltage rating for the MOSFETs must be at least $V_{IN(MAX)} + |V_{OUT}|$. For an asynchronous design, the current rating for the diode must be at least $I_{SW(MAX)}$ and the voltage rating for the diode must be at least $V_{IN(MAX)} + |V_{OUT}|$ to allow operation in reverse mode. The inductor must be selected to avoid saturation and rated with a current above the peak inductor current.
- Enabling and level shifting. Unless the inverting buck/boost converter is always enabled, level shifting the enable pin is necessary and schemes can be introduced to address the issue. Varieties of options are available and a simple circuit with only one binary junction transistor (BJT) of the PNP type or one MOSFET of the positive channel (PMOS) type and three resistors accomplish the task. In some cases, level shifting is taken care of internally, such as in the case of the LTC3896 IC.
- Input capacitance. The RMS current that appears at the input of the converter and the RMS current through the top MOSFET have the same shape. They are also close in magnitude. The RMS current value calculated for the top MOSFET helps in the process of selecting the right combination of input capacitors to avoid excessive component stress. An LTspice simulation at maximum RMS current can reveal the actual RMS current spread across each capacitor as a function of its own impedance.
- Switching frequency. Choosing the optimal switching frequency helps to achieve the right balance between conduction losses and switching losses while trading off smaller or larger inductance with smaller or larger output capacitance.
- Compensation. The RHPZ reduces the bandwidth of the converter and compensation must be tuned at low line in boost mode. If a model of the converter is available in LTpowerCAD, the tuning process can be faster. If not, zeros and poles for the compensator are placed mathematically and load regulation can be verified in LTspice. If the output capacitors are entirely of the ceramic type, it is not necessary to add a high-frequency capacitor to cancel the zero produced by the output capacitors and its combined ESR.
- Loop analysis. Phase margin (PM) and gain margin (GM) must be verified across the line from high to nominal to low to maintain about 60° of PM and at least −6 dB of GM both at ½ the switching frequency and where the phase crosses 0° (LTpowerCAD, in the third tab for compensation of the LTC3896, tries to enforce −6 dB and −8 dB, respectively, when the GM figures are not met). Bode plots must be captured similarly to a buck converter, as shown in Figure 25, by using a 10 Ω to 49.9 Ω resistor. However, for the inverting buck/boost converter, because its output is negative, the AC injection into the feedback of the IC must be done across a resistor placed below R2 (near 0 V). The grounds of the input probes of the frequency response analyzer must float with respect to the input power supply and system ground. A cheater plug is sufficient to address the floating requirement. However, in this case, because the output is −48 V, a 10:1 attenuation is required to avoid damaging the inputs of the frequency response analyzers, which typically

do not tolerate more than about ±15 V. Therefore, the cheater plug can be avoided and high voltage differential probes with attenuation can be used.

- Capacitors between positive input and negative output. One or more capacitors can be placed across input and output to compensate for the high-frequency switching of the top MOSFET. Typically, the amount of capacitance is small. For dynamic load regulation, the capacitance can be increased in value which helps reducing the output voltage deviations (undershoot/overshoot) that occur when output loading changes abruptly. The value of capacitance must be a small fraction of the output capacitance. The voltage rating of the capacitors must be larger than $V_{IN(MAX)} + |V_{OUT}|$ and derating must be considered, especially for high-voltage applications.
- Output capacitance. Mathematically, increasing output capacitance reduces the output ripple voltage but it also reduces the loop bandwidth. Therefore, overloading an output rail with capacitance is not recommended because it can be counterproductive. For accurate calculations and results, DC bias must be considered. For more accurate results, AC bias can be introduced (AC bias is the output ripple voltage, which is added to the output regulated voltage). DC and AC biases add by superposition.
- Load regulation. The ability of the inverting buck/boost converter to regulate the output when a sudden load change occurs can be tested by appending a MOSFET at the output of the circuit. The drain must be connected to the system ground, the source must be connected to the negative output and the gate can be pulsed with a function generator that must float with respect to the input power supply and system ground. A cheater plug is sufficient to solve the floating requirement.
- Filtering. Additional output filtering may be necessary to clean up the electromagnetic content produced by switching at the output, which is coupled with the inevitable existence of ESL, especially when electrolytic capacitors are introduced and high voltages are required at the output. Additional LC filters influence the stability and operation of the switcher. Three-terminal capacitors are useful and powerful options. They provide low impedance at the switching frequency and suppress noise as well as reducing layout space. However, their voltage rating is relatively low so they are not suited for medium to high voltage applications. Tuning the switching frequency to match the lowest output impedance provides the optimal output ripple voltage solution.
- Output voltage clamping. If necessary, the output can be clamped by a Schottky diode which avoids excessive positive excursion between negative output and ground during startup. The diode must be placed between the nodes with the anode on the negative side and the cathode on the ground side.
- Power delivery limitations. Although the converter delivers full power at high line, in some cases, load current must be reduced to avoid excessive peak current at the switching node, which can damage the MOSFETs, especially for monolithic solutions. Controllers such as the LTC3896 are less constrained by current peaks because they allow flexibility in choosing MOSFETs that are external to the IC.
- Probing. It is important to probe signals such as switching nodes and output rails by using proper techniques. A pair of twisted wires terminating at a probe connector such as the Tektronix 131-0258-00 shown in Figure 26 can be mated with a passive voltage probe. The setup helps in reducing the amount of unwanted parasitic inductance that can magnify voltage spikes and ringing during transient events. This setup also reduces the amount of mechanical stress across components such as capacitors. Other alternatives that can be considered, if space allows, are shown in Figure 27 and include SubMiniature Version A (SMA) and U.FL connectors that can be mated with Bayonet Neill-Concelman (BNC) connectors directly at the oscilloscope inputs.

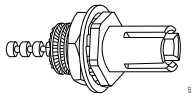


Figure 26. Tektronix 131-0258-00 Probe Connector

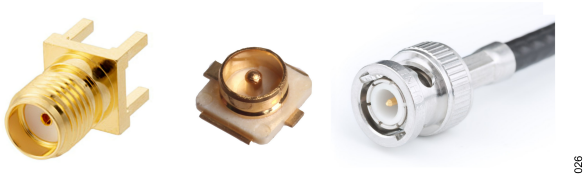


Figure 27. SMA, U.FL, and BNC Connectors

- Layout. Some PCBs host buck converters and can be reconfigured to work as inverting buck/boost converters. However, in some cases, reconfiguring the buck converter output to the ground plane and the ground plane to the negative output causes abnormal and erratic behavior at the bench, which is undesirable because it can be confusing and time-consuming. The best approach is to create a layout tailored specifically for the inverting buck/boost topology rather than adapting a PCB with a buck converter. This is for the best performance and low noise operation. Component placement must also be considered to reduce the amount of stray capacitance or inductance. The importance of a good layout must never be underestimated. Figure 28 shows the layout for the standard DC2447A demo board.

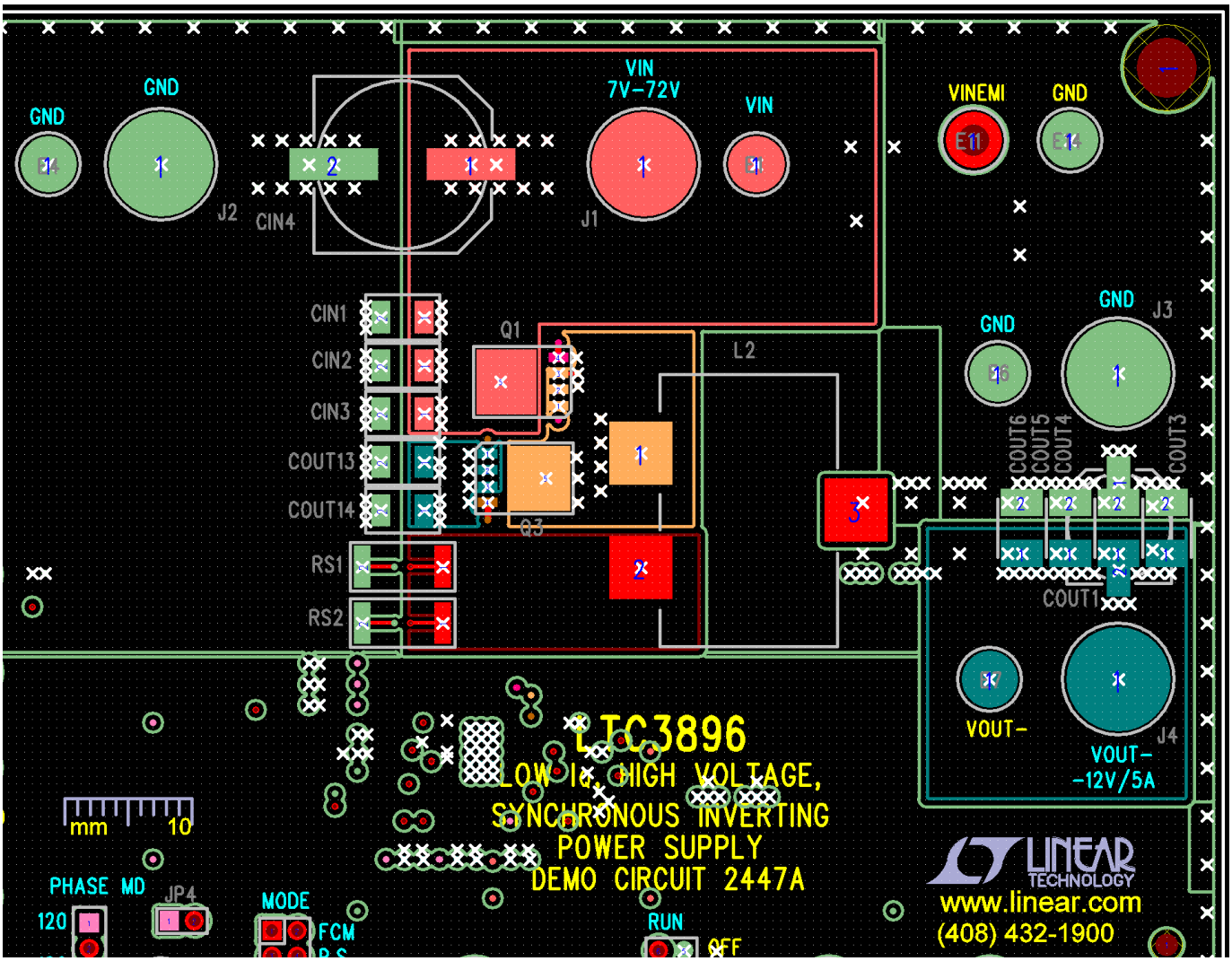


Figure 28. Layout for the DC2447A Demo Board that Hosts the LTC3896 Controller

SUMMARY

The inverting buck/boost topology is useful for generating negative voltage rails.

Although it can seem intimidating, the methodology outlined and the considerations listed in this document enable a designer to produce a circuit that can be simulated in software and tested at the bench. Software tools like LTpowerCAD and LTspice can help in designing and tuning the inverting buck/boost converter but the engineer can resort to pure mathematics to find a solution.

REFERENCES

Basso, Christophe. *Switch-Mode Power Supplies*. The McGraw-Hill Companies, Inc., 2008.

Kessler, Matthew. AN-1083 Application Note. *Designing an Inverting Buck Boost Using the ADP2300 and ADP2301 Switching Regulators*. Analog Devices, 2010.

Yang, Ricky. AN-1168 Application Note. *Designing an Inverting Power Supply Using the ADP2384/ADP2386 Synchronous Step-Down DC-to-DC Regulators*. Analog Devices, 2010.

Young, Sam. *Signal Level Shifting with µModule Regulator for Positive-to-Negative Inverting Applications*. Analog Devices, 2015.