True Bipolar Input, Fully Differential Output, ADC Driver Design

INTRODUCTION

Precision signal chains used in data acquisition and general-purpose test and measurement equipment must accommodate a wide range of input levels. The signal chain may need to offer high input impedance, support both gain and attenuation, and adjust the common-mode level to ensure that the signal falls within the appropriate input range for the ADC. The schematic in Figure 1 illustrates two-stage signal conditioning that scales and level shifts a differential, bipolar ±10 V signal to a fully differential ±4.096 V signal with a 2.048 V common-mode level required by the ADC. The design goal is to achieve this conditioning while not degrading the ADC noise and distortion performance. The ADC driver typically needs to have supply voltages that exceed the input range of the ADC, to allow for input and output swing voltage headroom. The driver usually must scale and shift the first stage output voltage to match the input voltage range of the ADC (or example, changing a true bipolar differential signal into a differential signal that swings from ground to V_{REF}).

The schematic in Figure 1 was created from LTspice®, a high performance SPICE III simulator, schematic capture, and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits. For additional information about the devices shown in Figure 1, see the LTC6373, ADA4945-1, and LTC2387-18 data sheets.

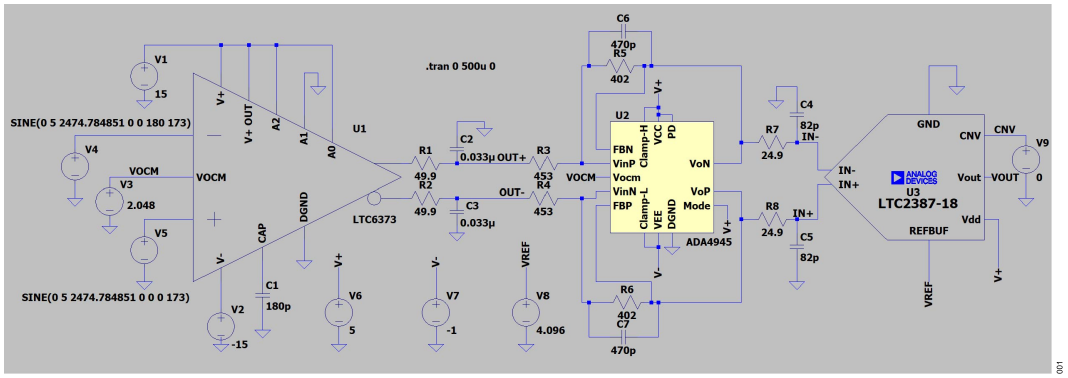

Figure 1. LTspice Schematic of the Bipolar Input, Fully Differential Output ADC Driver

TABLE OF CONTENTS

REVISION HISTORY

5/2023—Revision 0: Initial Version

KEY DESIGN SPECIFICATIONS

For a true bipolar input signal range of ±10 V, the key design specifications are listed in Table 1. For a differential, ±10 V peak sinewave, this circuit outputs a ±4.096 V differential output signal.

Table 1. Design Goal Key Specifications

Parameter	Value
Input Differential	±10 V
Output Differential	±4.096 V
Output Common-Mode Voltage (V_{OCM})	2.048 V
$+V_S/-V_s$ Supplies	±15 V, +5 V/−1 V
ADC Fully Differential	18 bits
Reference Voltage (V_{REF})	4.096 V
Input Frequency Range	0 kHz to 100 kHz
Total Harmonic Distortion (THD)	−117 dB
Single-to-Noise Ratio (SNR)	95.7 dB

DESIGN DESCRIPTION

The circuit is an ADC driver circuit that has a very high input impedance and can be tailored to drive a wide range of input voltages, both single-ended and differential. The output signal of the circuit is capable of driving ADCs with less than 30 ns acquisition times. The circuit accomplishes this while maintaining optimal noise and distortion performance. The circuit in Figure 1 is composed of the LTC6373 programmable gain-instrumentation amplifier as the input stage, the ADA4945-1 fully differential amplifier (FDA) as the second stage ADC driver, and the LTC2387-18, an 18-bit, 15 MSPS ADC. Additionally, there is a 100 kHz filter between the LTC6373 output and the ADA4945-1 input to reduce noise and a glitch suppression/noise reduction filter between the ADA4945-1 output and the LTC2387-18 input. The LTC6373 is configured as a differential-to-differential amplifier with a gain of 0.5 and output common-mode voltage of 2.048 V. The ADA4945-1 is configured as an attenuating differential-to-differential driver with a gain of 0.8. The ADA4945-1 has an output common-mode voltage of 2.048 V to be compatible with the LTC2387-18 input range. The LTC2387-18 has an input signal range of 0 V to 4.096 V at each input, resulting in a differential input signal range of ±4.096 V when using its internal 4.096 V reference.

DESIGN TIPS

If greater or less signal range is necessary, the gain of the LTC6373 and the ratio of R_F/R_G can be changed. For example, if a ±100 mV signal range is required, R_F can be increased while keeping R_G at its original value. The following formula can be used to recalculate R_F:

$$R_F = (V_{OUT}/V_{IN}) \times R_G \quad (1)$$

where:

$$V_{OUT} = ADC_{IN} + (MAX) - ADC_{IN} - (MIN) \quad (2)$$

$$V_{IN} = V_{IN}(MAX) - V_{IN}(MIN) \quad (3)$$

Because of the greater gain bandwidth of the ADA4945-1, it is recommended to increase its gain rather than the LTC6373.

The filters composed of R5, C6, R6, and C7 reduce the bandwidth of the ADA4945-1. The lower bandwidth results in lower noise at the LTC2387-18 input. The values of C6 and C7 were experimentally determined by gradually increasing the value until the SNR stopped improving.

The filter composed of Resistors R7 and R8 and Capacitors C4 and C5 helps to isolate the ADA4945-1 output from the sampling glitches generated by the ADC inputs if they are not buffered. It limits the bandwidth of the signal provided to the ADC inputs and helps to reduce the noise seen at the ADC inputs.

If the filter between the driver and ADC does not have time to settle, the result is a gain error. Depending on the application, a small gain error may be tolerable but the inability to settle can also cause distortion, which must be avoided. The Precision ADC Driver Tool can be used to check filter settling and estimate circuit SNR and THD performance.

DESIGN PROCEDURE

Initial Conditions and Assumptions

The power supplies for the LTC6373 are set at ±15 V and the power supplies for the ADA4945-1 are set at +5 V/−1 V. Given the input range of 20 V p-p (±10 V) and the output range of 8.192 V p-p (into the ADC), the total gain distributed across the analog front end (AFE) is as follows:

$$G_{TOTAL} = 8.192\ \text{V p-p}/20\ \text{V p-p} = 0.4096\ \text{V/V} \quad (4)$$

Allowing some headroom to accommodate component tolerances and a small variation in common mode, the total gain target is set at 0.4 V/V. The LTC6373 supports a fixed selection of gain values: {0.25, 0.5, 1, 2, ..., 16}. Selecting the gain of both stages to be < 1 allows the use of the smaller power supply range for the ADA4945-1 and lowers the noise gain of each stage. Setting the gain of the LTC6373 to 0.5 results in a gain of 0.8 for the ADA4945-1.

The common mode for both the LTC6373 and ADA4945-1 is set to 2.048 V

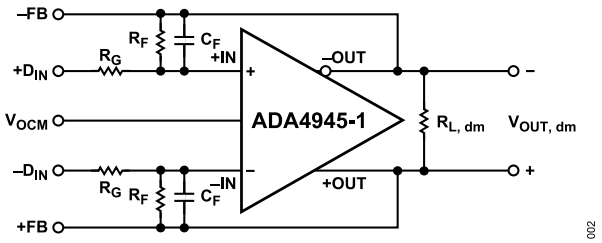

Figure 2. Circuit Definitions for the ADA4945-1

1. For the ADC (LTC2387-18), set the full scale input of ±4.096 V with V_{REF} = 4.096 V and ±V_{FS} = ±4.096 V.
2. Set the driver amplifier (ADA4945-1) V_{OCM}.

   V_{OCM} is biased to 4.096 V/2 = 2.048 V. Check this against the data sheet output common-mode requirement.

   $$(-V_S + 0.4) \le V_{OCM} \le (+V_S - 1.4\ \text{V})$$

   For this application,

   $$-V_S = -1\ \text{V},\ +V_S = 5\ \text{V},\ V_{OCM} = 2.048\ \text{V}$$
   $$(-1 + 0.4) \le V_{OCM} \le (5 - 1.4\ \text{V})$$
   $$(-0.6) \le 2.048\ \text{V} \le (3.6\ \text{V})$$

   where V_{OCM} is within the allowed range. V_{OCM} is supplied by the V_{OCM} pin of the LTC2387-18.
3. Set the input amplifier (LTC6373) input and output limits.

   Because the gain is set to 0.5, the output swing is

   $$\pm 10\text{V}/2 = \pm 5\ \text{V}$$

   The output swing is

$$V_{OCM} \pm 5\ \text{V}/2$$

$$V_{OUT_{max}} = +D_{IN} = 2.048\ \text{V} + 5\ \text{V}/2$$
$$= 2.048\ \text{V} + 2.5\ \text{V} = 4.548\ \text{V}$$
$$V_{OUT_{min}} = -D_{IN} = 2.048\ \text{V} - 5\ \text{V}/2$$
$$= 2.048\ \text{V} - 2.5\ \text{V} = -0.452\ \text{V}$$

For the reversed signal polarity, the value of ±D_{IN} is simply reversed (0.452 V, −4.548 V).

Figure 3 shows the input and output swing limits for the LTC6373 with a gain of 0.5. Looking at the V_S = ±15 V curve, it can be seen that with an input common-mode voltage of 2.048 V and an output differential voltage swinging between ±4.548 V, the LTC6373 is easily capable of supporting this application. However, if ±5 V supplies are used, the LTC6373 may operate outside of its differential output voltage range. The common-mode range vs. differential output voltage curves for all LTC6373 gains are available in the data sheet.

The V_{OCM} of the LTC6373 is also set to 2.048 V using the V_{OCM} pin of the LTC2387-18 to eliminate having to generate another bias point.

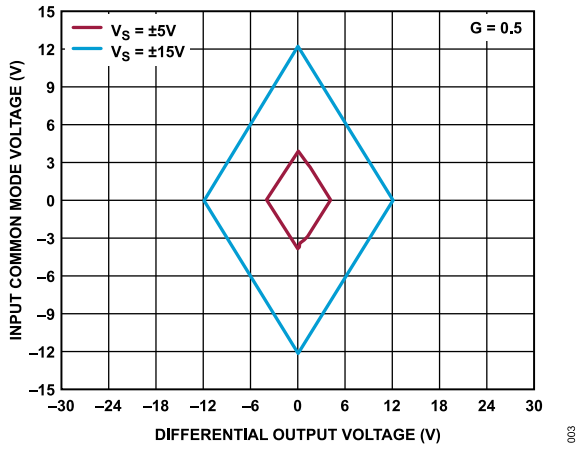

Figure 3. Input Common Mode Range vs. Differential Output Voltage

4. Set the amplifier gain as follows:

$$Gain = V_{OUTdm\_pp}/V_{INdm\_pp} \quad (5)$$

For this application,
$Gain = 8\ \text{V}_{\text{P-P}}/(0.5 \times 20\ \text{V}) = 0.8\ \text{V/V}$

For optimal noise, the ADA4945-1 data sheet recommends 499 Ω for R_F and R_G in a unity-gain setup. In this instance, R_G is scaled to 402 Ω for the desired gain. R_G is composed of the 49.9 Ω and 453 Ω resistors. If THD is more important than SNR, 2 kΩ can be used for R_G and 1.62 kΩ for R_F with a potential 3 dB improvement in THD at the expense of 4 dB in SNR.

5. Set the driver amplifier (ADA4945-1) output swing.

Because the driver amplifier has a differential output swinging about V_{OCM}, when observing +V_{FS}, the op amp outputs are reversed voltages for −V_{FS}. The V_{REF} (4.096 V) is used for the range, even though the actual maximum range is limited to 4 V by the circuit gain. The ADA4945-1 outputs must be able to swing from 0.0 V to 4.096 V for this application.

$$V_{OUTdm} = V_{+OUT} - V_{-OUT} \quad (6)$$

For V_{OUTdm} = +V_{FS},

$$V_{+OUT} = V_{OCM} + V_{OUTdm}/2$$
$$V_{+OUT} = 2.048\ \text{V} + 4.096\ \text{V}/2 = 4.096\ \text{V}$$
$$V_{-OUT} = V_{OCM} - V_{OUTdm}/2 \quad (7)$$
$$V_{-OUT} = 2.048\ \text{V} - 4.096\ \text{V}/2 = 0.0\ \text{V}$$

6. Check the driver amplifier (ADA4945-1) output voltage swing against the data sheet requirements for the supply rails.

According to the ADA4945-1 data sheet at 1 kΩ load,

$$(-V_S + 0.1\ \text{V}) \le V_{OUT} \le (+V_S - 0.1\ \text{V}) \quad (8)$$

For this application,

$$V_{+OUT\_min} = 0\ \text{V}, \quad V_{+OUT\_max} = 4.096\ \text{V}$$
$$-V_{S\_min} = V_{+OUT\_min} - 0.1\ \text{V}$$
$$-V_{S\_min} = 0\ \text{V} - 0.1\ \text{V} = -0.1\ \text{V} \quad (9)$$
$$+V_{S\_min} = V_{+OUT\_max} + 0.1\ \text{V}$$
$$+V_{S\_MIN} = 4.096\ \text{V} + 0.1\ \text{V} = 4.196\ \text{V}$$

7. Set the driver amplifier (ADA4945-1) input swing.

For V_{OUTdm} = +V_{FS}, compute the input common mode voltage as follows:

V_{OUTdm} = 4.096 V, +D_{IN} = 4.548 V, −D_{IN} = −0.452 V,
V_{OUT+} = 4.096 V, V_{OUT-} = 0.0 V
$V_{+IN} = +D_{IN}(R_F/(R_F + R_G)) + V_{-OUT}(R_G/(R_F + R_G))$
V_{+IN} = +4.548(402/(402 + 503)) + 0.0 V(503/(402 + 503)) = 2.02 V (10)
$V_{-IN} = -D_{IN}(R_F/R_F + R_G)) + V_{+OUT}(R_G/(R_F + R_G))$
V_{-IN} = −0.452(402/(402 + 503)) + 4.096 V(503/(402 + 503)) = 2.07 V

For V_{OUTdm} = −V_{FS}, compute the input common mode voltage as follows:

V_{OUTdm} = −4.096 V, +D_{IN} = −0.452 V, −D_{IN} = +4.548 V, V_{OUT+} = 0.0 V, V_{OUT-} = 4.096 V
$V_{+IN} = +D_{IN}(R_F/(R_F + R_G)) + V_{-OUT}(R_G/(R_F + R_G))$
V_{+IN} = −0.452(402/(402 + 503)) + 4.096 V(503/(402 + 503)) = 2.07 V (11)
$V_{-IN} = -D_{IN}(R_F/R_F + R_G)) + V_{+OUT}(R_G/(R_F + R_G))$
V_{-IN} = 4.548(402/(402 + 503)) + 0 V(503/(402 + 503)) = 2.07 V

The ADA4945-1 inputs must be able to swing from 2.02 V to 2.07 V for this application.

8. Check the driver amplifier (ADA4945-1) input common mode.

According to the ADA4945-1 data sheet,

$$-V_S \le V_{CM} \le (+V_S - 1.3\ \text{V})$$
$$-1\ \text{V} \le 2.048\ \text{V} \le 3.7\ \text{V} \quad (12)$$

Data sheet requirements are met.

For this application,

$$V_{+IN\_min} \leq V_{CM} \leq V_{+IN\_max}$$
$$2.03\ \text{V} \leq 2.048\ \text{V} \leq 2.07\ \text{V} \quad (13)$$

Application requirements are met.

DESIGN SIMULATIONS

The **Precision ADC Driver Tool** provides a specialized simulation environment where the engineer can quickly determine the impact of the drive amplifier and R-C filter selection on the overall performance of an ADC signal chain.

Using the Precision ADC Driver Tool as shown in Figure 4, settling time, noise, and THD performance are estimated. The Precision ADC Driver Tool does not currently allow the LTC6373 to be added to the schematic. Therefore, only the ADA4945-1 performance driving the LTC2387-18 is simulated. The driver tool suggests the minimum supply voltages to be +4.6 V and −0.5 V. The driver tool warns that the driver selected significantly degrades the overall noise performance. R_F and R_G are the largest contributors to driver noise. The driver tool does not allow capacitors to be added across R_F as in the application shown. The capacitors reduce driver noise. The summary of design goals vs. simulated results is shown in Table 2.

Table 2. Design Goal vs. Simulation

Parameter	Design Goal	Simulation
SNR	95.7 dB	91.9 dB
THD	−117 dB	−116 dB

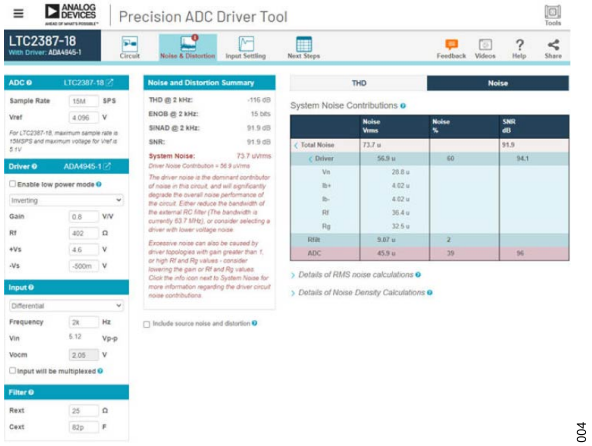

Figure 4. Precision ADC Driver Tool: Noise and THD Results

MEASURED RESULTS

The measured ADC SNR performance is 0.4 dB lower than the ADA4945-1 data sheet typical specification of −95.7 dB, and the THD performance is 3.8 dB lower than the data sheet typical specification of −117 dB, as shown in Figure 5.

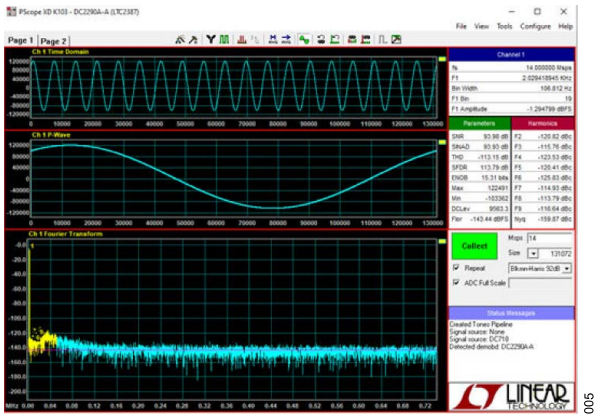

Figure 5. Measured Performance of the Circuit of Figure 1

The summary of design goals vs. simulated results is shown in Table 3. THD performance can potentially be improved by up to 3 dB by increasing the ADA4945-1 R_G to 2 kΩ and R_F to 1.62 kΩ. This increase results in a degradation of SNR performance by 4 dB according to the ADC driver tool. It is up to the user to determine whether THD or SNR performance is more important. All data taken is at a 14 MSPS data rate. At 15 MSPS, THD is degraded significantly due to the small ADC acquisition period.

Table 3. Design Goal vs. Measured

Parameter	Design Goal	Measured
SNR	95.7 dB	95.3 dB
THD	−117 dB	−113.2 dB

As shown in Figure 6, THD exceeds −100 dB when the input frequency goes above 15 kHz. SNR goes below 90 dB when the input frequency goes above 90 kHz. This data was taken at 25°C. At lower or higher temperatures, performance may start to degrade earlier. Variations in circuit processing may also result in a different voltage where performance starts to degrade.

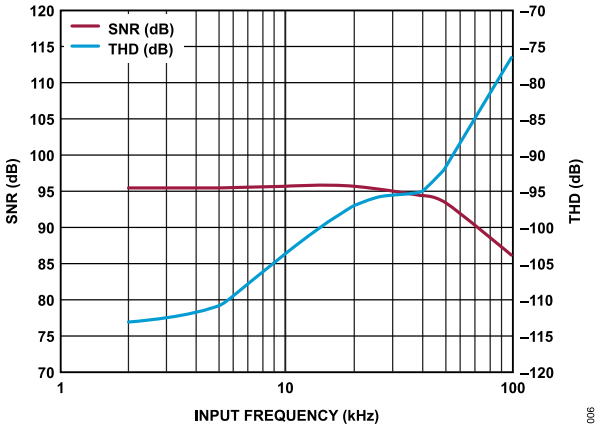

Figure 6. SNR and THD vs. Input Frequency

DESIGN DEVICES

Table 4. Operational Amplifiers—ADA4945-1

Parameter	Value
Input Offset Voltage Maximum	50 µV

Table 4. Operational Amplifiers—ADA4945-1 (Continued)

Parameter	Value
Bias Current Maximum	−2.5 µA
Gain Bandwidth Product Typical	145 MHz
Noise Voltage Typical	5 nV/√Hz
Quiescent Current per Amplifier Typical	180 µA
Supply Voltage Span Minimum/Maximum	3 V/10 V

Table 5. Operational Amplifiers—LTC6373

Parameter	Value
Input Offset Voltage Maximum	464 µV
Bias Current Maximum	0.0005 µA
Gain Bandwidth Product Typical	7 MHz
Noise Voltage Typical	26.4 nV/√Hz
Quiescent Current per Amplifier Typical	4.4 mA
Supply Voltage Span Minimum/Maximum	9 V/36 V

Table 6. ADCs—LTC2387-18

Parameter	Value
Resolution	20 bits
Sampling Frequency Maximum	1 MSPS
Input Type (Single-Ended or Differential)	Fully differential
V_{IN} Span V_{MIN}/V_{MAX}	5 V
SNR Typical	104 dB
THD Typical	−125 dB
Data Interface (I^2C, Serial Peripheral Interface (SPI), Parallel)	SPI