Single-Ended-to-Differential Converters for Voltage Output and Current Output DACs Using the AD8042 Op Amp

CIRCUIT FUNCTIONS AND BENEFITS

With single-ended signaling, one wire from the signal source is routed throughout the system to the data acquisition interface. The voltage measured is the difference between the signal and the ground. Unfortunately, ground can be a different level in different places because the ground impedance can never be zero. This can lead to errors when using single-ended inputs, especially where the signal trace is long and grounds currents contain large digital transients. Single-ended signal runs are sensitive to noise pickup because they act as an antenna, picking up electrical activity. With single-ended inputs there is no way of distinguishing between the signal and the interfering noise. Most of the ground and noise problems are solved by differential signaling.

With differential signaling, two signal wires run from the signal source to the data acquisition interface. This can solve both of the problems caused by single-ended connections. Noise between the sending and receiving ground planes acts as a common-mode signal and is, therefore, greatly attenuated. The use of twisted pair wire causes noise pickup to appear as a common-mode signal, which is also greatly attenuated at the receiver. Another advantage of differential transmission is that the differential signal has twice the amplitude of the equivalent single-ended signal, therefore giving greater noise immunity.

Here we describe a differential driver that can be adapted to either a voltage or current output DAC. The driver is based on the dual AD8042 op amp configured as a cross-coupled differential driver. The AD8042 has a rail-to-rail output stage that operates within 30 mV of either rail and an input stage that can operate 200 mV below the negative supply (ground in this circuit) and within 1 V of the positive supply. In addition, the AD8042 has 160 MHz bandwidth and fast settling time, making it an ideal choice for the output driver.

The voltage output DAC is the 12-bit AD5620, a member of the *nano*DAC® family. The DAC contains an on-chip 5 ppm/°C reference and is available in an 8-lead SOT-23 or MSOP package. The current output DAC is the 12-bit AD5443, which is available in a 10-lead MSOP package.

The two circuits represent a cost effective, low power, and small board area solution for generating differential signals from industrial CMOS DACs. Both circuits operate on a single +5 V supply.

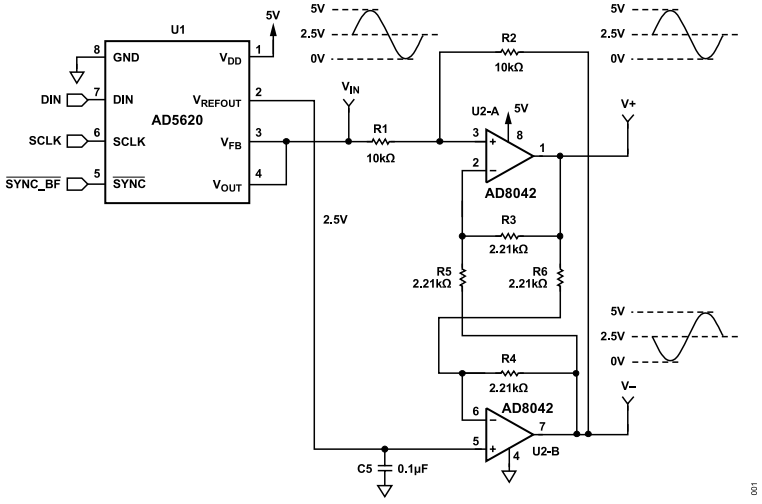

Figure 1. Differential Driver for the AD5620 Voltage Output DAC

TABLE OF CONTENTS

REVISION HISTORY

4/2024—Rev. A to Rev. B

Converted Document from CN-0143 to AN-2509..... 1
Deleted Common Variations Section, Learn More Section, and Data Sheets and Evaluation Boards Section..... 3

CIRCUIT DESCRIPTION

The circuit shown in Figure 1 operates on a single +5 V supply and utilizes the AD5620 voltage output DAC. The input to the DAC is controlled by an SPI port. The output of the DAC swings between 0 V and +5 V. The on-chip DAC reference (+2.5 V) is used to set the common-mode voltage of the AD8042 differential driver circuit. This reference has a temperature coefficient of 5 ppm/°C.

The output at V− is the inverted DAC output centered around a common-mode voltage of +2.5 V. The feedback network and U2-B force the voltage at V+ to be 180° out of phase with respect to V−. Waveforms for the input and output of the driver are shown in Figure 2. The differential outputs will only go to within about 30 mV of each rail; therefore, there will be some clipping if the DAC is operated in these regions.

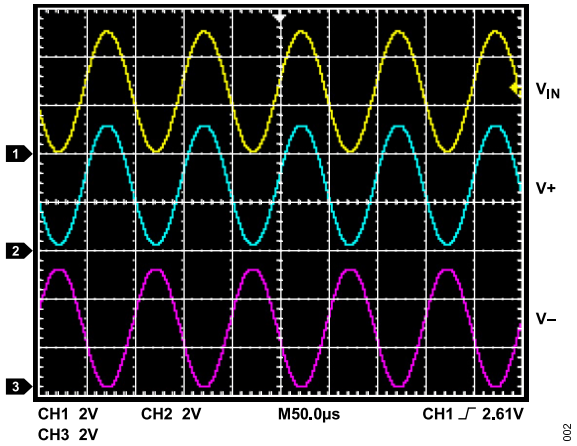

Figure 2. AD5620 V_{IN}, V+, and V− at 100 kSPS Update Rate

The circuit shown in Figure 3 also operates on a single +5 V supply and utilizes the AD5443 current output DAC in a mode where the IOUT2 pin is connected to +2.5 V, and the VREF pin is grounded. The ADR444 precision 4.096 V reference and a divider network are used to generate the +2.5 V for the IOUT2 pin of the DAC and the +3.75 V common-mode voltage for the output driver stage.

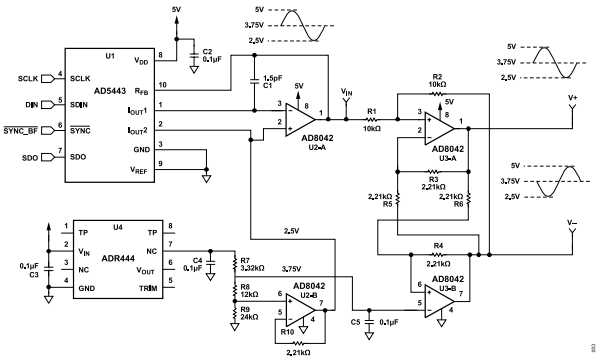

Figure 3. Differential Driver for the AD5443 Current Output DAC

Under these conditions the output of U2-A swings between +2.5 V and +5 V. The differential outputs of the driver will only go to within about 30 mV of the positive rail; therefore, there will be some clipping if the DAC is operated in this region. Figure 4 shows the corresponding input and output waveforms for the output driver stage of Figure 3.

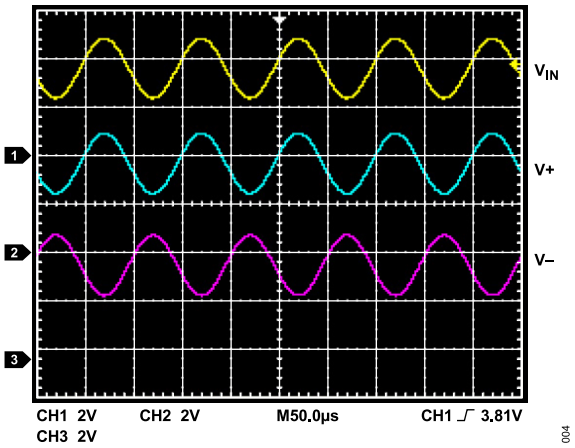

Figure 4. AD5443 V_{IN}, V+, and V− at 100 kSPS Update Rate

The single-ended-to-differential converter stage has a bandwidth of typically 10 MHz. However, the maximum output frequency is controlled by a DAC update rate, which is 125 kSPS for the AD5620 and 2.5 MSPS for the AD5443. Sampling theory limits the maximum output frequency to about one-third the maximum update rate.

Excellent layout, grounding, and decoupling techniques must be utilized to achieve the desired performance from the circuits discussed (see Tutorial MT-031 and Tutorial MT-101).