AN-2047
APPLICATION NOTE

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Configuring the ADIN1300 Ethernet PHY

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INTRODUCTION

The ADIN1300 is a low power, low latency, robust 10 Mbps, 100 Mbps, and 1000 Mbps, Ethernet physical layer (PHY) device targeting harsh applications in industrial automation, factory automation, building automation, energy, time sensitive networking (TSN), and industrial Internet of Things (IoT). The ADIN1300 has been extensively tested for electromagnetic compatibility (EMC), electrostatic discharge (ESD), and robust performance for industrial applications. The ADIN1300 provides various configurations for fitting the PHY into an industrial Ethernet communications system. This application note describes the various configurations available of the PHY device core of the ADIN1300 using its hardware configuration pins.

The sections within this application note provide a high level overview, and this application must be used in conjunction with the ADIN1300 data sheet.

Note that multifunction pin names maybe referenced by their relevant function only.

TABLE OF CONTENTS

REVISION HISTORY

4/2020—Revision 0: Initial Version

PHY DEVICE CORE OF THE ADIN1300

The ADIN1300 is compliant with the IEEE 802.3 Ethernet standard. The ADIN1300 can operate in unmanaged or managed applications using multilevel strapping and operates over a wide industrial temperature range (−40°C to +105°C). The ADIN1300 supports the following media access control (MAC) interfaces:

- Media independent interface (MII)
- Reduced MII (RMII)
- Reduced gigabit MII (RGMII)

HARDWARE CONFIGURATION PINS

In unmanaged applications, the PHY devices core of the ADIN1300 is configured from the voltage levels of the configuration pins (PHY_CFG1 and PHY_CFG0) without any software intervention via the MDIO pin interface. The PHY can also establish a link once an Ethernet cable is connected.

In managed applications, the ADIN1300 can be configured using software via the MDIO pin interface. Before the software configuration process, the PHY must enter power-down mode after a reset.

There are several hardware configuration pins in the ADIN1300. The voltage on these pins is sensed and latched when exiting from a reset. Some pins are multilevel sensed, while other pins are two-level sensed. Note that the hardware configuration pins are also shared with functional pins.

The following functions are configurable from the ADIN1300 hardware pins:

- PHY address
- Forced or advertised PHY speed
- Software power-down mode after reset
- Downspeed enabled
- Energy detect power-down mode
- Energy efficient Ethernet (EEE) enabled
- Automatic medium dependent interface crossover (MDIX)
- MAC interface selection (RGMII, RMII, or MII)

Four different modes are available with four different voltage levels that can be sensed on a hardware configuration pin. MODE_1 and MODE_4 are relevant to the two-level sense pins, and these modes are implemented with a 10 kΩ pull-down resistor or a 10 kΩ pull-up resistor, respectively.

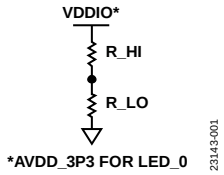

Figure 1. Hardware Configuration Pin Implementation

For the LED_0 pin, the resistor must be pulled up to AVDD_3P3 rather than VDDIO.

The voltage levels in Table 2 were chosen to steer clear of the standard input high voltage (V_{IH}) and input low voltage (V_{IL}) levels to avoid any shoot through currents (and unknown voltage levels) in the input driver of disabled devices connected to the pins. V_{IH} and V_{IL} voltage levels do have voltage and device dependencies, and, therefore, it may not always be possible to avoid such artifacts.

Table 1 assumes no extra loading from external circuitry to the ADIN1300. However, it is expected that some configuration pins are connected to external circuits, such as field-programmable gate array (FPGA) inputs that can have their own internal pull-up/pull-down resistors, which loads the resistor divider voltage. For example, assuming there is an external pull-up resistor >43 kΩ and an external pull-down resistor >37 kΩ, replace the 10 kΩ resistor used in MODE_1 and MODE_4 with a 2.5 kΩ resistor.

The large resistance values in Table 1 were chosen to minimize power consumption from the resistor ladder. Although smaller resistance values can be used, but the user must maintain the same resistor ratios for the selected values.

Table 1. Configuration Modes

Mode	Low Resistor (R_LO)	High Resistor (R_HI)	Voltage Threshold
MODE_1	10 kΩ	Open	
MODE_2	10 kΩ	56 kΩ	>0.1 × VDDIO[1]
MODE_3	56 kΩ	10 kΩ	>0.5 × VDDIO[1]
MODE_4	Open	10 kΩ	>0.9 × VDDIO[1]

[1] The supply rail for the LED_0 pin is AVDD_3P3 rather than VDDIO. Therefore, pull up any pull-up on the LED_0 pin to AVDD_3P3.

Table 2. Voltage Levels for Modes vs. VDDIO Voltage (or AVDD_3P3 for LED_0)

Mode	1.8 V (V)	2.5 V (V)	3.3 V (V), VDDIO/AVDD_3P3[1]
MODE_1	<0.18	<0.25	<0.33
MODE_2	>0.18	>0.25	>0.33
MODE_3	>0.9	>1.25	>1.65
MODE_4	>1.62	>2.25	>2.97

[1] The supply rail for the LED_0 pin is AVDD_3P3 rather than VDDIO. Therefore, pull up any pull-up on the LED_0 pin to AVDD_3P3.

MAC Interface Selection

The type of MAC interface can be configured using the MACIF_SEL0 (Pin 34) pin and the MACIF_SEL1 (Pin 35) pin. These pins are two-level pins (high or low) that have internal 45 kΩ pull-down resistors. However, external pull-down resistors can be used for stronger pull-down. See Table 1 for the recommended R_LO and R_HI values.

Table 3 describes the MAC interface selection using the MACIF_SELx pins. See the ADIN1300 data sheet for the specific requirements for MAC interface selection.

MAC interface selection can also be configurable from the hardware pins. The ADIN1300 must be in software power-down before any changes can be made to the MAC interface configuration. The exemption is RMII mode, which is not configurable using software because this mode requires a 50 MHz reference clock. Do not use software to configure the MAC interface to the RMII.

The choice of the MAC interface is for the practicality of pin count, latency, and availability. The MII and the RMII support 10 Mbps and 100 Mbps. The MII requires 15 pins, while the RMII requires only 7 pins. On the processor side, there can be different interfaces (general-purpose device for the PHY), and it is common to see the RMII used because this interface saves on pin count. Likewise, on a multiport switch (4, 5, 8, or higher ports), the MII is not typically used because of its higher pin count.

The RGMII supports 10 Mbps, 100 Mbps, and gigabit Ethernet. The GMII requires 25 pins, while the RGMII requires only 12 pins. Therefore, the RGMII is typically used because this interface saves on pin count in gigabit interfaces. When the RGMII is compared to the MII for 10 Mbps and 100 Mbps, the RGMII also saves on pin count, which is why the RGMII is commonly used in gigabit Ethernet designs.

For devices designed for a nonGigabit Ethernet applications, the MII or the RMII are typically used instead of RGMII because a gigabit Ethernet PHY has higher IC pin counts than the 100 Mbps or 10 Mbps Ethernet PHY.

The disadvantage of the RMII over the MII and the RGMII is that the RMII uses a 50 MHz clock, while the MII and the RGMII use a 25 MHz clock, which can add complexity and cost to an Ethernet design.

Latency is an important parameter when considering MAC interface selection, especially for industrial Ethernet. The MII has the lowest latency for 10 Mbps and 100 Mbps, and, in particular, an MII where the input clock pin on the PHY (CLK_IN) is synchronous and fixed in phase to the MII clock to eliminate the use of the first in, first out (FIFO) at the MII interface. The RMII has higher latency, primarily because FIFO and clock delays must be used to multiplex the data into the pins, which is half of the pin count of the MII. The RGMII is almost as low latency as the GMII with an additional 8 ns. However, when using 100 Mbps, there is an additional 40 ns.

Table 3. MAC Interface Selection

MAC Interface Selection	MACIF_SEL1	MACIF_SEL0
RGMII RXC/TXC 2 ns Delay	Low	Low
RGMII RXC Only 2 ns Delay	High	Low
MII	Low	High
RMII	High	High

PHY Address

The ADIN1300 has four PHY address pins available for configuring the PHY address: PHYAD_0 (Pin 33), PHYAD_1 (Pin 32), PHYAD_2 (Pin 30), and PHYAD_3 (Pin 29). These pins are shared with the RXD_0 to RXD_3 pins. The PHYAD_x pins are two-level configuration pins, which means that it is possible to configure the ADIN1300 to any of the 16 available PHY addresses. There are weak internal pull-down resistors on all PHYAD_x pins.

Speed Configuration

The PHY configuration pins, PHY_CFG0 (Pin 21) and PHY_CFG1 (Pin 26), are also shared to the functional pins. These pins have no internal pull-up resistors. Therefore, use external resistors to configure the appropriate function. These pins are multilevel sense pins, allowing four distinct voltage levels to be configured to provide a wider range configuration.

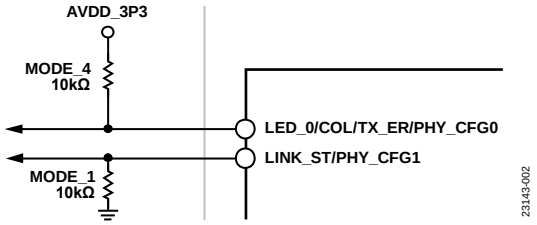

Figure 2. An Example Speed Configuration for PHY_CFGx

In Figure 2, PHY_CFG1 has an external pull-down resistor configuring MODE_1 (0 V), while PHY_CFG0 has a pull-up resistor configuring MODE_4 (3.3 V). This setting results in the PHY operating on either 10 Mbps with half duplex or full duplex or 100 Mbps with half duplex or full duplex advertised speeds. When connected to a link partner, the ADIN1300 links with the highest common speed.

Medium Dependent Interface Configuration

The medium dependent interface configuration is determined by the MDIX_MODE (Pin 27), which is also a shared function. The MDIX_MODE pin describes the interface from a physical layer implementation to the physical medium used to carry the transmission (straight or crossover). With a straight through cable, the cable must be set to a medium dependent interface (MDI) on one side and MDIX on the other side (see Figure 3). With a crossover cable, the cable can be either MDI or MDIX (see Figure 4).

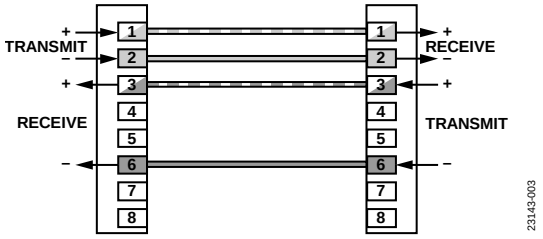

Figure 3. Straight Connection

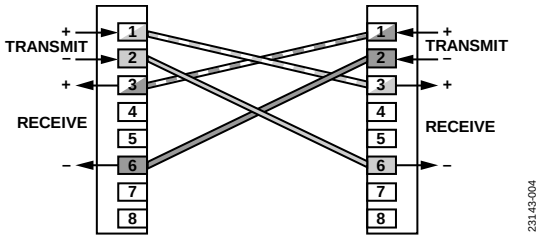

Figure 4. Crossover Connection

The MDIX_MODE pin does not have an internal pull-up. This pin is a multilevel sense pin. Therefore, there are four voltage level options available for this configuration using external resistors.

If automatic MDIX mode is enabled, the MDIX_MODE pin must be configured to MODE_3 or MODE_4 (see Table 4). These modes enable the device to automatically detect the appropriate MDI or MDIX configuration suited to the link partner.

Table 4. Media Dependent Interface Configuration

Configuration	MDIX_MODE
Manual MDI	MODE_1
Manual MDIX	MODE_2
Automatic MDIX, Prefer MDIX	MODE_3
Automatic MDIX, Prefer MDI	MODE_4

During automatic MDIX or negotiate, each PHY automatically transmits pulses. Setting one PHY communication side as prefer MDI, and the other PHY communication side as prefer MDIX, controls which PHY starts sending pulses, and typically, results in a faster MDI and/or MDIX resolution. However, this setting still works as normal automatic MDIX even if the other side does not support prefer MDI or prefer MDIX. For more information, refer to the ADIN1300 data sheet.

Pair swapping of the Ethernet pins are allowed in the ADIN1300 because of the automatic MDIX feature. Automatic MDIX swops pairs automatically because a crossover cable is used, and it considers the printed circuit board (PCB) layout and placement of the MDI_x_x pins (Pin 12 to Pin 19) of the PHY to the RJ45 of the Ethernet.

Table 5 details the MDI_x_x pins to the RJ45 of the Ethernet pairings with MDI mode and MDIX mode.

Table 5. MDI_x_x Pins to RJ45 of the Ethernet on 10 Mbps or 100 Mbps Pairings (See Figure 3 Through Figure 6)

MDI_x_x Pin	RJ45 Pin	MDI Mode	MDIX Mode
MDI_0_P	1	Transmit±	Receive±
MDI_0_N	2	Transmit±	Receive±
MDI_1_P	3	Receive±	Transmit±
MDI_1_N	6	Receive±	Transmit±
MDI_2_P	4	Not used	Not used
MDI_2_N	5	Not used	Not used
MDI_3_P	7	Not used	Not used
MDI_3_N	8	Not used	Not used

For example, in Figure 5, 10BASE-T and 100BASE-Tx transmit on one pair and receive on the other pair. Therefore, in MDI mode, transmit is on MDI_x_x, Pair 0 (RJ45, Pin 1 and Pin 2) and receive is on MDI_x_x, Pair 1 (RJ45, Pin 3 and Pin 6), while in MDIX mode, Pair 0 and Pair 1 swop. Therefore, a crossover cable must connect the PHYs together. If a straight through cable is used, the PHYs detect this and automatically swaps Pair 0 and Pair 1 on the PHY. In 1000BASE-T, echo cancellation is used, and transmitting and receiving are done on each pair. Four logical pairs, A, B, C, and D, are mapped. For MDI mode, Pair 0 is Transmit A and Receive B, and Pair 1 is Transmit B and Receive A.

Table 6. MDI_x_x Pins to RJ45 of the Ethernet on 1 Gbps Pairing (See Figure 3 Through Figure 6)

MDI_x_x Pin	RJ45 Pin	MDI Mode	MDIX Mode
MDI_0_P	1	Transmit A±	Transmit B±
MDI_0_N	2	Receive B±	Receive A±
MDI_1_P	3	Transmit B±	Transmit A±
MDI_1_N	6	Receive A±	Receive B±
MDI_2_P	4	Transmit C±	Transmit D±
MDI_2_N	5	Receive D±	Receive C±
MDI_3_P	7	Transmit D±	Transmit C±
MDI_3_N	8	Receive C±	Receive D±

Figure 5 and Figure 6 illustrate the pairing of the RJ45 pins of two Ethernet PHYs as detailed in Table 5 for a 10 Mbps or 100 Mbps connection and Table 6 for a 1 Gbps connection.

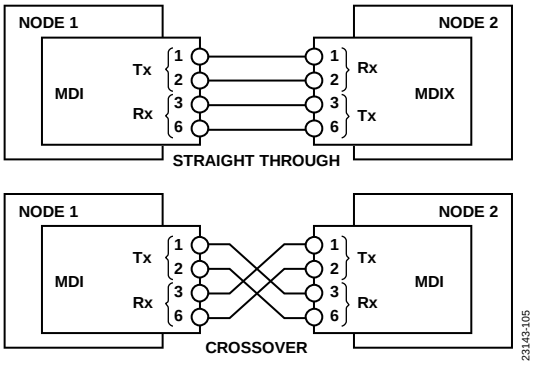

Figure 5. 10 BASE-T or 100BASE-Tx Pairing

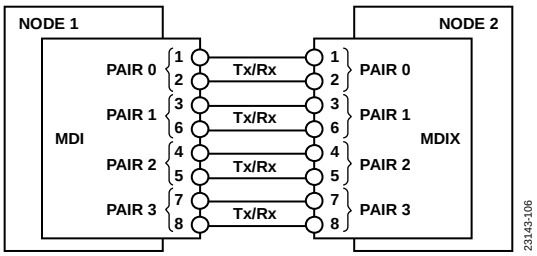

Figure 6. 1000BASE-T Pairing

HARDWARE CONFIGURATION EXAMPLES

This section details how to configure the ADIN1300 for common Ethernet PHY scenarios.

MANAGED APPLICATIONS

In managed applications, it is appropriate to configure the PHY at all possible speeds. It is easier to configure a managed application because the number of strapping resistors is at a minimum, and the strapping resistors are pulled to VDDIO or ground.

Figure 7 provides the minimum configuration of strapping resistors and is shows the recommended configuration for a managed application.

RGMII, Advertised 10 Mbps, 100 Mbps, or 1000 Mbps with Full Duplex or Half Duplex with Downspeed, Energy Detect Power-Down (EDPD) Mode, and EEE Enabled

The example shown in Figure 7 shows the minimum set of strapping resistors suited for an RGMII managed application. The MAC interface configuration pins have pull-down resistors and default to the RGMII MAC interface. The PHY address pins also have pull-down resistors, Therefore, the PHY address defaults to zero. To configure automatic MDIX operation, add a pull-up resistor on GP_CLK.

In addition, it is recommended to have pull-up resistors on the PHY_CFG0 and PHY_CFG1 pins and to configure these pins to the MODE_4 settings. It is also recommended to use an active low light emitting diode (LED) on LED_0.

The following summarizes an RGMII downspeed, EDPD, and EEE enabled configuration for managed applications:

- MAC interface = RGMII (default)
  - MACIF_SEL0 = MODE_1 = 10 kΩ pull-down resistor
  - MACIF_SEL1 = MODE_1 = 10 kΩ pull-down resistor
- MDIO_MODE = automatic MDIX, preferred MDI
  - MODE_4 (10 kΩ pull-up resistor)
- PHY address = 0b0000
- Speed selection = 10 Mbps, 100 Mbps, or 1000 Mbps with full duplex or half duplex, automatic negotiate enabled, downspeed, EDPD and EEE
  - PHY_CFG0 = MODE_4 = 10 kΩ pull-up resistor
  - PHY_CFG1 = MODE_4 = 10 kΩ pull-up resistor

To perform software power-down mode, set the SFT_PD bit of the MII_CONTROL register. For more information, refer to the ADIN1300 data sheet.

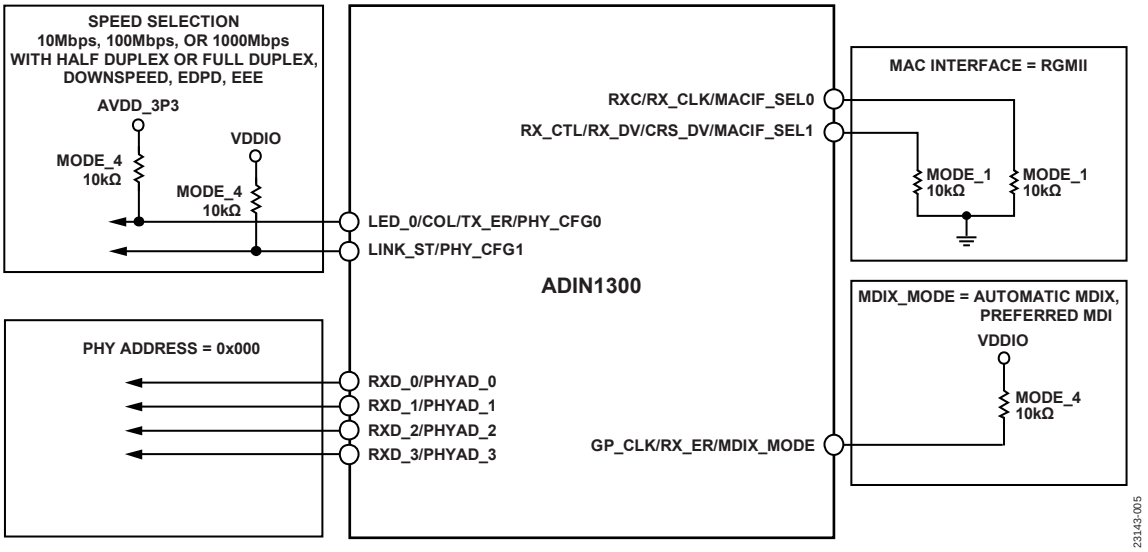

Figure 7. RGMII, 10 Mbps, 100 Mbps, or 1000 Mbps with Full Duplex or Half Duplex with Downspeed, EDPD Mode, and EEE Enabled Configuration for Managed Applications

RGMII, Advertised 10 Mbps, 100 Mbps, or 1000 Mbps with Full Duplex or Half Duplex with Software Power-Down Enabled After Reset

A managed RGMII can also be bootstrapped into software power-down mode. The following list describes an advertised 10 Mbps, 100 Mbps, or 1000 Mbps, full duplex or half duplex with software power-down enabled after reset. The MAC interface configuration pins are pulled to ground, setting the PHY to an RGMII. GP_CLK is pulled to VDDIO to configure an automatic MDIX operation. In addition, the PHY_CFG0 and PHY_CFG1 pins are both configured to the MODE_3 settings, and an active low LED must be used on LED_0.

The following list summarizes an RGMII auto negotiate, 10 Mbps, 100 Mbps, or 1000 Mbps with full duplex or half duplex, with the software power-down enabled after reset:

- MAC Interface = RGMII
  - MACIF_SEL0 = MODE_1 = 10 kΩ pull-down resistor
  - MACIF_SEL1 = MODE_1 = 10 kΩ pull-down resistor
- MDIX_MODE = automatic MDIX, preferred MDI
  - MDIX_MODE = MODE_4
- PHY address = 0b0001
- Speed selection = 10 Mbps, 100 Mbps, or 1000 Mbps with full duplex or half duplex, automatic negotiate enabled
  - PHY_CFG0 = MODE_4 = 10 kΩ pull-up resistor
  - PHY_CFG1 = MODE_3 = 10 kΩ pull-up resistor and 56 kΩ pull-down resistor

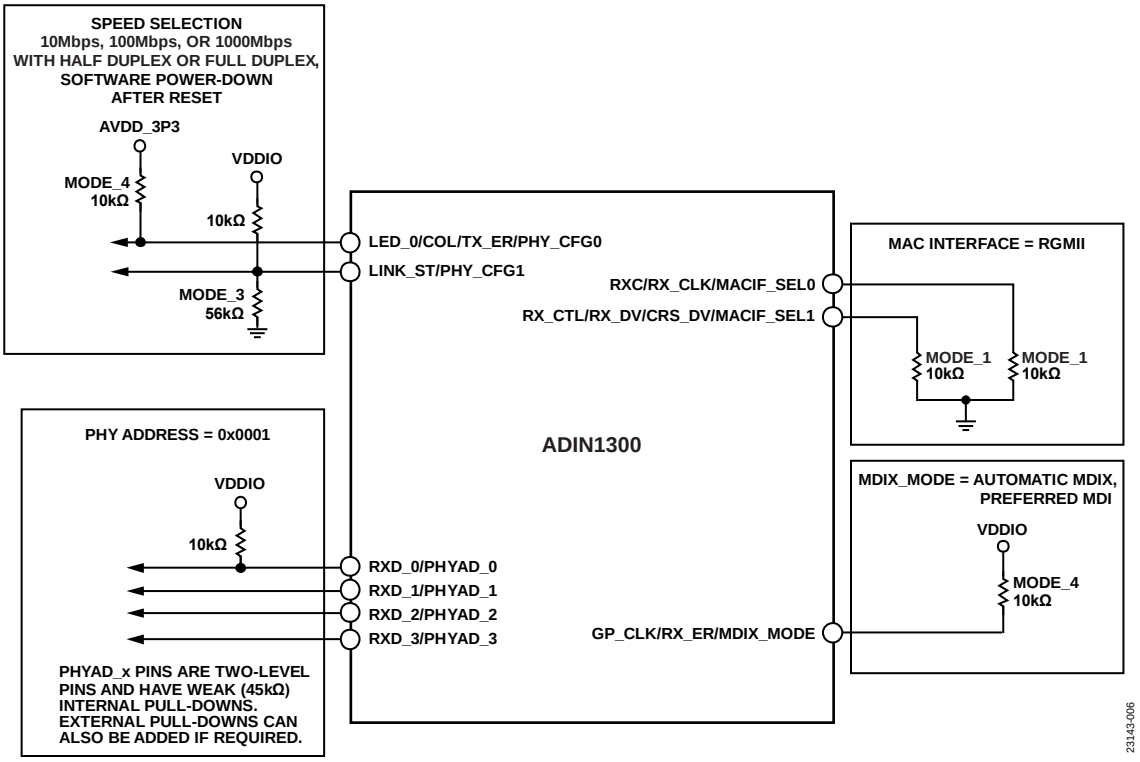

Figure 8. RGMII Auto Negotiate, 10 Mbps, 100 Mbps, and 1000 Mbps with Half Duplex or Full Duplex with Software Power-Down Enabled After Reset Configuration for Managed Applications

UNMANAGED APPLICATION

In unmanaged applications, the ADIN1300 latches the configuration based on the voltage levels acquired during bootstrap. These voltage values are read during power-up or hardware reset and are latched. Then, the PHY immediately attempts to bring up links as configured by the configuration pins. More information about unmanaged applications can be found in the ADIN1300 data sheet.

MII, Advertised 10 Mbps or 100 Mbps with Full Duplex and or Half Duplex

The following list details the pin configuration and external resistors required for the MII MAC interface with automatic negotiate enabled:

- MAC interface = MII
  - MACIF_SEL0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - MACIF_SEL1 = MODE_1 is configured using a 10 kΩ pull-down resistor
  - MDIX_MODE = automatic MDIX, preferred MDIX
    - MDIX_MODE = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)
  - PHY address = 0b0011
  - Speed selection = 10 Mbps or 100 Mbps with full duplex and or half duplex, automatic negotiate enabled
    - PHY_CFG0 = MODE_2 = 56 kΩ pull-up resistor and 10 kΩ pull-down resistor
    - PHY_CFG1 = MODE_4 = 10 kΩ pull-up resistor

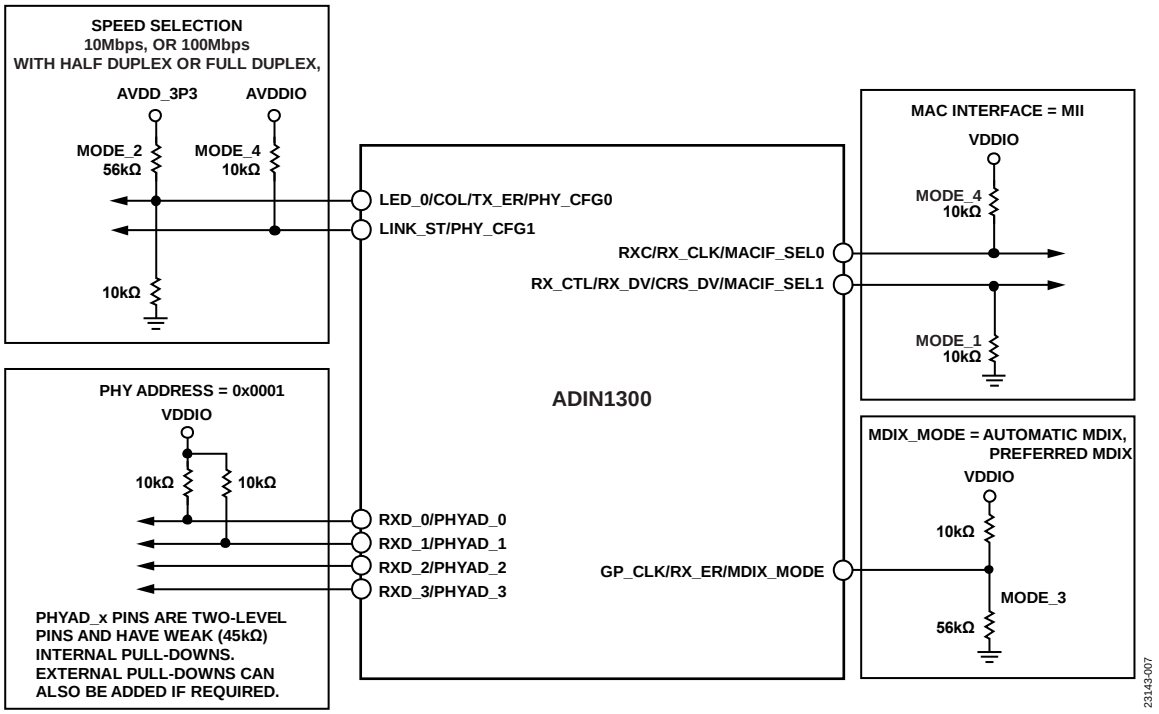

Figure 9. MII, Advertised 10 Mbps or 100 Mbps with Full Duplex and or Half Duplex Configuration for Unmanaged Applications

RMII, Advertised 10 Mbps or 100 Mbps with Full Duplex

The following list details the pin configuration and resistors required external to the ADIN1300 for RMII MAC interface with auto negotiate enabled advertising 10 Mbps or 100 Mbps with full duplex speed:

- MAC interface = RMII
  - MACIF_SEL0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - MACIF_SEL1 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - MDIX_MODE = automatic MDIX, preferred MDIX
    - MDIX_MODE = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)
  - PHY address = 0b0100
  - Speed selection = 10 Mbps or 100 Mbps with full duplex, automatic negotiate enabled
    - PHY_CFG0 = MODE_3 = 10 kΩ pull-up resistor and 56 kΩ pull-down resistor
    - PHY_CFG1 = MODE_4 = 10 kΩ pull-up resistor

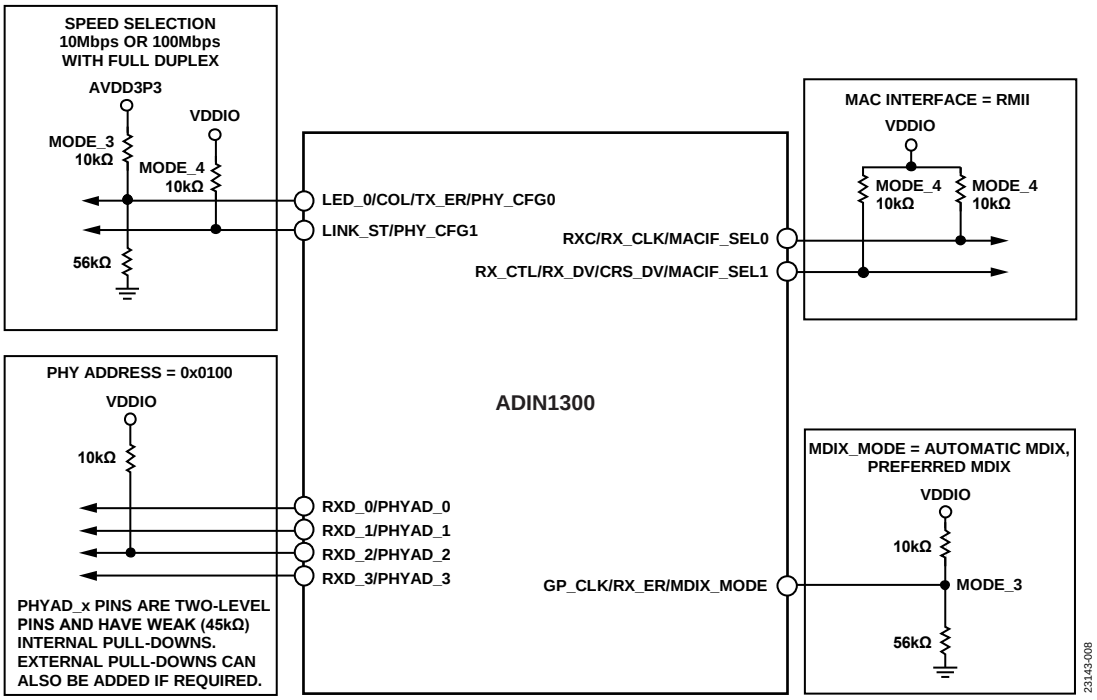

Figure 10. RMII, Advertised 10 Mbps or 100 Mbps with Full Duplex Configuration for Unmanaged Applications

RMII, Forced 100 Mbps with Full Duplex

The following list details the pin configuration and resistors required external to the ADIN1300 for an RMII MAC interface with forced negotiate enabled 100 Mbps with full duplex:

- MAC interface = RMII
  - MACIF_SEL0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - MACIF_SEL1 = MODE_4 is configured using a 10 kΩ pull-up resistor
- MDIX_MODE = manual MDI
  - MDIX_MODE = MODE_1 (10 kΩ pull-down resistor)
- PHY address = 0b0101
- Speed selection = 100 Mbps with full duplex, forced
  - PHY_CFG0 = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)
  - PHY_CFG1 = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)

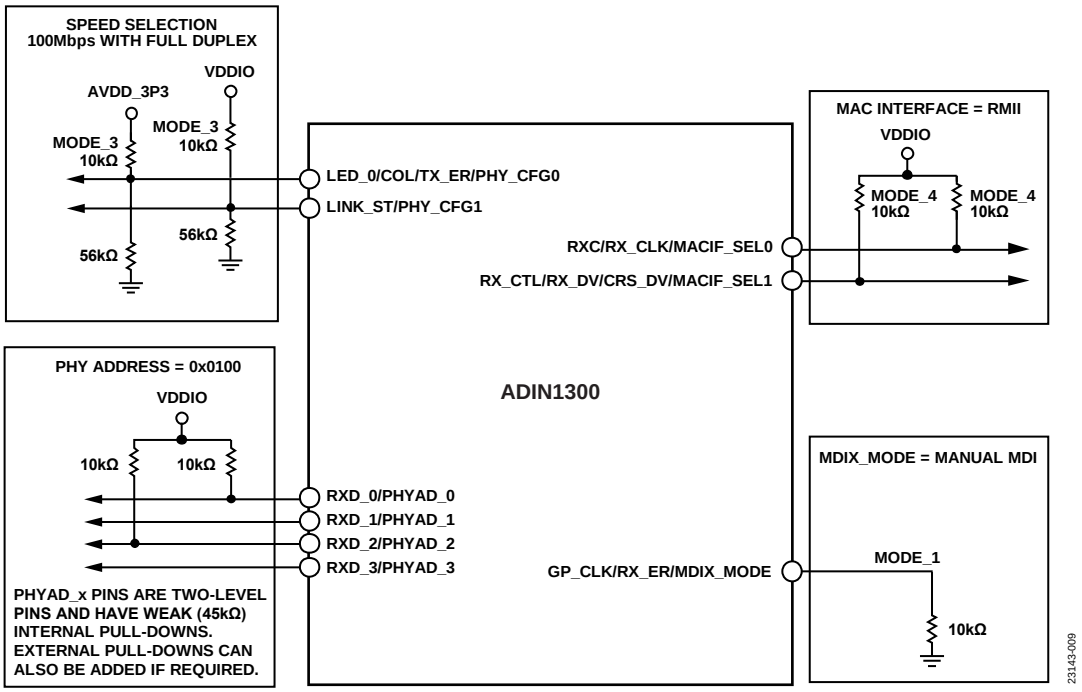

Figure 11. RMII, Forced 100 Mbps, Full Duplex Configuration for Unmanaged Applications

CONCLUSION

The ADIN1300 1 Gb Ethernet PHY can be configured on different MAC interfaces, speeds, and transmission mediums. The examples discussed in this application note tackle common application configurations for the ADIN1300 Ethernet PHY in the industrial Ethernet market. If software intervention is performed on the PHY, the configurations listed in the unmanaged applications section can also be used on managed applications.

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