AN-2044
APPLICATION NOTE

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How to Configure the AD5592R/AD5592R-1 for Control and Monitoring for a Flexible System Design with Multifunctional Operations

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INTRODUCTION

The AD5592R/AD5592R-1 are an 8-channel, 12-bit, configurable analog-to-digital converter (ADC) or digital-to-analog converter (DAC). Each channel has an input/output (I/Ox) pin (I/O0 to I/O7) that can be independently configured as analog outputs, analog inputs, digital outputs, digital inputs, 85 kΩ pull-down resistors, or three-state pins. When configured as an analog output, the I/Ox pin behaves as a 12-bit DAC channel, and when configured as an analog input, the I/Ox pin behaves as a multiplexed ADC channel. When configured as a digital output, the I/Ox pin is configured as a push pull or open-drain output, and when configured as a digital input, the I/Ox pin can read the status of the general-purpose input/output.

Optionally, when configured with a pull-down resistor to GND, the I/Ox pin can connect to a logic input, to a microcontroller, or to a logic gate. The I/Ox pin can also be three-state when the I/Ox pin of multiple devices are connected to the same signal path.

In addition, the I/O7 pin can be configured as a $\overline{\text{BUSY}}$ output indicator for an on-chip ADC conversion.

The main application of the AD5592R/AD5592R-1 is for control and monitoring due to their high flexibility and small size. See the latest functional block diagram of the AD5592R/AD5592R-1 in the AD5592R/AD5592R-1 data sheet.

This application note is a guide on how to configure the AD5592R/AD5592R-1 and should be used in conjunction with the AD5592R/AD5592R-1 data sheet.

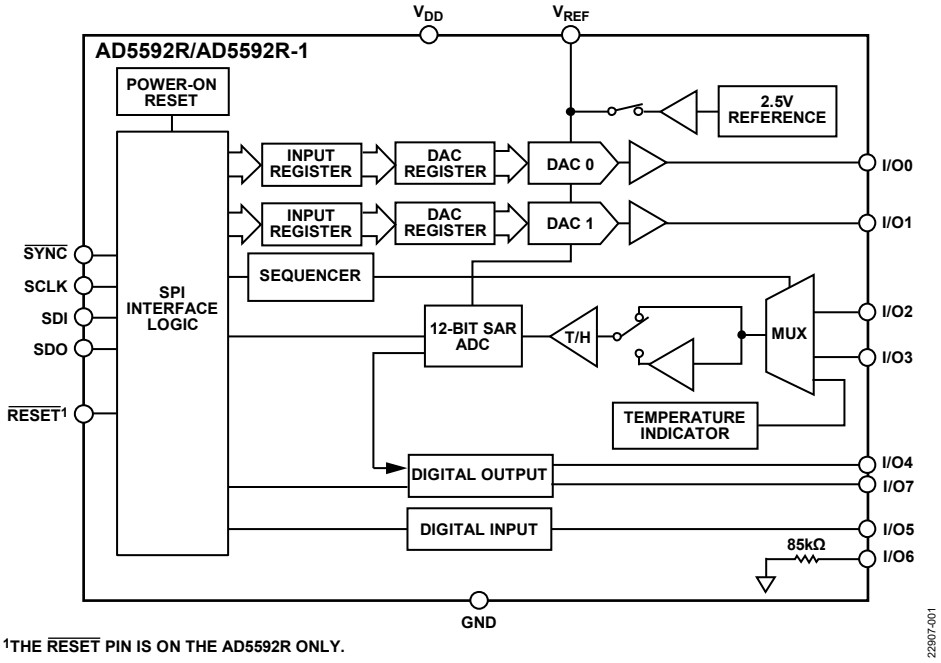

Figure 1. AD5592R/AD5592R-1 After Configuration

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REVISION HISTORY

1/2021—Revision 0: Initial Version

DEVICE PIN CONFIGURATION

The AD5592R/AD5592R-1 have 8-channel configurable analog and digital input and output ports. The AD5592R/AD5592R-1 have eight pins that can be independently configured as a 12-bit DAC output channel, a 12-bit ADC input channel, a digital input pin, or a digital output pin. The function of each pin is determined by programming the ADC, the DAC, or the GPIO configuration registers, as appropriate.

Table 1 and Figure 1 show a typical configuration where I/O0 and I/O1 are configured as DACs, I/O2 and I/O3 are configured as ADCs, I/O4 is configured as digital output, I/O5 is configured as digital input, and I/O6 remains in its default power-up state set as a pull-down with an 85 kΩ internal resistor connected to GND. I/O7 is configured as a $\overline{\text{BUSY}}$ signal to indicate when an ADC conversion is taking place on I/O2 or I/O3.

Table 1. I/Ox Pin Configuration

Channel	Output
I/O0	DAC
I/O1	DAC
I/O2	ADC
I/O3	ADC
I/O4	Digital output
I/O5	Digital input
I/O6	Pull-down with an 85 kΩ internal resistor connected to GND
I/O7	$\overline{\text{BUSY}}$ signal to indicate when an ADC conversion is taking place

SERIAL INTERFACE

The AD5592R/AD5592R-1 have a serial interface ($\overline{\text{SYNC}}$, SCLK, SDI, and SDO) that is compatible with serial port interface (SPI) standards, as well as with most digital signal processors (DSPs). The input shift register is 16 bits wide. The MSB (D15) determines what type of write function is required. When D15 is 0, a write to the control register is selected. The control register address is selected by D14 to D11. D10 and D9 are reserved and are 0s. D8 to D0 set the data that is written to the selected control register. When D15 is 1, data is written to a DAC channel (assuming that the channel was set to be a DAC). D14 to D12 select which DAC is addressed. D11 to D0 is the 12-bit data loaded to the selected DAC, with D11 being the MSB of the DAC data.

The SPI defines four transmission modes. The SPI master can typically support all four modes, but this support must be confirmed beforehand because sometimes the master is not compatible with a particular mode. The mode depends on the SCLK level, sometimes called polarity (CPOL), when the transmission initiates ($\overline{\text{CS}}$ or $\overline{\text{SYNC}}$ is pulled low) and the sampling edge, called phase (CPHA), as shown in Figure 2. See Application Note AN-1248 for a good introduction into the SPI and its various modes of operation. The SPI of the AD5592R/AD5592R-1 supports the transmission modes with CPOL = 0 and CPOL = 1 and with CPHA = 1.

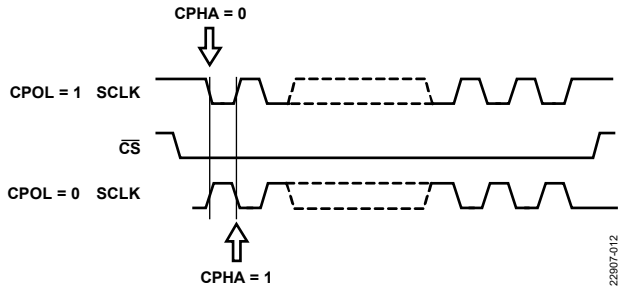

Figure 2. SPI Timing

A read or write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data on SDI is clocked into the 16-bit shift register on the falling edge of SCLK, and data on SDO is shifted out on the rising edge of SCLK. After the 16th falling clock edge, the last data bit is clocked in. $\overline{\text{SYNC}}$ is then brought high, and the programmed function executes. $\overline{\text{SYNC}}$ must be brought high for a minimum of 20 ns before the next read or write transaction. Refer to the AD5592R/AD5592R-1 data sheet for more details.

POWER-ON RESET

When power is applied to the AD5592R/AD5592R-1, the power-on reset (POR) block initializes the device and loads the registers with the default values. The device initialization process takes 250 µs. Do not write to any of the registers during this time.

After the POR sequence completes, configure the I/Ox channels using the SPI command detailed in Table 2.

Table 2. SPI Command to Configure the I/Ox Pins

	Register Write					
	MSB	Address	Reserved	Reserved/Enable $\overline{\text{BUSY}}$	[IO7:IO0]	
Command	D15	[D14:D11]	[D10:D9]	D8	[D7:D0]	Description
1	0	0101	00	0	0000 0011	To set the I/O0 and I/O1 pins as DACs.
2	0	0100	00	0	0000 1100	To set the I/O2 and I/O3 pins as ADCs.
3	0	1000	00	1	1001 0000	To set the I/O4 pin as a digital output and to configure I/O7 as a $\overline{\text{BUSY}}$ signal for the ADC conversion status.

	Register Write					
	MSB	Address	Reserved	Reserved/Enable $\overline{BUSY}$	[IO7:IO0]	
Command	D15	[D14:D11]	[D10:D9]	D8	[D7:D0]	Description
4	0	1010	00	0	0010 0000	To set the I/O5 pin as a digital input.
5	0	0110	00	0	0100 0000	To set the I/O6 pin as a pull-down with an 85 kΩ internal resistor connected to GND (default condition at power-up)

ADDITIONAL CONFIGURATIONS

After configuring the I/Ox pins with the values detailed in Table 1, select the voltage reference, DAC output voltage range, ADC input voltage range, and ADC internal buffer.

ADC Configuration

When configured as an ADC, the I/Ox pin connects to a 12-bit switched capacitor input, successive approximation register (SAR) ADC via an analog multiplexer. For more details on the SAR ADC architecture, see the MT-021 Tutorial. Configurable ADC features include selecting a voltage reference, input voltage range, and an internal buffer.

The AD5592R/AD5592R-1 have an integrated 2.5 V, 20 ppm/°C reference that is turned off by default. When the on-chip reference is powered up (using the EN_REF bit in the power-down/reference control register), the reference voltage appears on the V_{REF} pin. When the reference is powered down, an external reference must be connected to the V_{REF} pin. There is an ADC range bit in the general-purpose control register (as mentioned in Table 3), which sets the channel input range as 0 V to V_{REF} (gain = 1) or 0 V to 2 × V_{REF} (gain = 2), as shown in Figure 3 and Figure 4, respectively.

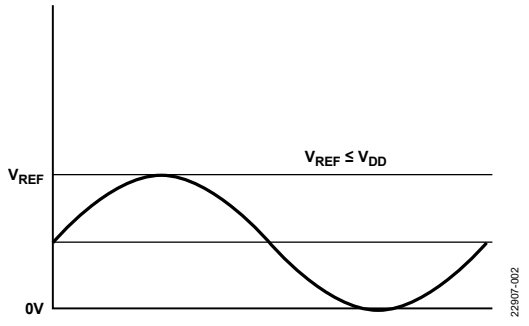

Figure 3. Input Voltage Range of the ADC with Gain = 1

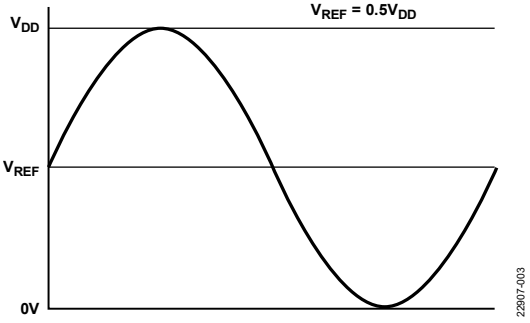

Figure 4. Input Voltage Range of the ADC with Gain = 2

The current flowing into the I/Ox pins configured as ADC inputs vary with the sampling rate (f_S), the voltage difference between successive channels (V_{DIFF}), and whether buffered or unbuffered mode is used. In buffered mode, the ADC internal buffer is enabled using the ADC buffer enable bit of the general-purpose control register. Figure 5 shows a simplified version of the ADC input structure. When a new channel is selected for conversion, the 5.8 pF capacitor must be charged or discharged of the voltage that was on the previously selected channel. The time required by the charge or discharge depends on the voltage difference between the two channels. This effects the input impedance of the multiplexer, and therefore, the input current flowing into the I/Ox pins.

In buffered mode, Switch S1 is open and Switch S2 is closed, in which case, the U1 buffer is directly driving the 23.1 pF capacitor, and its charging time is negligible. In unbuffered mode, Switch S1 is closed and Switch S2 is open. In unbuffered mode, the 23.1 pF capacitor must additionally be charged from the I/Ox pins, which contributes to the input current. For applications where the ADC input current is too high, an external input buffer may be required. The choice of buffer is a function of the particular application.

There is an option to precharge the ADC using the ADC buffer precharge bit of the general-purpose control register. When the selected channel is sampled for conversion, the precharge buffer technically helps to reduce the switching kickback from the SAR ADC. The precharge buffers are not full buffers and do not replace the external driver op amp(s). The analog input precharge buffers provide the initial charging of the internal switched capacitor network during the initial part of the sampling phase. For the remaining part of the sampling phase, the buffers are automatically bypassed, and the fine accuracy settling charge is provided by the external driver, which eases the driving requirement of the external op amp(s), and in some cases, allows lower power op amps to be used.

When using the internal ADC buffer, there is a dead band of 0 V to 5 mV, which means that the ADC performance is not accurate in this band. With the internal ADC buffer disabled, no dead band exists, and the input range of the ADC input is from 0 V to V_{REF}. Note that all ADC input channels share the same input range.

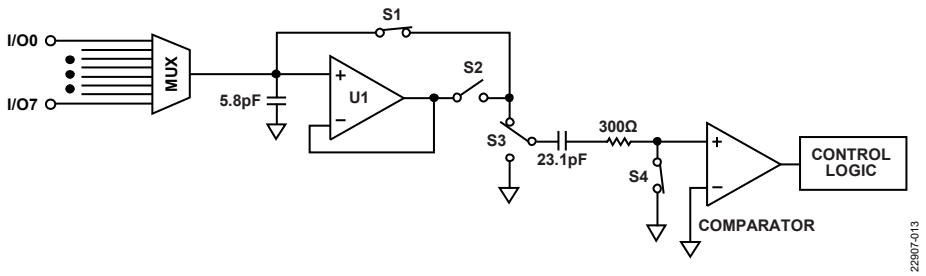

Figure 5. ADC Input Structure

DAC Configuration

When an I/Ox pin is configured as a DAC, the I/Ox pin is driven by a 12-bit segmented resistor string DAC with an internal output buffer. For more details on the DAC architecture, refer to the MT-014 Tutorial and MT-016 Tutorial. Configurable DAC features include voltage reference selection, output voltage range selection, the DAC power-down option, and the DAC update option.

The voltage reference selection feature is common for both the ADC and DAC configurations. The user must choose between an internal 2.5 V reference and an external reference using the EN_REF bit of the power-down/reference control register as shown in Table 4. Note that there is no option to separately choose a different reference input for the ADC and the DAC.

The DAC output voltage range can be configured to 0 V to V_{REF} (gain = 1) or 0 V to 2 × V_{REF} (gain = 2) using DAC range bit of the general-purpose control register, as shown in Figure 6 and Figure 7, respectively. When $V_{REF} = V_{DD}$, the 0 V to 2 × V_{REF} range does not allow the DAC to swing the output beyond V_{DD}.

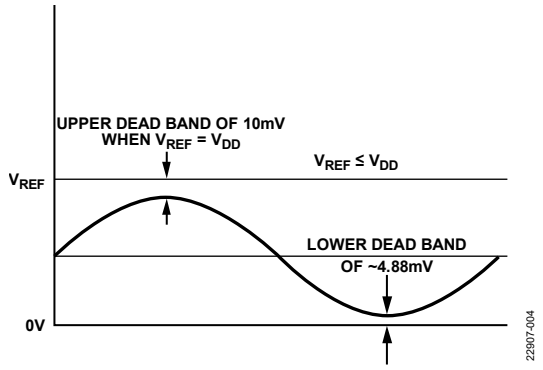

Figure 6. Output Voltage Range of the DAC with Gain = 1 (Unloaded Condition)

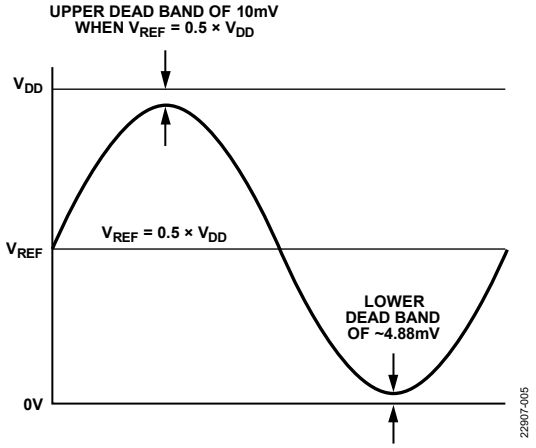

Figure 7. Output Voltage Range of the DAC with Gain = 2 (Unloaded Condition)

When $V_{REF} = V_{DD}$ for gain = 1 or $V_{REF} = 0.5 \times V_{DD}$ for gain = 2, there is an upper dead band of 10 mV at the DAC channel output in unloaded conditions. Additionally, there is a lower dead band of ~4.88 mV at the DAC channel output in unloaded conditions. When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the DAC channel. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.

It is possible to set the same I/Ox pin as both a DAC and an ADC. When an I/Ox pin is set as both a DAC and an ADC, the primary function is that of the DAC. If the I/Ox pin is selected for inclusion in an ADC conversion sequence, the voltage on the I/Ox pin is converted and made available via the SPI, allowing the DAC output voltage to be monitored.

Note that there is a power-down/reference control register available to reduce the power consumption when certain functions are not needed. The power-down/reference control register allows any channels set as DACs to be individually placed in a power-down state by using the PDx bits. When in a power-down state, the DAC outputs are three-state. When a DAC channel is set to normal mode, the DAC output returns to its previous value, which is programmed before the power-down state initiates.

There is no dedicated power-down function for the ADC as there is no power consumed by the ADC when the ADC is not in conversion. The PD_ALL bit simultaneously powers down the DACs, the internal reference, the ADC, and its buffer.

Table 3 and Table 4 detail the register configurations for an unbuffered ADC with a $2 \times V_{REF}$ input range and an internal reference, respectively. The selected DACs have a range of 0 V to V_{REF}, and each DAC is updated separately. An internal 2.5 V reference is used, and none of the ADC or DAC blocks are powered down.

Table 3. SPI Command to Configure the ADC Input Range and the DAC Output Range Through the General-Purpose Control Register

MSB	Address	Reserved	ADC Buffer Precharge	ADC Buffer Enable	Lock	All DACs	ADC Range	DAC Range	Reserved	
D15	[D14:D11]	D10	D9	D8	D7	D6	D5	D4	[D3:D0]	Description
0	0011	0	0	0	0	0	1	0	0000	Sets the ADC input range to (0 V – $2 \times V_{REF}$) and the DAC output range to (0 V – V_{REF})

Table 4. SPI Command to Enable the Internal Reference Through the Power-Down/Reference Control Register

MSB	Address	PD_ALL	EN_REF	Reserved	PD DACs	
D15	[D14:D11]	D10	D9	D8	[D7:D0]	Description
0	1011	0	1	0	00000000	Enable internal reference

DAC OPERATION

The AD5592R/AD5592R-1 contain eight 12-bit DACs. The DAC channels have a DAC range bit that sets the output range as 0 V to V_{REF} or 0 V to 2 × V_{REF} for all DAC channels. Because the output range bit is shared by all DAC channels, it is not possible to set the different output ranges on a per channel basis. The input coding to the DAC is straight binary. Use the following equation to calculate the ideal output voltage for the DAC:

$$V_{OUT} = G \times V_{REF} \times (D/2^N)$$

where:
G = 1 for an output range of 0 V to V_{REF} or 2 for an output range of 0 V to 2 × V_{REF}.
D is the decimal equivalent of the binary code (0 to 4095) that is loaded to the DAC register.
N = 12.

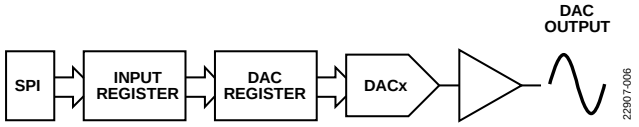

Figure 8. Transfer of Register Commands

The two registers that update the DAC to a specific value are the input register and the DAC register. Data is written to the selected DAC input register. Data written to the input register can be automatically copied to the DAC register, if required. Data is transferred to the DAC register based on the setting of the LDAC mode bits in the readback and LDAC mode register. There are three ways to update the DAC values based on the register values of the readback and LDAC mode and general-purpose control registers.

SINGLE CHANNEL UPDATE

When the LDAC mode bits (Bits[1:0]) of the readback and LDAC mode register are set to 00, new data is automatically transferred from the input register to the DAC register, and the analog output updates (see Table 5).

SYNCHRONOUS UPDATE

When the LDAC mode bits are set to 01, data remains in the input register. This LDAC mode allows writes to the input registers without affecting the DAC outputs. When the input registers are loaded, setting the LDAC mode bits to 10 transfers the values in the input registers to the DAC registers, and the DAC outputs are updated simultaneously (see Table 6, Table 7, and Table 8).

Table 5. SPI Command for Single Channel Update of the DAC Channels

MSB	Address	DAC Data	
D15	[D14:D12]	[D11:D0]	Description
1	000	011101100101	Updates the Channel 0 input register and the DAC register with a value of 0x765, and consequently, the DAC output updates.
1	001	111100001111	Updates the Channel 1 input register and the DAC register with a value of 0xF0F, and consequently, the DAC output updates.

Table 6. SPI Command for Synchronous Update of DAC Channels (Sequence 1)

MSB	Address	Reserved	REG_READBACK	LDAC Mode	
D15	[D14:D11]	[D10:D7]	[D6:D2]	[D1:D0]	Description
0	0111	0000	00000	01	Updates the LDAC mode register for synchronous updates.

Table 7. SPI Command for Synchronous Update of DAC Channels (Sequence 2)

MSB	Address	DAC Data	
D15	[D14:D12]	[D11:D0]	Description
1	000	0111 0110 0101	Updates the input register of Channel 0 with a value of 0x765.
1	001	1111 0000 1111	Updates the input register of Channel 1 with a value of 0xF0F.

Table 8. SPI Command for Synchronous Update of DAC Channels (Sequence 3)

MSB	Address	Reserved	REG_READBACK	LDAC Mode	
D15	[D14:D11]	[D10:D7]	[D6:D2]	[D1:D0]	Description
0	0111	0000	00000	10	Data is copied from the input register to the DAC register, and the DAC outputs are updated simultaneously.

ALL CHANNEL UPDATE

When the all DACs bit (D6) in the general-purpose control register is set to 1, for future DAC writes, the DAC address bits in the DAC write register are ignored, and all channels are configured as DACs are updated with the same data (see Table 9 and Table 10).

Table 9. SPI Command to Update All the DAC Channels (Sequence 1)

MSB	Address	Reserved	ADC Buffer Precharge	ADC Buffer Enable	Lock	All DACs	ADC Range	DAC Range	Reserved	
D15	[D14:D11]	D10	D9	D8	D7	D6	D5	D4	[D3:D0]	Description
0	0011	0	0	0	1	1	0	0	0000	Updates the general-purpose control register to update all DACs simultaneously with the same value.

Table 10. SPI Command to Update All the DAC Channels (Sequence 2)

MSB	Address	DAC Data	
D15	[D14:D12]	[D11:D0]	Description
1	XXX[1]	0010 1111 1111	Updates all DAC channels with a value of 0x2FF as an example.

[1] X means don't care.

ADC OPERATION

The 12-bit, single-supply ADC is capable of throughput rates of 400 kSPS. The ADC is preceded by a multiplexer that switches selected I/Ox pins to the ADC. A sequencer is included to automatically switch the multiplexer to the next selected channel.

Channels are selected for conversion by writing to the ADC sequence register. When the write to the ADC sequence register is completed, the first channel in the conversion sequence goes into track mode. Allow each channel to track the input signal for a minimum of 500 ns. The first $\overline{\text{SYNC}}$ falling edge following the write to the ADC sequence register begins the conversion of the first channel in the sequence. Each conversion takes 2 µs, and the conversion must be completed before another conversion is initiated.

Note that the data that appears on the SDO pin on the $\overline{\text{SYNC}}$ falling edge following the write to the ADC sequence register is invalid. The subsequent $\overline{\text{SYNC}}$ falling edge begins clocking out the ADC conversion result and also initiates the next conversion. ADC data is clocked out on SDO in a 16-bit frame as provided in Table 11. The ADC operates with one cycle latency, thus the conversion result corresponding to each conversion is available one serial read cycle after the cycle in which the conversion was initiated. While reading the ADC conversion result, do not perform any other read operation.

The ADC has an input range selection bit (ADC range bit in the general-purpose control register) that sets the input range as 0 V to V_{REF} (default) or 0 V to 2 × V_{REF}. All ADC channels share the same input range.

The ADC digital code is related to the ADC input voltage (V_{IN}) as follows:

$$V_{IN} = D \times G \times (V_{REF}/2^N)$$

where:
D is the digital code given by the ADC.
G = 1 for an output range of 0 V to V_{REF} or 2 for an output range of 0 V to 2 × V_{REF}.
N = 12.

$\overline{\text{BUSY}}$ SIGNAL (I/O7)

I/O7 can be configured as a $\overline{\text{BUSY}}$ signal (using the enable $\overline{\text{BUSY}}$ bit in the GPIO write configuration register) to indicate when an ADC conversion is taking place (see Table 12). Only I/O7 has the option to be configured as a $\overline{\text{BUSY}}$ output apart from the DAC, the ADC, or the GPIO. $\overline{\text{BUSY}}$ goes low while a conversion is in progress and high when an ADC conversion result is available. This $\overline{\text{BUSY}}$ indicator allows the SPI master to communicate with the AD5592R/AD5592R-1 for other channels that are configured as DACs or GPIOs and to monitor the $\overline{\text{BUSY}}$ signal to read out the ADC result when needed. If any ADC channels are not enabled for conversion in the ADC sequence register, I/O7 can be configured as a DAC or a GPIO for other system requirements.

SINGLE READ

Channel 2 and Channel 3 (the D4 and D5 bits) are selected in the ADC sequence register with the REP bit (D9) in the reset state. The ADC converts Channel 2 followed by Channel 3 sequentially in ascending order on successive $\overline{\text{SYNC}}$ falling edges. Once all the selected channels in the ADC sequence register are converted, the ADC conversion stops, and the ADC goes three-state. See Table 13 and Figure 9.

Table 11. ADC Conversion Result on SDO

MSB	Address	ADC Result
D15	**[D14:D12]**	**[D11:D0]**
0	ADC address[1]	12-bit ADC conversion result

[1] The ADC addresses are as follows: 000 = ADC0, 001 = ADC1, 010 = ADC2, … , 111 = ADC7.

Table 12. SPI Command to Configure I/O7 as $\overline{\text{BUSY}}$

MSB	Address	Reserved	Enable $\overline{\text{BUSY}}$	GPIO Data	
D15	**[D14:D11]**	**[D10:D9]**	**D8**	**[D7:D0]**	**Description**
0	1000	00	1	1001 0000	I/O7 configured as a $\overline{\text{BUSY}}$ signal and keeping I/O4 pin as output

Table 13. ADC Sequence Register for Start Single ADC Conversion

MSB	Address	Reserved	REP	TEMP	ADC Channels	
D15	**[D14:D11]**	**D10**	**D9**	**D8**	**[D7:D0]**	**Description**
0	0010	0	0	0	0000 1100	Enable Channel 2 and Channel 3 for conversion in ADC sequencer

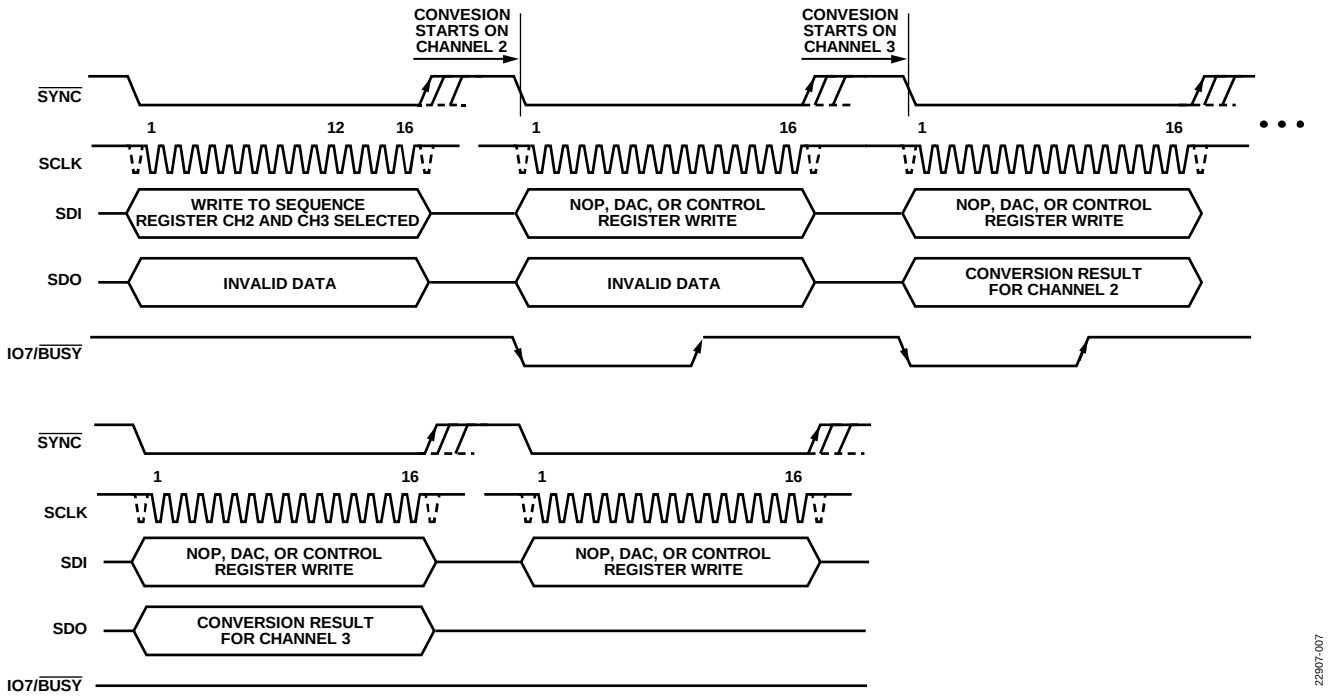

Figure 9. SPI Sequence for Single ADC Conversion of Channel 2 and Channel 3

REPEATED READ

To repeat ADC conversions, set the REP bit (D9) in the ADC sequence register. The ADC converts all selected channels sequentially in ascending order on successive $\overline{\text{SYNC}}$ falling edges. Once all the selected channels in the control register are converted, the ADC repeats the sequence as long as the REP bit is set. If the REP bit is clear, the ADC goes three-state, and the ADC conversion stops (see Table 14 and Figure 10).

Table 14. ADC Sequence Register for Starting and Stopping Repeated ADC Conversions

MSB	Address	Reserved	REP	TEMP	ADC Channels	
D15	[D14:D11]	D10	D9	D8	[D7:D0]	Description
0	0010	0	1	0	0000 1100	Enables Channel 2 and Channel 3 for repeated conversion in sequential order in the ADC sequencer.
0	0010	0	0	0	0000 0000	Stops the repeated ADC conversion and disables Channel 2 and Channel 3 for conversion.

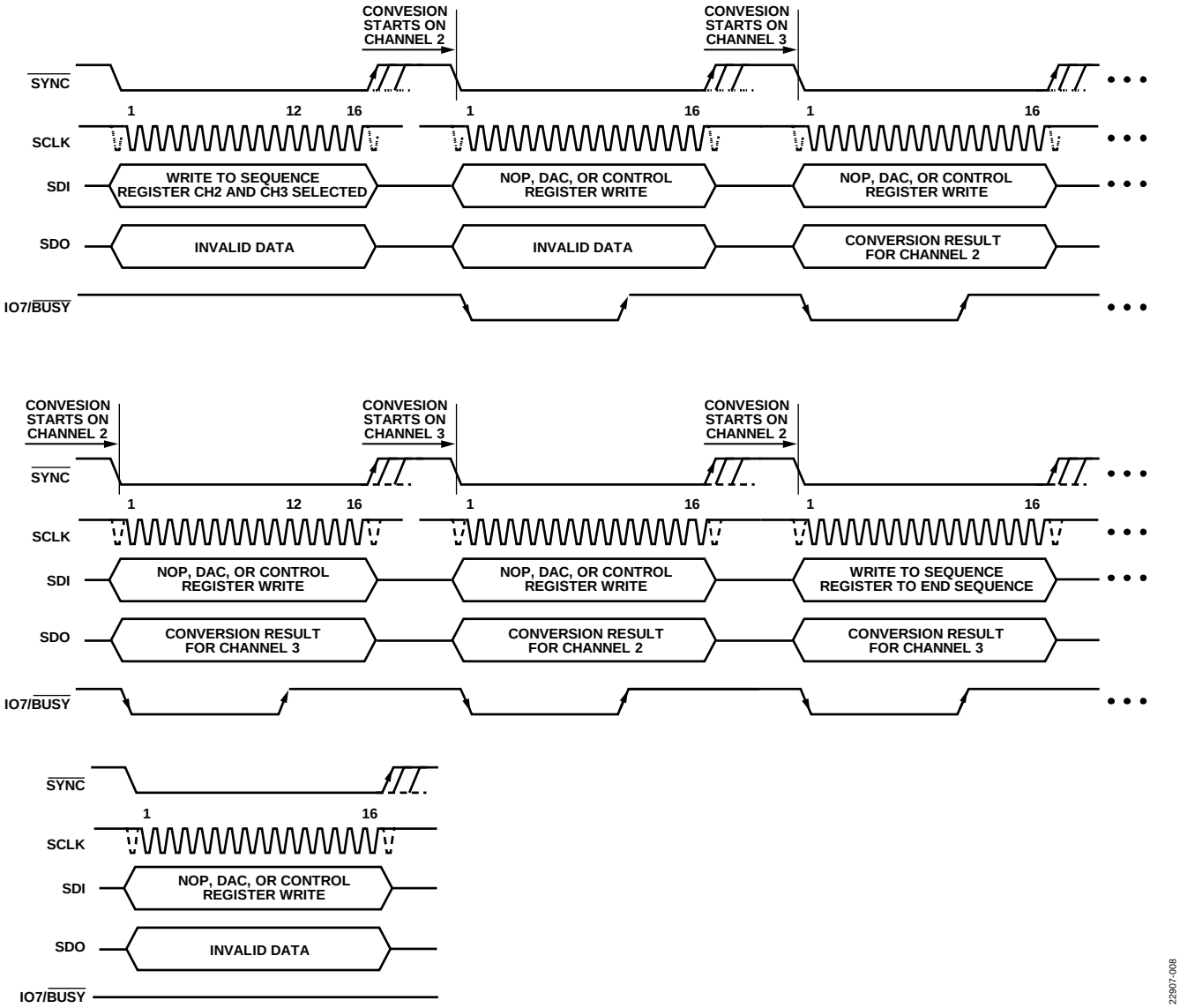

Figure 10. SPI Sequence for Repeated ADC Conversion of Channel 2 and Channel 3

TEMPERATURE READBACK

The AD5592R/AD5592R-1 contain an integrated temperature indicator that can be used for fault detection, where a sudden rise in die temperature can indicate a fault condition, such as a shorted output. Temperature indicator readback is enabled by setting the TEMP bit (D8) in the ADC sequence register to 1. The temperature result is then added to the ADC conversion sequence and has an address of [D15:D12] = 1000 (see Table 16). Ensure that this result, as detailed in Table 16, is not confused with readback conversion result from DAC0 channel. The temperature conversion takes 5 µs when the ADC buffer is enabled and 20 µs when the buffer is disabled.

To calculate the ADC temperatures for a gain of 1 and a gain of 2, use the following two equations:

For ADC gain = 1, use the following equation:

$$Temperature\ (°C) = 25 + \frac{\left(ADC\ Code - \left(0.5/V_{REF}\right) \times 4095\right)}{\left(2.654 \times \left(2.5/V_{REF}\right)\right)}$$

For ADC gain = 2, use the following equation:

$$Temperature\ (°C) = 25 + \frac{\left(ADC\ Code - \left(0.5/\left(2 \times V_{REF}\right)\right) \times 4095\right)}{\left(1.327 \times \left(2.5/V_{REF}\right)\right)}$$

The range of codes returned by the ADC with ADC gain = 1 when reading from the temperature indicator is approximately 645 to 1035, corresponding to a temperature between −40°C to +105°C. The accuracy of the temperature indicator, averaged over five samples, is typically 3°C.

Table 15. ADC Sequence Register for Temperature Readback

MSB	Address	Reserved	REP	TEMP	ADC Channels	
D15	[D14:D11]	D10	D9	D8	[D7:D0]	Description
0	0010	0	0	1	0000 1100	Enables temperature indicator readback and adds it to the ADC conversion sequence. Its result is available following the conversion of ADC Channel 2 and Channel 3.

Table 16. Temperature Indicator Readback

Address	ADC Result
[D15:D12]	[D11:D0]
1000	12-bit temperature indicator result

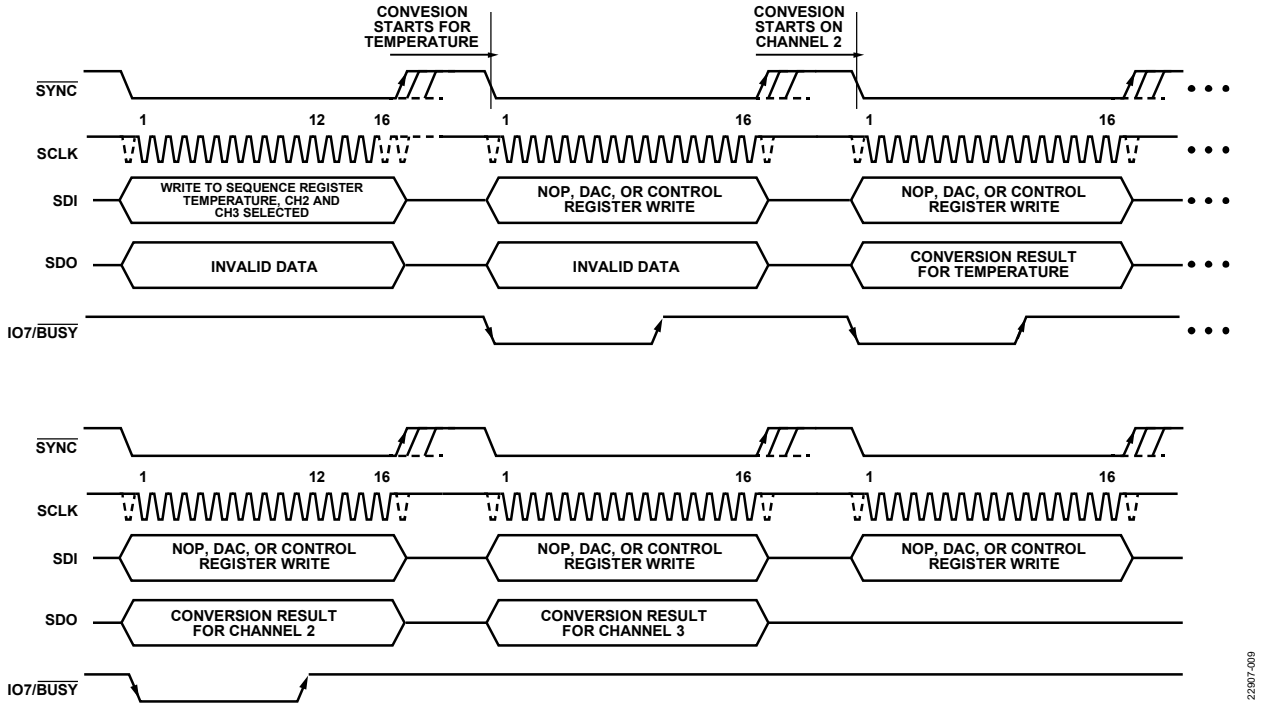

Figure 11. SPI Sequence for Single ADC Conversion of Channel 2 and Channel 3 Along with Internal Temperature

DIGITAL INPUT AND OUTPUT

The I/Ox pins of the AD5592R/AD5592R-1 can operate as a general-purpose, digital input, or digital output pin. The function of the I/Ox pins is determined by writing to the appropriate bit in the GPIO read configuration and GPIO write configuration registers.

DIGITAL OUTPUT

By default, the digital outputs are configured as push-pull outputs. The output is driven to V_{DD} or GND, as determined by the data in the GPIO write configuration register.

Using Command 3 in Table 2, I/O4 is configured as digital output. Table 17 provides the SPI command to set the digital output of the I/O4 pin as high (V_{DD}).

Open-Drain Output

To set any I/Ox pin as an open-drain output, set the appropriate data bit in the GPIO open-drain configuration register to 1. When in an open-drain configuration, the output is driven to GND when a data bit is set to 0 in the GPIO write data register. When the data bit value is 1, the output is not driven and is set to high impedance mode. The output must be pulled high by an external resistor. Figure 12 shows a simplified circuit diagram of an open-drain digital output.

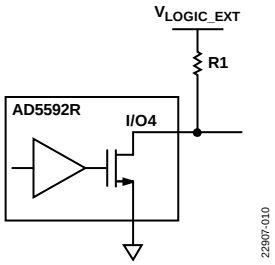

Figure 12. Open-Drain Digital Output Simplified Block Diagram

The open-drain configuration allows multiple output pins from different components to be tied together. If all pins are normally high, the open-drain configuration allows one pin to pull down all of the pins connected in the same line. This method is commonly used where multiple pins are used to trigger an alarm or an interrupt pin.

Table 18 provides the SPI command to configure I/O4 as open-drain and sets the output to high impedance mode.

DIGITAL INPUT

To set any I/Ox pin as a general-purpose input, set the appropriate bit in the GPIO read configuration register to 1.To read the state of the general-purpose inputs, write to the GPIO read configuration register.

When using Command 4 in Table 2, I/O5 is configured as a digital input. Table 19 provides the GPIO read configuration register value to read the status of I/O5 pin. Figure 13 shows the SPI sequence to read the digital status of I/O5 pin.

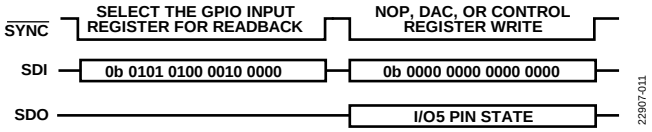

Figure 13. SPI Sequence to Readback the Status of the Digital Input Pin I/O5

Table 17. SPI Command to Set the Digital Output of I/O4

MSB	Address	Reserved	Enable $\overline{BUSY}$	Data	
D15	[D14:D11]	[D10:D9]	D8	[D7:D0]	Description
0	1001	00	0	0001 0000	Sets the output of I/O4 as high (V_{DD})

Table 18. SPI Commands to Configure the Digital Output I/O4 as Open-Drain.

MSB	Address	Reserved	Data	
D15	[D14:D11]	[D10:D8]	[D7:D0]	Description
0	1100	000	0001 0000	Open-drain output configuration for I/O4
0	1001	000	0001 0000	Sets the output of I/O4 to high impedance mode

Table 19. GPIO Read Configuration Register Value to Read the Status of the I/O5 Pin

MSB	Address	Enable Readback	Reserved	Data	
D15	[D14:D11]	D10	[D9:D8]	[D7:D0]	Description
0	1010	1	00	0010 0000	Configure I/O5 as a digital input and reads back its status in the next SPI frame

I/O CHANNELS AS THREE-STATE

The I/Ox pins can be set to three-state by writing to the three-state configuration register. When the I/Ox channel is set to three-state, the output assumes a high impedance state, which removes the output from the circuit. If more than one device is electrically connected to another device for the same I/O pins, putting an output into the high impedance state is often used to prevent short circuits or one device driving high (Logic 1) against another device driving low (Logic 0).

Table 20 shows the SPI command to configure the I/O1 to I/O4 pins to three-state mode and to exit three-state mode.

I/O CHANNEL AS 85 kΩ PULL-DOWN RESISTOR PINS

The I/Ox pins can be connected to GND via a 85 kΩ pull-down resistor by setting the appropriate bits in the pull-down configuration register. In the current configuration, the I/O6 pin has been configured as pull-down to GND using Command 5, as mentioned in Table 2. This feature is often used when connecting a switch or active low inputs to a microcontroller or other logic gates.

Table 20. SPI Command to Configure the I/O1 to I/O4 Pins to Three-State Mode and to Exit Three-State Mode

MSB	Address	Reserved	Data	
D15	[D14:D11]	[D10:D8]	[D7:D0]	Description
0	1101	000	0001 1110	Sets the I/O1 to I/O4 pins to three-state mode.
0	1101	000	0000 0000	Exits the I/O1 to I/O4 pins from three-state mode. The I/Ox function is determined by the pin configuration registers.