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APPLICATION NOTE

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Configuring the ADIN1200 Ethernet PHY

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INTRODUCTION

The ADIN1200 is a low power, low latency, robust 10 Mbps and 100 Mbps, Ethernet physical layer (PHY) device targeting harsh applications in industrial automation, factory automation, building automation, energy, time sensitive networking (TSN), and industrial Internet of Things (IoT). The ADIN1200 has been extensively tested for electromagnetic compatibility (EMC), electrostatic discharge (ESD), and robust performance for industrial applications. This design integrates an energy efficient Ethernet (EEE), a PHY device core with the associated common analog circuitry, input and output clock buffering, management interface and subsystem registers, media access control (MAC) interface, and control logic to manage the reset and clock control and pin configurations.

This application note gives an overview of the various managed configurations of the PHY core device of the ADIN1200 using its hardware configuration pins. This application note also provides some information on unmanaged configurations that are common in industrial Ethernet applications.

The details that follow provide a high level overview and should be used in conjunction with the ADIN1200 data sheet.

Multifunction pin names may be referenced by their relevant function only.

TABLE OF CONTENTS

REVISION HISTORY

4/2020—Revision 0: Initial Version

PHY DEVICE CORE OF THE ADIN1200

The ADIN1200 is compliant with the IEEE 802.3 Ethernet standard. The ADIN1200 can operate in unmanaged or managed applications using multilevel strapping and operates over a wide industrial temperature range (−40°C to +105°C). The ADIN1200 supports the following MAC interfaces:

- Media independent interface (MII)
- Reduced MII (RMII)
- Reduced gigabit MII (RGMII)

HARDWARE CONFIGURATION PINS

The ADIN1200 can operate in unmanaged or managed applications. In an unmanaged application when an Ethernet cable is connected, the PHY device core attempts to establish a link. No software intervention via the management interface (MDIO) is required to establish a link. Instead, the PHY device core configures itself based on the voltage levels of the various hardware pin configurations.

In a managed application, software is available to configure the PHY device core via the management interface (MDIO). In this case, it is possible to configure the PHY device core to enter software power-down after reset, such that the PHY can be configured before attempting linking.

The following functions are configurable from the ADIN1200 hardware pins:

- PHY address
- Forced or advertised PHY speed
- Software power-down mode after reset
- Downspeed enabled
- Energy detect power-down mode
- EEE enabled
- Automatic MDIX
- MAC interface selection (RGMII, RMII, or MII)

The hardware configuration pins are pins shared with functional pins. The voltage level on these pins are sensed when exiting from a reset. Some hardware configuration pins are multilevel sensed, and others are two-level sensed. Using two resistors, R_LO and R_HI (see Figure 1), four different voltage levels can be sensed (see Table 1). Only MODE_1 (low) and MODE_4 (high) are relevant to the two-level sense pins, and these modes are implemented with a 10 kΩ pull-down resistor or a 10 kΩ pull-up resistor, respectively. Note that LED_0 must be pulled up to the AVDD_3P3 rail rather than VDDIO.

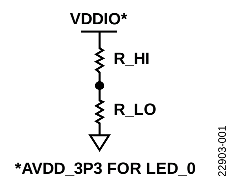

Figure 1. Hardware Configuration Pin Implementation

Note that the values listed in Table 1 assume no extra loading from circuitry external to the ADIN1200. It is likely that some configuration pins are connected to a field-programmable gate array (FPGA) inputs that can have their own internal pull-up or pull-down resistors, which load the resistor divider voltage. Assuming a pull-up resistor >43 kΩ and a pull-down resistor >37 kΩ, replace the 10 kΩ resistor used in MODE_1 and MODE_4 with a 2.5 kΩ resistor.

The voltage levels shown were chosen to steer clear of standard input high voltage (V_{IH}) and input low voltage (V_{IL}) levels to avoid any shoot through currents (and unknown voltage levels) in the input driver of disabled devices connected to the pins. V_{IH} and V_{IL} voltage levels do have voltage and device dependencies, and, therefore, it may not always be possible to avoid such artifacts.

The large resistor values recommended in Table 1 were chosen to minimize power consumption from the resistor ladder. Although, smaller value resistors can be used, but the user must maintain the same resistor ratios for the values used.

Table 1. Recommended Resistor Values

Mode	Low Resistor (R_LO)	High Resistor (R_HI)	Voltage Threshold
MODE_1	10 kΩ	Open	Not applicable
MODE_2	10 kΩ	56 kΩ	>0.1 × VDDIO[1]
MODE_3	56 kΩ	10 kΩ	>0.5 × VDDIO[1]
MODE_4	Open	10 kΩ	>0.9 × VDDIO[1]

[1] The supply rail for the LED_0 pin is AVDD_3P3 rather than VDDIO. Therefore, pull-up any pull-up on the LED_0 pin to AVDD_3P3.

MAC Interface Selection

The type of MAC interface can be configured using the MACIF_SEL1 pin (Pin 29) or the MACIF_SEL0 pin (Pin 28). These pins are two-level pins (only high or low) that have internal 45 kΩ pull-down resistors. However, external pull-down resistors can be used for stronger pull-down. Table 2 describes the MAC interface selection using the MACIF_SELx pins. In addition, refer to the ADIN1200 data sheet for the requirements for MAC interface selection.

Table 2. MAC Interface Selection

MAC Interface Selection	MACIF_SEL1	MACIF_SEL0
RGMII RXC/TXC 2 ns Delay	Low	Low
RGMII RXC Only 2 ns Delay	High	Low
MII	Low	High
RMII	High	High

PHY Address

The ADIN1200 has four PHY address pins available for configuring the PHY address: PHYAD_0 (Pin 27), PHYAD_1 (Pin 26), PHYAD_2 (Pin 24), and PHYAD_3 (Pin 23). These pins are shared with the RXD_0 to RXD_3 pins. The PHYAD_x pins are two-level configuration pins, which means that it is possible to configure the ADIN1200 to any of the 16 available PHY addresses. There are weak internal pull-down resistors on all PHYAD_x pins.

Speed Configuration

The PHY configuration pins, PHY_CFG0 (Pin 16) and PHY_CFG1 (Pin 20), are also shared pins with the functional pins. These pins have no internal pull-up resistors. Therefore, use external resistors to configure the appropriate function. These pins are multilevel sense pins, allowing four distinct voltage levels to be configured to provide a wider range configuration.

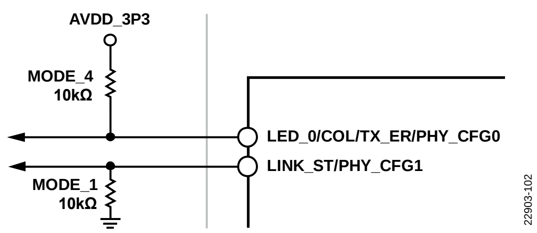

Figure 2. An Example Speed Configuration for PHY_CFGx

In Figure 2, the PHY_CFG1 has an external pull-down resistor configuring MODE_1 (0 V), while the PHY_CFG0 has a pull-up resistor configuring MODE_4 (3.3 V). This setting configures the PHY device for automatic negotiate with 10 Mbps with half duplex or full duplex and 100 Mbps with half duplex or full duplex advertised speeds. When connected to a link partner, the ADIN1200 links with the highest common speed.

Medium Dependent Interface Configuration

The medium dependent interface configuration is determined by the MDIX_MODE pin (Pin 21), which is also a shared function. The MDIX_MODE pin describes the interface from a physical layer implementation to the physical medium used to carry the transmission (straight or crossover). With a straight through cable, the cable must be set to MDI on one side and MDIX on the other side (see Figure 3). With a crossover cable, the cable can be either MDI or MDIX (see Figure 4).

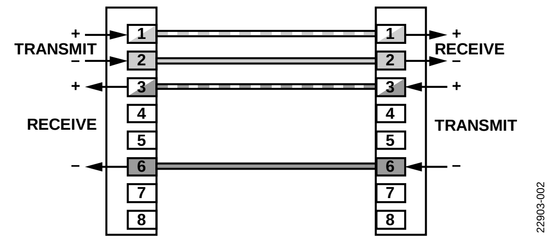

Figure 3. Straight Connection

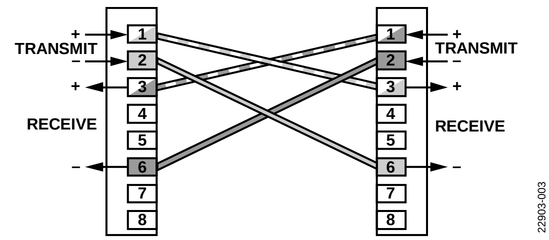

Figure 4. Crossover Connection

The MDIX_MODE pin does not have an internal pull-up. This pin is a multilevel sense pin. Therefore, there are four voltage level options available for this configuration using external resistors.

If automatic MDIX mode is enabled, the MDIX_MODE pin must be configured to MODE_3 or MODE_4 (see Table 3). These modes enable the device to automatically detect the appropriate MDI or MDIX configuration suited to the link partner.

Table 3. Automatic MDIX Configuration

Configuration	MDIX_MODE
Manual MDI	MODE_1
Manual MDIX	MODE_2
Automatic MDIX, Prefer MDIX	MODE_3
Automatic MDIX, Prefer MDI	MODE_4

When the MDIX_MODE pins have an external 3.3 V pull-up resistor, automatic MDI mode is selected. This mode enables the ADIN1200 to automatically detect the appropriate MDI or MDIX configuration suited to the link partner.

During automatic MDIX, each PHY transmits automatic negotiate pulses. Setting one PHY communication side as prefer MDI, and the other PHY communication side as prefer MDIX, controls which PHY starts sending pulses, and typically, results in a faster MDI and/or MDIX resolution. However, this setting still works as normal automatic MDIX even if the other side does not support prefer MDI or prefer MDIX. For additional information, refer to the ADIN1200 data sheet.

Pair swapping of the Ethernet pins are allowed in the ADIN1200 because of its automatic MDIX feature. Automatic MDIX swaps pairs automatically because a crossover cable is used, and it also considers the printed circuit board (PCB) layout and placement of the MDI_x_x pins (Pin 11 to Pin 14) of the PHY to the RJ45 of the Ethernet.

Table 4 details the MDI_x_x pins to the RJ45 of the Ethernet pairing with MDI mode and MDIX mode.

As an example, in Figure 5, 10BASE-T or 100BASE-Tx transmit on one pair and receive on the other. Therefore, in MDI mode, transmit is on MDI_x_x, Pair 0 (RJ45, Pin 1 and Pin 2) and receive is on MDI_x_x, Pair 1 (RJ45, Pin 3 and Pin 6), while in the MDIX mode, Pair 0 and Pair 1 swop. Therefore, a crossover cable must connect the PHYs together. If a straight through cable is used, the PHYs detect this and automatically swap Pair 0 and Pair 1 on the PHY.

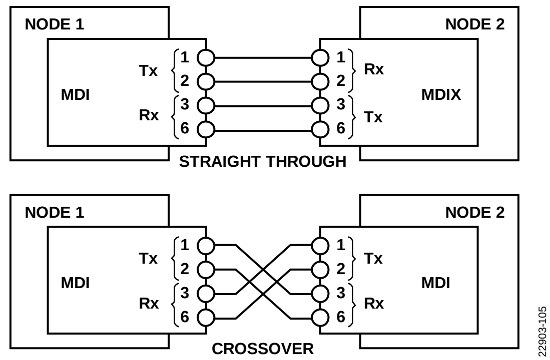

Figure 5. 10 BASE-T or 100BASE-Tx Pairing

Table 4. MDI_x_x Pins to RJ45 on 10 Mbps or 100 Mbps Pairing (See Figure 3, Figure 4, and Figure 5)

MDI_x_x Pin	RJ45 Pin	MDI Mode	MDIX Mode
MDI_0_P	1	Transmit±	Receive±
MDI_0_N	2	Transmit±	Receive±
MDI_1_P	3	Receive±	Transmit±
MDI_1_N	6	Receive±	Transmit±
MDI_2_P	4	Not used	Not used
MDI_2_N	5	Not used	Not used
MDI_3_P	7	Not used	Not used
MDI_3_N	8	Not used	Not used

HARDWARE CONFIGURATION EXAMPLES

This section details how to configure the ADIN1200 for common Ethernet PHY scenarios.

MANAGED APPLICATIONS

In managed applications, the host software configures the PHY at power-up. A managed configuration can be easily configured with a minimum set of external strapping resistors.

The example shown in Figure 6 provides the minimum configuration of strapping resistors and is the recommended configuration for a managed application.

RGMII, Advertised 100 Mbps or 10 Mbps with Half Duplex or Full Duplex, Downspeed, Energy Detect Power-Down (EDPD) Mode, and EEE Enabled

The example shown in Figure 6 shows the minimum set of strapping resistors suited for an RGMII managed application. The MAC interface configuration pins have pull-down resistors and default to the RGMII MAC interface. The PHY address pins also have pull-down resistors, therefore, the PHY address defaults to zero. To configure automatic MDIX, preferred MDI operation, add a pull-up resistor on GP_CLK.

In addition, it is recommended to have pull-up resistors on the LED_0 and LINK_ST pins and to configure these pins to the MODE_4 settings. It is also recommended to use an active low light emitting diode (LED) on LED_0.

The following summarizes an RGMII downspeed, EDPD mode, and EEE enabled configuration for managed applications:

- MAC interface = RGMII (default)
- MDIO_MODE = automatic MDIX, preferred MDI
  - MODE_4 (10 kΩ pull-up resistors)
- PHY address = 0b0000
- Speed selection = 10 Mbps or 100 Mbsp with full duplex or half-duplex, automatic negotiate enabled, downspeed, EDPD, and EEE
  - PHY_CFG0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - PHY_CFG1 = MODE_4 is configured using a 10 kΩ pull-up resistor

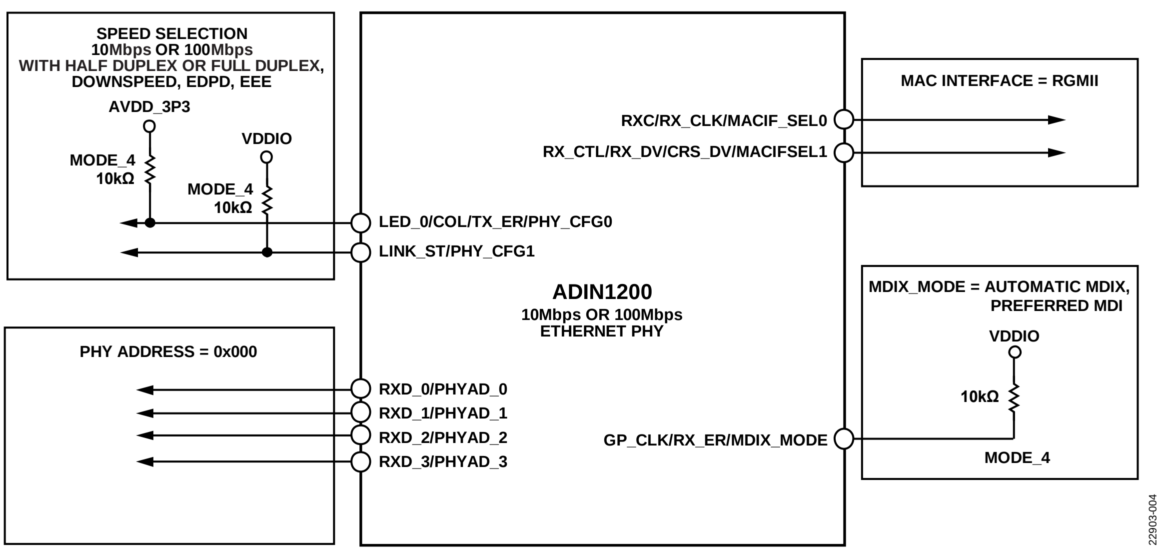

Figure 6. RGMII, Advertised 100 Mbps or 10 Mbps with Half Duplex or Full Duplex, Downspeed, EDPD Mode, and EEE Enabled Configuration for Managed Applications

MII, Advertised 100 Mbps or 10 Mbps with Full Duplex or Half Duplex

The following example details the pin configuration and resistors required external to the ADIN1200 for the MII MAC interface with auto negotiate enabled advertising all speeds:

- MAC interface = MII
  - MACIF_SEL0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - MACIF_SEL1 = MODE_1 is configured using a 10 kΩ pull-down resistor
- MDIX_MODE = automatic MDIX, preferred MDIX
  - MDIX_MODE = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)
- PHY address, as required
- Speed selection = 10 Mbps or 100 Mbps with full duplex or half duplex, automatic negotiate enabled
  - PHY_CFG0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - PHY_CFG1 = MODE_1 is configured using a 10 kΩ pull-down resistor

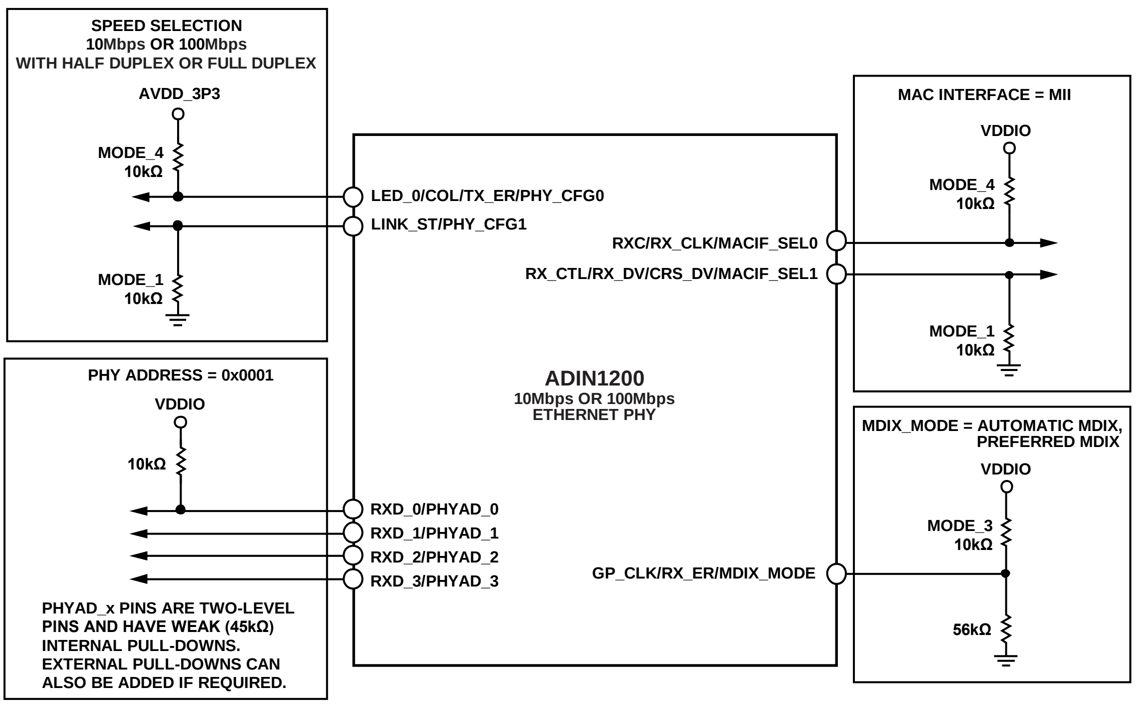

Figure 7. MII, Advertised 100 Mbps or 10 Mbps with Full Duplex or Half Duplex Configuration for Managed Application

UNMANAGED APPLICATION

In unmanaged applications, the ADIN1200 latches the configuration based on the voltage levels acquired during bootstrap. These voltage values are read during power-up or hardware reset and are latched. Then, the PHY immediately attempts to bring up links as configured by the configuration pins. More information about unmanaged applications can be found in the ADIN1200 data sheet.

RMII, Advertised 100 Mbps with Full Duplex

The following example details the pin configuration and resistors required external to the ADIN1200 for the RMII MAC interface with auto negotiate enabled advertising 100 Mbps with full duplex speed:

- MAC interface = RMII
  - MACIF_SEL0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - MACIF_SEL1 = MODE_4 is configured using a 10 kΩ pull-up resistor
- MDIX_MODE = automatic MDIX, preferred MDIX
  - MDIX_MODE = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)
- PHY address, as required
- Speed selection = 100 Mbps with full duplex, auto negotiate enabled
  - PHY_CFG0 = MODE_1 is configured using a 10 kΩ pull-down resistor
  - PHY_CFG1 = MODE_4 is configured using a 10 kΩ pull-up resistor

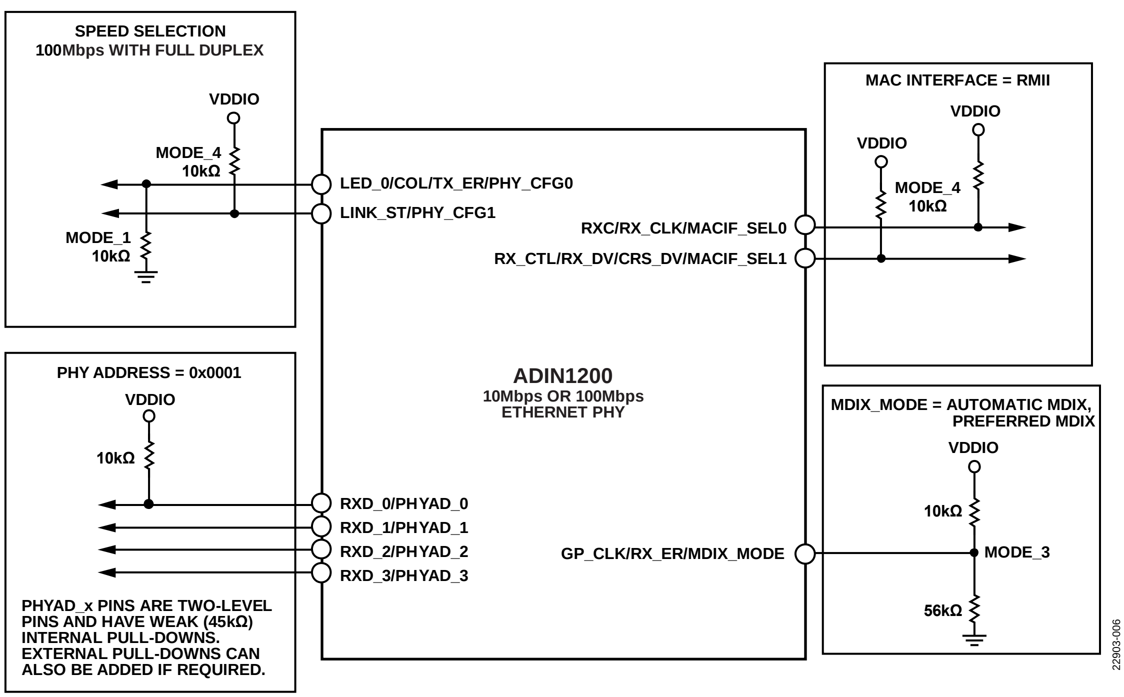

Figure 8. RMII, Advertised 100 Mbps with Full Duplex Configuration for Unmanaged Application

RMII, Forced 100 Mbps with Full Duplex

The following example details the pin configuration and resistors required external to the ADIN1200 for the RMII MAC interface with forced advertising, 100 Mbps with full duplex speeds:

- MAC interface = RMII
  - MACIF_SEL0 = MODE_4 is configured using a 10 kΩ pull-up resistor
  - MACIF_SEL1 = MODE_4 is configured using a 10 kΩ pull-up resistor
- MDIX_MODE = manual MDI
  - MDIX_MODE = MODE_1 (10 kΩ pull-down resistors)
- PHY address, as required
- Speed selection = 100 Mbps with full duplex, forced
  - PHY_CFG0 = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)
  - PHY_CFG1 = MODE_3 (10 kΩ pull-up resistor and 56 kΩ pull-down resistor)

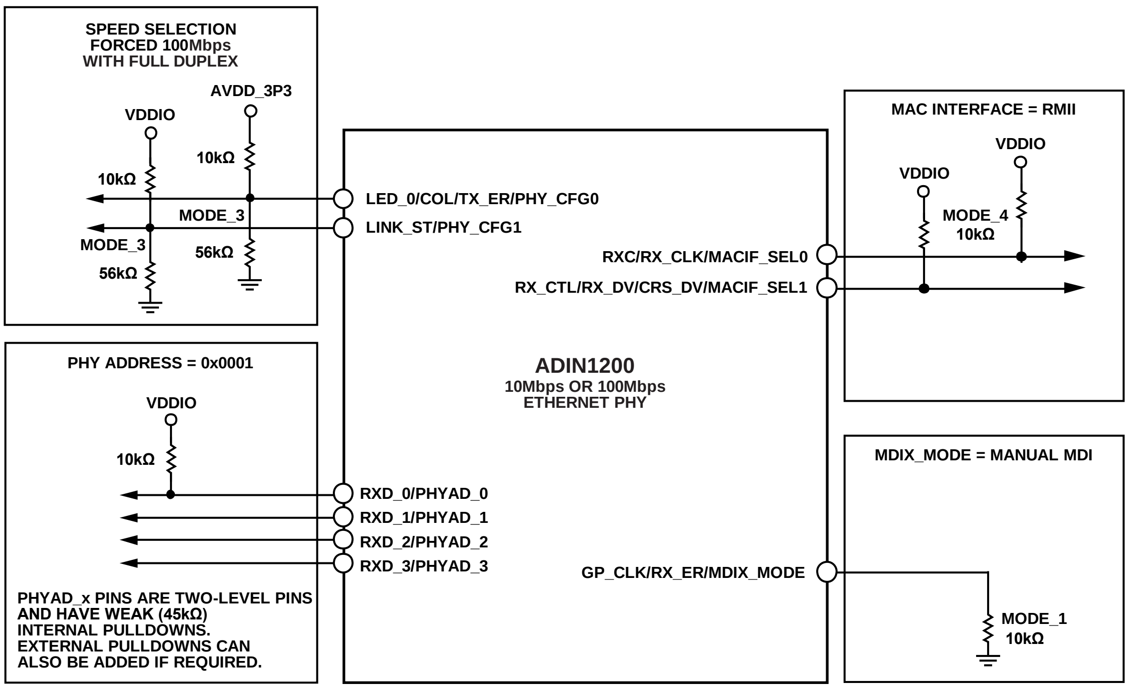

Figure 9. RMII, Forced 100 Mbps with Full Duplex Configuration for Unmanaged Application

CONCLUSION

The ADIN1200 Ethernet PHY can be configured on different MAC interfaces, speeds, and transmission mediums. The examples discussed in this application note tackle common application configurations for the ADIN1200 Ethernet PHY in the industrial Ethernet market. If software intervention is performed on the PHY, the configurations listed in the unmanaged applications section can also be used on managed applications.

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