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APPLICATION NOTE

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Enabling IEEE 802.15.4g-2012 Packet Mode in ADF7030-1

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INTRODUCTION

This application note describes how to enable the IEEE 802.15.4g-2012 compliant packet mode for the ADF7030-1 transceiver IC through a firmware download module. The firmware download module adds the following features to the ADF7030-1:

- Gaussian filtering
- Solution for incorrect 2-byte cyclic redundancy check (CRC) generation and detection when payload is less than 4 bytes long
- LSB first payload bytes transmission or reception
- Receiver physical layer (PHY) header (PHR) event when enabled
- Receiver block event when enabled

The firmware download module also enables the ADF7030-1 to use IEEE 802.15.4g-2012 functionalities, specifically mode switch disabled packet transmission or reception, LSB payload transmission or reception, forward error correction (FEC) encoding, frame check sequence (FCS), and data whitening.

This application note can also be used as a supplementary document in understanding the IEEE 802.15.4g-2012 functionality supported by the ADF7030-1.

TABLE OF CONTENTS

REVISION HISTORY

3/2021—Revision 0: Initial Version

IEEE 802.15.4G-2012 PACKET MODE REGISTERS

The registers used in IEEE 802.15.4g-2012 packet mode are summarized in Table 1.

Table 1. IEEE 802.15.4g-2012 Packet Mode Registers

Address	Register Name	Bit(s)	Bit Name	Description
0x200002F4	PROFILE_PACKET_CFG	[31:16]	GENERATED	Generated by the ADF7030-1 design center
		[15:14]	TYPE_FRAME0	0: generic packet
				1: IEEE 802.15.4g-2012 packet[1]
		[13:0]	GENERATED	Generated by the ADF7030-1 design center
0x200004F4	GENERIC_PKT_BUFF_CFG0	[31:25]	GENERATED	Generated by the ADF7030-1 design center
		[24]	ROLLING_BUFF_EN	0: rolling buffer mode disabled
				1: rolling buffer mode enabled
		[23]	GENERATED	Generated by the ADF7030-1 design center
		[22]	BIT2AIR	0: MSB first
				1: LSB first[1]
		[21:11]	PTR_TX_BASE	Transmitter base buffer offset pointer
		[10:0]	PTR_RX_BASE	Receiver base buffer offset pointer
0x200004FC	GENERIC_PKT_FRAME_CFG0	[31:30]	GENERATED	Generated by the ADF7030-1 design center
		[29:24]	CRC_LEN	16: 1-byte FCS
				32: 2-byte FCS
		[23:22]	GENERATED	Generated by the ADF7030-1 design center
		[21:16]	SYNC0_LEN	Length of Sync Word 0 in bits
		[15:8]	GENERATED	Generated by the ADF7030-1 design center
		[7:0]	PREAMBLE_LEN	Number of preamble units
0x20000500	GENERIC_PKT_FRAME_CFG1	[31:24]	TRX_IRQ1_TYPE	Select sources of interrupt on IRQ_OUT1
		[23:16]	TRX_IRQ0_TYPE	Select sources of interrupt on IRQ_OUT0
		[15:13]	GENERATED	Generated by the ADF7030-1 design center
		[12]	PREAMBLE_UNIT	0: bit pairs
				1: octets[1]
		[11:0]	PAYLOAD_SIZE	Number of payload bytes (generic packet only)
0x20000504	GENERIC_PKT_FRAME_CFG2	[31:24]	ENDEC_MODE	0x08: FEC enabled
				0x00: FEC disabled
		[23:16]	PREAMBLE_VAL	0x55: Preamble value of 0x55
		[15:14]	GENERATED	Generated by the ADF7030-1 design center
		[13:12]	LEN_SEL	Size of the length field
				00: fixed length mode, no length field in the packet[1]
				01: length field is 8 bits
				10: length field is 16 bits
		[11]	CRC_SHIFT_IN_ZEROS	Determines if the final register value is reversed. Set 1 for IEEE 802.15.4g-2012 packet
		[10:9]	GENERATED	Generated by the ADF7030-1 design center
		[8:3]	SYNC1_LEN	Length of Sync Word 1 in bits
		[2:0]	GENERATED	Generated by the ADF7030-1 design center
0x20000508	GENERIC_PKT_FRAME_CFG3	[31:16]	RX_LENGTH	Received PHR
		[15:0]	GENERATED	Generated by the ADF7030-1 design center
0x20000510	GENERIC_PKT_FRAME_CFG5	[31:16]	GENERATED	Generated by the ADF7030-1 design center
		[15:0]	TX_PHR	PHR used in IEEE 802.15.4g-2012 packet transmission
0x20000514	GENERIC_PKT_SYNCWORD0	[31:0]	VAL	0x6F4E: SFD for FEC encoded packet
0x20000518	GENERIC_PKT_SYNCWORD1	[31:0]	VAL	0x904E: SFD for nonFEC encoded packet
0x2000051C	GENERIC_PKT_CRC_POLY	[31:0]	VAL	0x1021: 1-byte FCS
				0x04C11DB7: 2-byte FCS
0x20000520	GENERIC_PKT_CRC_SEED	[31:0]	VAL	0x0: 1-byte FCS
				0x46AF6449: 32-bit FCS

Address	Register Name	Bit(s)	Bit Name	Description
0x20000524	GENERIC_PKT_CRC_FINAL_XOR	[31:0]	VAL	0x0: 1-byte FCS 0xFFFFFFFF: 2-byte FCS

[1] Used in IEEE 802.15.4g-2012 packet mode

IEEE 802.15.4G-2012 PACKET STRUCTURE

The ADF7030-1 supports specifications defined in the IEEE 802.15.4g-2012 standard for low rate wireless smart utility network (SUN).

PACKET STRUCTURE

The ADF7030-1 packet structure follows the PHY protocol data unit (PPDU) format with the mode switch disabled. Table 5 shows an example PPDU format. The ADF7030-1 does not support PPDU format with the mode switch.

The PPDU consists of three main fields: synchronization header (SHR), PHR, and PHY service data unit (PSDU).

SYNCHRONIZATION HEADER (SHR)

The SHR consists of two fields, the preamble and the start frame delimiter (SFD), as shown in Table 2.

Table 2. Synchronization Header

SHR	Size
Preamble	4 to 255 bytes of 0x55
SFD	2 bytes

Preamble

The preamble contains multiples of the 8-bit sequence 01010101. The ADF7030-1 supports transmission of the preamble sequence from 4 bytes up to 255 bytes.

Start Frame Delimiter (SFD)

The SFD is a 2-byte sequence selected from one of the two values shown in Table 3. The SFD determines whether the FEC is applied in the PHR and the PSDU. The FEC encoding adds bit redundancies in the PHR and the PSDU for error correction in the receiver side.

The SFD value for an FEC encoded PHR and PSDU is 0x6F4E, while the SFD value for an unencoded PHR and PSDU is 0x904E.

Table 3. Start Frame Delimiter Values

Description	SFD Value
FEC coded PHR and PSDU	0x6F4E
FEC uncoded PHR and PSDU	0x904E

PHY HEADER (PHR)

The PHR is a 2-byte sequence. Each bit field is shown in Table 4 and defined in the subsequent sections.

Table 4. PHY Header

PHR	Bits
Mode switch	Bit 15
Reserved	Bits[14:13]
FCS type	Bit 12
Data whitening	Bit 11
Length	Bits[10:0]

Mode Switch

The mode switch is used to enable a device to change its modulation scheme and/or data rate on a packet by packet basis. Because the ADF7030-1 does not support PPDU with the mode switch enabled, set this bit to 0 to indicate that packet transmission and reception takes place over a single data rate and modulation scheme.

FCS Type

The FCS type field of the PHR indicates the length of the FCS field included in the PSDU. If the FCS type is set to 1, the FCS is 2 bytes. Otherwise, the FCS is 4 bytes. The ADF7030-1 automatically generates the FCS based on the FCS type in transmit mode and checks the received FCS based on the received FCS type in the PHR during receive mode.

Data Whitening

Data whitening ensures that the data transmitted over the air are dc free, which gives a smooth power distribution over the occupied RF bandwidth. The data whitening bit in the PHR indicates whether the PSDU is whitened or not. If this bit is set to 1, the PSDU is whitened. Otherwise, the PSDU is not whitened. Data whitening is not applied in the SHR and the PHR.

On the receiver side, data dewhitening is employed if the received PHR bit indicates that the PSDU has been whitened on the transmitter side.

Length

Bits[10:0] indicate frame length, which is the length of the PSDU before the FEC encoding (if enabled). This field is equal to the length of the payload and the FCS in bytes. Note that the FCS depends on the setting of the FCS type, which can be 2 bytes or 4 bytes.

PHY SERVICE DATA UNIT (PSDU)

The PSDU field carries the data of the PPDU. The PSDU contains 2 fields, the payload and the FCS. The FCS is either 2 bytes or 4 bytes depending on the FCS type field of the PHR.

Table 5. PPDU Format Example

SHR		PHR					PSDU	
Preamble	SFD	Mode Switch	Reserved	FCS Type	Data Whitening	Length	Payload	FCS
4 Bytes to 255 Bytes of 0x55	10010000010011100	0	00	1	1	000000100000	Whitened	Whitened and 16-bit or 32-bit

CONFIGURING THE ADF7030-1

The following sections describe how to configure the ADF7030-1 to use IEEE 802.15.4g-2012 packet mode, as well as the events generated by the ADF7030-1

The registers and bits discussed in this section are described in the IEEE 802.15.4g-2012 Packet Mode Registers section. Detailed information on the registers can be found in the ADF7030-1 Software Reference Manual.

GENERAL CONFIGURATION

Only two-level Gaussian frequency shift keying (2GFSK) modulation with the bandwidth time (BT) product = 0.5 is supported for data rates up to 200 kbps. Refer to the ADF7030-1 Software Reference Manual on how to properly configure the ADF7030-1 radio parameters.

Configure the ADF7030-1 in the PHY_OFF state. After writing the configurations in the PHY_OFF state, the CMD_CFG_DEV command must be called to apply the configurations.

The following configurations are used to initialize the ADF7030-1 for IEEE 802.15.4g-2012 packet mode.

To enable IEEE 802.15.4g-2012 PPDU format, set the TYPE_FRAME0 bit of the ADF7030-1 to 1.

Preamble

Configure the preamble as follows, in no particular order:

- Set the PREAMBLE_VAL bits to 0x55.
- Set the PREAMBLE_UNIT bit to 1.
- Set the PREAMBLE_LEN bits to the desired number of preamble bytes (4 to 255).

In transmit mode, the ADF7030-1 generates the preamble detect event when the first bit of the preamble transmits and generates the preamble gone event when the last bit of the preamble shifts out. In receive mode, the ADF7030-1 generates the preamble detect event when the ADF7030-1 detects a preamble sequence and generates the preamble gone event when the preamble sequence is gone.

SFD

Configure the SFD as follows, in no particular order:

- Write 0x6F4E in the GENERIC_PKT_SYNCWORD0 register.
- Set the SYNC0_LEN bits to 16.
- Write 0x904E in the GENERIC_PKT_SYNCWORD1 register.
- Set the SYNC1_LEN bit to 16.

PSDU

Write the correct CRC settings based on the FCS type as shown in Table 6.

Table 6. ADF7030-1 CRC Settings

Register	Bits	16-Bit FCS	32-Bit FCS
GENERIC_PKT_FRAME_CFG0	CRC_LEN	16	32
GENERIC_PKT_CRC_POLY	VAL	0x1021	0x04C11DB7
GENERIC_PKT_CRC_SEED	VAL	0x0000	0x46AF6449
GENERIC_PKT_FRAME_CFG2	CRC_SHIFT_IN_ZEROS	1	1
GENERIC_PKT_CRC_FINAL_XOR	VAL	0x0000	0xFFFFFFFF

TRANSMIT MODE CONFIGURATIONS

The following sections describe additional configurations needed in transmitting the IEEE 802.15.4g-2012 packets.

SFD

To enable the FEC encoding in transmit mode, set the ENDEC_MODE bits in the GENERIC_PKT_FRAME_CFG2 register to 0x08. The ADF7030-1 transmits the SFD sequence in the GENERIC_PKT_SYNCWORD0 register with the MSB first out and then transmits an FEC encoded PHR and PSDU.

To disable the FEC encoding, set the ENDEC_MODE bits in the GENERIC_PKT_FRAME_CFG2 register to 0x00. The ADF7030-1 transmits the SFD sequence in the GENERIC_PKT_SYNCWORD1 register with the MSB first out and then transmits an unencoded PHR and PSDU.

The ADF7030-1 generates the sync detect event after the last bit of the SFD sequence transmits.

PHR

The PHR that is chosen to transmit is written to the TX_PHR bits. The PHR transmits with the MSB (Bit 15) first. It is not necessary to set the LEN_SEL bits in transmit mode.

The ADF7030-1 generates the length field pattern event after the last bit of the PHR field transmits.

PSDU

The PSDU is comprised of the payload and the FCS. However, because the ADF7030-1 supports FCS generation and checking, only the payload must be written to or read from the ADF7030-1 payload memory.

The user must write the payload to the ADF7030-1 transmitter payload buffer. Refer to the ADF7030-1 Software Reference Manual on how to write payload bytes to the payload memory.

The ADF7030-1 transmits the payload bytes starting from the lowest location in the transmitter payload buffer. The order of the bits transmitted over the air in each byte depends on the BIT2AIR bit. Set the BIT2AIR bit to 1 for LSB transmission of each payload byte. Note that each payload byte must be written to the payload memory as MSB first, and the ADF7030-1 transmits each payload byte as LSB first.

The ADF7030-1 generates the FCS based on the FCS type setting in the TX_PHR bits. The generated FCS then becomes part of the PSDU transmitted over the air.

The ADF7030-1 generates the payload and the CRC events when the last bit of the PSDU transmits. The payload event is not generated if the payload is truncated or if the transmitter is aborted. The ADF7030-1 also generates the end of frame (EOF) event after the PA ramps down following a complete packet transmission or the termination of the transmission caused by a radio command that triggers an exit from the transmit mode.

RECEIVE MODE CONFIGURATIONS

The following sections describe additional configurations needed in receiving the IEEE 802.15.4g-2012 packets.

SFD

If the incoming SFD matches the SFD sequence in the GENERIC_PKT_SYNCWORD0 register, the PHR and PSDU are treated as FEC encoded and the ADF7030-1 FEC decodes these fields. If the incoming SFD matches the SFD sequence in the GENERIC_PKT_SYNCWORD1 register, the PHR and PSDU are treated as unencoded. The first bit received over the air is treated as the MSB of the received SFD.

The ADF7030-1 generates the sync detect event after the incoming SFD matches the SFD sequence stored in the GENERIC_PKT_SYNCWORD0 register or the GENERIC_PKT_SYNCWORD1 register.

PHR

To receive the IEEE 802.15.4g-2012 packets, the LEN_SEL bits must be set to 0. The received PHR (FEC decoded if enabled) is stored in the RX_LENGTH bits. The first PHR bit received over the air is treated as the MSB of the stored PHR.

The ADF7030-1 generates the length field pattern event after completely receiving the PHR field.

PSDU

The ADF7030-1 stores the received PHY payload (FEC decoded and dewhitened) in the receiver payload buffer. Refer to the ADF7030-1 Software Reference Manual on how to read payload bytes from the payload memory.

The received FCS is not stored as part of the PHY payload. Instead, the ADF7030-1 checks the received PHR to identify the incoming FCS type and internally generates an FCS over the received PHY payload to compare against the received FCS.

The ADF7030-1 stores the received payload bytes, starting from the lowest location in its receiver payload buffer. That is, the first received payload byte is stored in the first receiver buffer location. The order of the bits received over the air in each byte depends on the BIT2AIR bit. Set the BIT2AIR bit to 1 for each payload byte to be treated as LSB first.

The ADF7030-1 generates the payload event when the complete PSDU is received. If the received FCS matches that calculated over the received PSDU, the ADF7030-1 also generates the CRC event. The ADF7030-1 also generates the EOF event after the full packet is received or receive mode is aborted by a radio command that causes an exit from the receive mode.

IEEE 802.15.4G-2012 PPDU EXAMPLE

As an example, consider the transmission of the following frame with a 3-byte payload with 4-byte FCS nonFEC encoded: Payload: 0x02, 0x00, 0x6A.

Generating the SHR

To transmit an SHR with a 4-byte preamble sequence, set the ADF7030-1 as follows:

- PREAMBLE_VAL bits = 0x55
- PREAMBLE_UNIT bit = 1
- PREAMBLE_LEN bits = 4

The SFD sequence taken for an unencoded frame is 0x904E, while 0x6F4E is the SFD sequence for the FEC encoded SFD. Set the SFD settings for the ADF7030-1 as follows:

- GENERIC_PKT_SYNCWORD0 register = 0x6F4E
- SYNC0_LEN bits = 16
- GENERIC_PKT_SYNCWORD1 register = 0x904E
- SYNC1_LEN bits = 16
- ENDEC_MODE bits = 0x0 to disable FEC encoding

The over the air bit sequence for this SHR is 0x55555555904E with the left-most bit transmitted first over time.

Generating the PHR

Because a 4-byte FCS is desired, the FCS type bit is set to 0. To disable data whitening, Bit 11 of the PHR is also set to 0. Frame length = payload size + FCS size, which is 7. Always clear the remaining reserved fields. The resulting PHR bytes are given as 0x0007. Write 0x0007 to the TX_PHR bits.

Table 7. PHR

PHR Field	Value
Mode Switch	0
Reserved	00
FCS Type	0
Data Whitening	0
Length	00000000111

The over the air bit sequence for this PHR is given as 0x0007 with the left-most bit transmitted first over time.

Generating the PSDU

When the frame is written in the transmitter payload buffer, the frame is laid out in the payload memory as shown in Table 8.

Table 8. Payload

Payload Memory	Payload
ADDR_MEM_0	0x02
ADDR_MEM_1	0x00
ADDR_MEM_2	0x6A

Set the BIT2AIR bit in the GENERIC_PKT_BUFF_CFG0 register to 1. The ADF7030-1 transmits each payload byte LSB first, and the over the air bit sequence of the PSDU is 0x4000565D29FA28, as seen in Table 9.

Table 9. PSDU

Payload	FCS
0x400056	0x5D29FA28

TEST CONDITIONS

Table 10. Receiver Performance

Parameter	Typical Specification	Test Conditions/Comments
Sensitivity, 4-Byte Preamble	−109.6 dBm	50 kbps, 25 kHz deviation, PSDU length = 20 bytes, packet error rate (PER) = 1%
Sensitivity, 4-Byte Preamble	−107.0 dBm	100 kbps, 50 kHz deviation, PSDU length = 20 bytes, PER = 1%
Sensitivity, 8-Byte Preamble	−104.4 dBm	100 kbps, 25 kHz deviation, PSDU length = 20 bytes, PER = 1%
Sensitivity, 12-Byte Preamble	−101.2 dBm	150 kbps, 37.5 kHz deviation, PSDU length = 20 bytes, PER = 1%
Sensitivity, 16-Byte Preamble	−104.2 dBm	200 kbps, 100 kHz deviation, PSDU length = 20 bytes, PER = 1%
Sensitivity, 16-Byte Preamble	−99.4 dBm	200 kbps, 50 kHz deviation, PSDU length = 20 bytes, PER = 1%

FIRMWARE DOWNLOAD SEQUENCE

The firmware module must be downloaded to the ADF7030-1 memory in the PHY_OFF state after download of configuration files (radio profile, generic packet) and after device configuring using the CMD_CFG_DEV command. When the CMD_PHY_ON command is issued, the firmware module is enabled.

When waking up from PHY_SLEEP, the user must again download the firmware module and then issue the CMD_CFG_DEV command before transitioning to the PHY_ON state via the CMD_PHY_ON command.

Two firmware modules are available for IEEE 802.15.4g-2012 functionality. Use IEEE_15d4g_v1_0_00R.dat for the FEC encoded packets and use IEEE_15d4g_v1_0_00R_non_FEC.dat for the nonFEC encoded packets. Each firmware module contains four blocks of data to be written to the ADF7030-1. The memory location and size of each block is summarized in Table 11.

Information on how to write to the ADF7030-1 can be found in the ADF7030-1 Software Reference Manual.

The firmware modules can be obtained from the ADF7030-1 product page.

Table 11. Firmware Module Memory Location and Size

Block	Address	IEEE_15d4g_v1_0_00R.dat	IEEE_15d4g_v1_0_00R_non_FEC.dat
0	0x20000130	4 bytes	4 bytes
1	0x2000112C	3520 bytes[1]	2512 bytes[1]
2	0x20002BA0	164 bytes	164 bytes
3	0x20002FA0	84 bytes	84 bytes

[1] Block is provided in smaller blocks in the firmware module.