ANALOG DEVICES

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APPLICATION NOTE

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SPICE-Compatible Op Amp Macro-Models

by Mark Alexander and Derek F. Bowers

There is a definite trend towards a comprehensive circuit-simulation approach. We believe that 75 percent of all installed circuit simulators are being used for system, rather than IC, design. Almost all of these simulators are variants of SPICE. With the growth of the electronics industry, system engineers have come to need increasingly accurate models for an ever larger number of integrated circuits, especially the ubiquitous operational amplifier. However, the increasing speed and complexity of these IC devices has caused problems that were never anticipated by the original developers of SPICE.

Because of the large number of active devices in a typical op amp, circuit simulations that use only transistor-level models can take an unacceptable amount of time, particularly when the circuit contains several op amps. Even simple models of semiconductor devices consume a large amount of computing time because of the multiplicity of nonlinear equations involved. In some cases, the time needed for a complete simulation might exceed the time necessary to build an engineering prototype. Obviously, such a situation would completely defeat the whole purpose of using SPICE.

Fortunately, you can reduce simulation time by using a macro-model that represents the op amp as accurately as possible without using large numbers of transistors or other nonlinear devices. However, it is quite a challenge to design a macro-model that, for all intents and purposes, exactly mimics the real device. For an op amp model to be of real use to the circuit designer, it must not only accommodate all important DC parameters, but also provide a reasonbly close approximation of the AC characteristics over a region that extends well beyond the unity-gain crossover frequency.

EXISTING MACRO-MODELS ARE INADEQUATE

Macro-models for many op amps already exist in the device libraries of several available software simulators. Most of these models are based on the original work done by Graeme Boyle and his colleagues (see Reference 1), who developed their macro-model during the mid-1970s to ease the CPU-time crunch on the already overloaded mainframe computers of the day. Boyle eliminated all but two transistors from his macro-model. The two remaining devices formed the differential-input stage of the op amp; all subsequent stages were implemented with linear controlled sources, passive components, and diodes. The transistors in the input stage were retained because they facilitated the simulation of real-world effects such as bias currents and variation of output dV/dt with the differential input voltage.

Because Boyle's method greatly reduces the number of overall nonlinear elements, the simulation time required per amplifier also decreases substantially. The Boyle structure is certainly an improvement over a full transistor-level simulation, but the structure still has several deficiencies, which prompted the development of the new macro-model. The deficiencies are as follows:

- The Boyle model provides only two poles (and no zeroes) for shaping the frequency response of the complete amplifier – a configuration that is barely adequate for slower op amps, and completely insufficient for today's faster devices.
- All internally generated node voltages are referenced to ground, even if the amplifier is "floated" with respect to ground. This configuration is not representative of the true operation of an op amp – almost none of the available devices provide a ground reference.
- The output-terminal current flows out of a controlled source connected to ground, instead of from the power-supply rails as it would in a real amplifier. This feature completely precludes the simulation of circuits that depend on the amp's output current splitting correctly between the supply rails.

IDEAL ELEMENTS CAN REDUCE COMPLEXITY

The circuit topology of the original Boyle model (Figure 1) was developed using two basic macro-modeling techniques (called simplification and build-up) that proved very useful in the development of the new macro-model as well.

The simplification technique successively reduces the complexity of major internal stages of the op amp by using simple ideal elements to replace real portions of the circuit. Therefore, you can expect a functional block that uses this approach to

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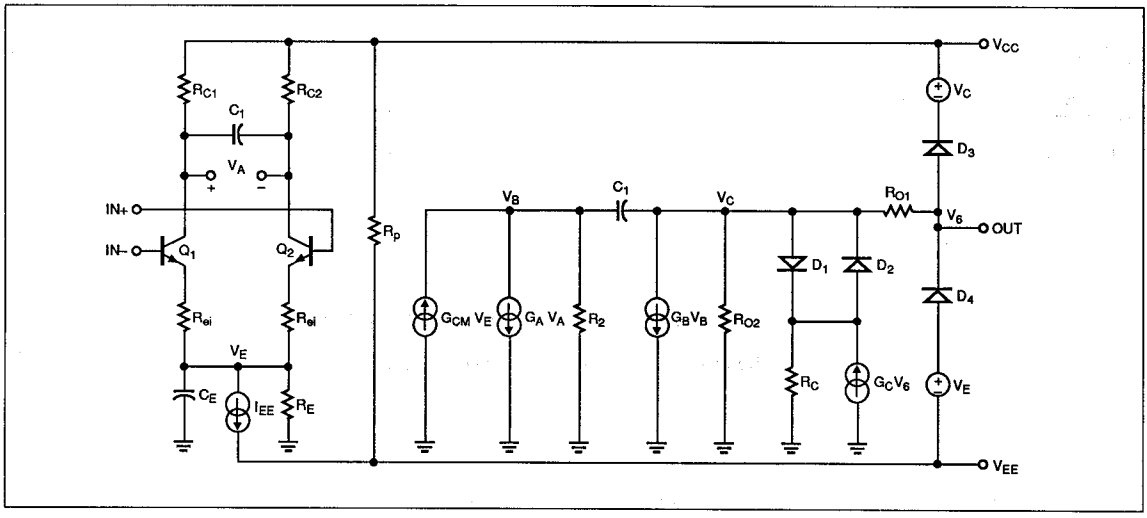

FIGURE 1: *A serious disadvantage to the Boyle op amp macro-model is that all voltages are referenced to ground.*

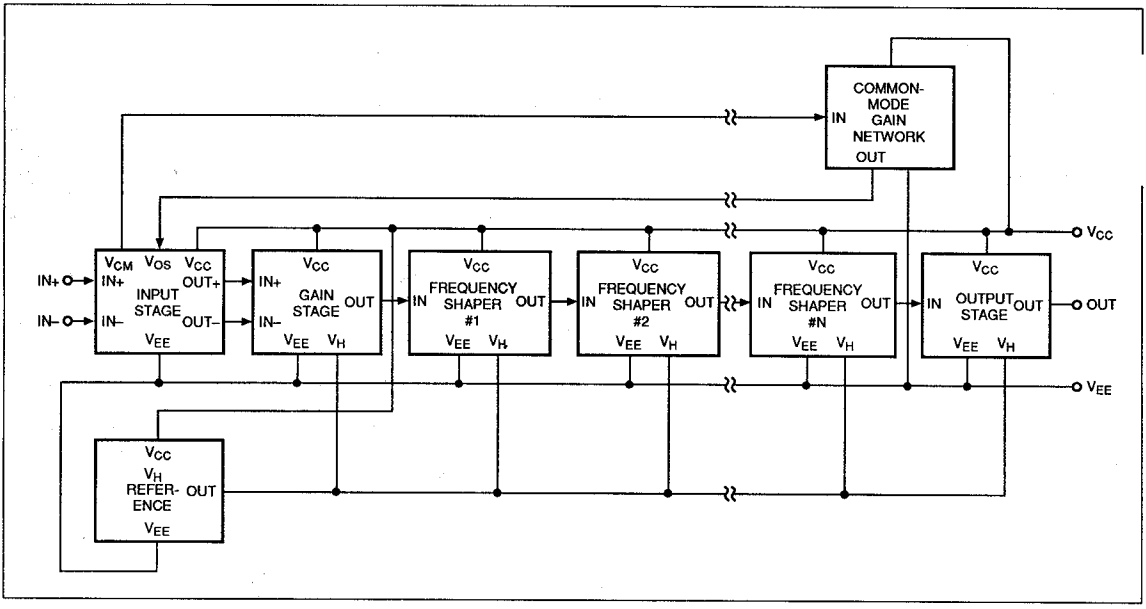

FIGURE 2: *The new op amp macro-model is inherently modular. You can cascade any of the building blocks to obtain any number of poles and zeroes in your op amp design.*

closely resemble the actual circuit. In Figure 1, the model of the input stage is a good example of simplification. The model retains the differential-input characteristics of an emitter-coupled pair, but eliminates any active loads; it replaces the tail-current source with an ideal element; and it assumes the task of generating the second amplifier pole. Adding a single capacitor (C_E) allows the model to provide a pole in this stage, and the reduction in overall component count makes the simulation run faster.

The build-up technique, on the other hand, lets you construct a circuit block composed entirely of ideal elements, which very closely emulates the behavior of the real section of the device. Unfortunately, the build-up technique often results in subsections that bear little resemblance to their physical equivalents. Figure 1's output stage is a good example: it provides the necessary output voltage clipping, has the correct output resistance, and also provides short-circuit current limiting; but does not look like anything one would expect to find in the schematic of a real op amp.

DEVELOPMENT OF AN IMPROVED MACRO-MODEL

The impetus behind the new macro-model (Figure 2), arose out of the desire to create a model that operates like a real op amp. Yet it still had to be simple enough so that it would suffice as a generic model. Figures 3, 4 and 5 show that the model consists of several cascaded sections that process the input signal.

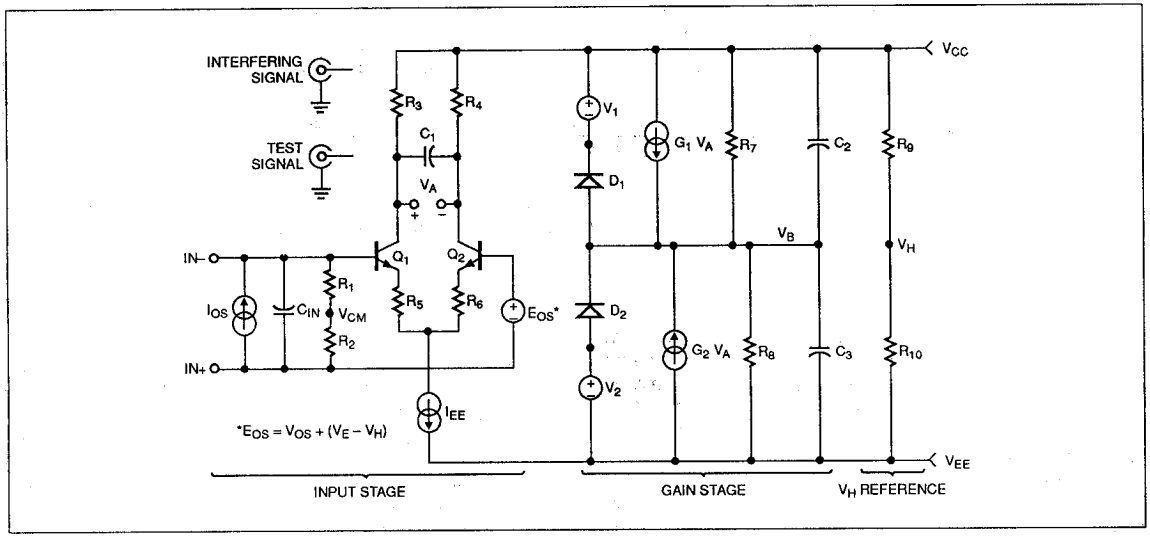

FIGURE 3: *The input stage of the new model resembles that of the Boyle, but all succeeding stages have a radically different structure.*

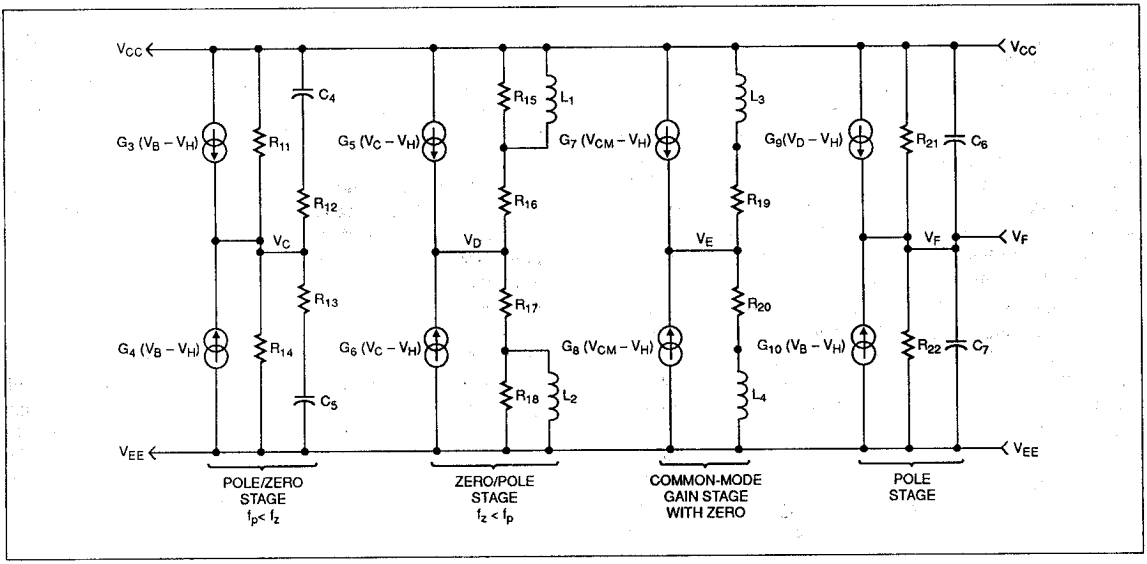

FIGURE 4: *Three types of frequency-shaping networks are available, in addition to a common-mode gain stage that provides a zero.*

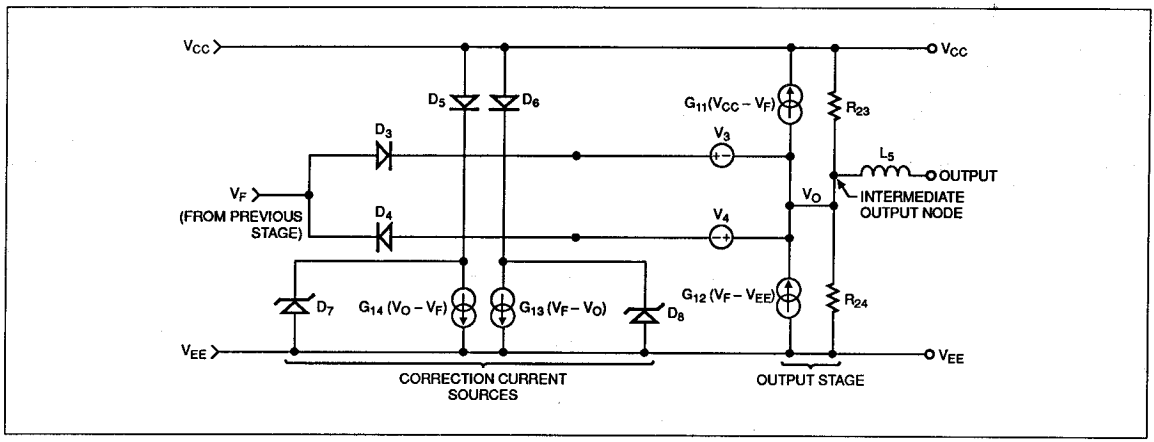

FIGURE 5: *The new output stage is complemented by current sources, which correctly split the load current between the power-supply rails.*

The input stage is very similar to the Boyle model's because the simplification technique was used in its construction. However, after the input stage, all similarity between the two macro-models disappears because of the way the build-up method was used to generate the rest of the new model. Notice that there is no ground reference in any of the signal-processing blocks. Instead, after differential to single-ended conversion, all internally generated node voltages are referred to the midpoint between the supply rails. This midpoint, called V_H in the model, is generated by two equal resistors connected between the supply rails.

The minimum requirement for modeling any particular op amp with the new macro-model is essentially the same as for the Boyle topology: a differential-input stage, a gain stage, and an output stage. This configuration yields a basic two-pole frequency response and allows direct comparisons between the two types of macro-models in terms of simulation time. You can add any combination of unity-gain pole, pole-zero, and zero-pole blocks between the gain stage and the output stage in order to obtain the desired frequency-dependent roll-off of the open-loop gain. The difference between the blocks is that the pole-zero block generates a pole at a lower frequency than that of the zero, whereas the zero-pole generates a pole at a higher frequency than that of the zero.

Box 2, "Calculation of Model Parameters," shows the calculations that you must perform in order to construct an op amp model based on the building blocks of Figures 3, 4 and 5. You can do these calculations quite easily on a hand calculator, given certain data sheet parameters of the op amp in question, together with the necessary pole-zero locations.

The input stage in Figure 3 is a simplified 2-transistor circuit. One major difference between the new model and its predecessor is that, in the new model, the input stage uses the same type of input devices as the physical op amp – that is, NPN or PNP bipolars, P-channel JFETs (or N-channel devices where applicable), or MOSFETs. The Boyle model allows *only* for bipolar devices in its input stage, which are fine if a bipolar input op amp is being modeled. However, when you model a FET input op amp with the Boyle technique, you have to dramatically increase the current gain of the input transistors in order to obtain the desired input bias current. You must also use emitter degeneration to reduce their transconductance. The result of these modifications is that the usual variation of output dV/dt of a FET input amplifier over a fairly wide input-differential voltage range (typically 1 to 2V) will not be correctly simulated. A degenerated bipolar input stage has a linearized, hyperbolic-tangent transfer characteristic (See Reference 2), whereas a FET input stage has a square-law transfer characteristic (See Reference 3). Obviously, these characteristics are not equivalent. Therefore, because the parameter calculations for a FET input stage are no more complicated than those of a bipolar stage, it makes sense to use the correct input devices in the model.

All input-stage parameters (such as offset voltage, offset current, and input capacitance) that exhibit nonideal behavior are modeled using separate ideal elements. Also, two equal resistors are connected between the inverting and noninverting input terminals to generate the common-mode input voltage. The input voltage is used in a later section of the model, where it is scaled and frequency-shaped before being fed back into the input stage as a modifier to the offset voltage.

The model assumes that the input transistors are perfectly matched and do not have any junction capacitance that would alter the overall frequency response. It does account for the correct input-bias current, however, through appropriate choice of current gain for the bipolar stage or gate-leakage currents for the FET stage. You set the voltage gain of the differential pair

BOX 1

THE EVOLUTION OF SPICE SIMULATORS

The electrical-circuit simulator SPICE, and the more powerful version called SPICE2, originally emanated from the University of California, Berkeley, during the 1970s (see Reference 4). Primarily written for the purpose of assisting design engineers with the analysis of integrated circuits at the transistor level (hence the acronym *S*imulation *P*rogram with *I*ntegrated *C*ircuit *E*mphasis), SPICE lets you use a computer to evaulate your designs more quickly and more thoroughly than is possible by means of laborious hand calculations. The popularity of SPICE soon spread to the system-level-design community for the same reasons that the IC designers embraced it.

The original version of SPICE was a public-domain program available at a purely nominal charge; however, many software vendors have recognized the need for a fully supported, adapted, and improved commercial circuit simulator. The first mainframe-based versions of such programs included HSpice from Meta-Software, I-Spice from NCSS timesharing and PRECISE from Electronic Engineering Software. Recently, most mainframe versions have been adapted for use on workstations, and some have been adapted for IBM PCs and compatibles.

The first PC-based version of SPICE was PSpice from MicroSim Corp. It was followed by others, such as IS-Spice from Intusoft. Other companies, including Analogy Inc (which offers a behavioral-simulation package known as Saber), have chosen to depart from the conventional SPICE format of using "boxed" circuit elements to construct models. Instead, Saber relies on rigorous defining equations written in a specific modeling language, called Mast, to control the behavior of any desired electrical circuit model.

to unity by making the load resistor value equal to the reciprocal of the transconductance of the transistors. This assumption simplifies the calculations to determine the slew-rate-limiting components. Tail current for the input stage is nominally set to 1mA for convenience; however, it can be scaled down to 100μA, 10μA, or 1μA depending on the amp's total quiescent current.

GAIN STAGE FEATURES

The model's open-loop gain is normally achieved in a single stage (See Figure 3), which consists of two voltage-controlled current sources, two resistors, two capacitors, and a voltage-limiting network. The conversion of signals from differential to single-ended form also takes place during this stage. The voltage-limiting network consists of a pair of diodes, each connected to its own voltage source. The network prevents the gain stage and the other internal nodes of the model from swinging beyond the power-supply-rail voltages during an input-overdrive condition. Voltage limiting *must* take place in the open-loop gain stage; otherwise, succeeding nodes could attempt to simulate the generation of huge (hundreds of kilovolts) signals.

Two capacitors, connected in parallel with the resistors, determine both the dominant amplifier pole and the slew rate. At present, the macro-model can handle only symmetrical positive and negative slew rates, because symmetry is the easiest condition to simulate. However, future enhancements may allow for some variation between them. Finally, to each of the two voltage-controlled current sources, the stage adds a DC component that makes up the bulk of the amp's quiescent supply current.

Investigation of op amp frequency response reveals that, in most cases, accurate simulation of the gain and phase variation of real devices at high frequencies requires more than two poles. Further, different types of op amps have varying numbers of poles and zeroes. To allow each of these diverse types to be easily converted to a SPICE-compatible subcircuit - without having to start from scratch every time – a truly general model would have to be highly modular and permit arbitrarily large numbers of poles and zeroes. Therefore, the final structure uses a few basic building blocks that are common to all individual op amp models. These blocks are shown in Figure 4.

All of the frequency-shaping blocks have unity-gain at DC, because the g_m of each voltage-controlled current source (VCCS) is equal to the reciprocal of the resistance connected from each node of the VCCS (voltage-controlled current source) to the power-supply rails. This topology is advantageous because during model generation for a specific amplifier, you can comment out separate poles or pole-zero pairs. You can then see their effect, individually, on the net frequency response of the amplifier, so that pole-zero tweaking becomes rather easy. Because all the frequency-shaping blocks have unity-gain at DC, the procedure does not alter the model's DC open-loop gain.

The common-mode gain stage in Figure 4 consists of two VCCSs that drive two equal resistors, each resistor is connected in series with an inductor to one of the supply rails. The inductors simulate the typical fall-off of CMRR that most amplifiers exhibit as the input frequency increases. The input common-mode voltage, relative to the V_h node, controls the current sources. Each controlled source has a g_m equal to the reciprocal of the associated resistor value divided by the CMRR of the amplifier at DC.

Accordingly, the gain from the input common-mode network to the internal common-mode gain node is equal to the reciprocal of the amplifier's CMRR. (The term "gain" is a misnomer here, because the common-mode gain has a value that is much less than unity).

The inductors add a zero to the common-mode gain, which is the same as adding a pole to the CMRR. The common-mode voltage, after being scaled and appropriately frequency-shaped, is then added back to the input stage as dictated by theory. This step is done by making the offset-voltage source in the input stage a unity-gain voltage-controlled voltage source, which has a DC component equal to the amplifier's V_{OS}.

The operation of the output stage in Figure 5 is not entirely obvious. The internal op amp output signal, after receiving all the appropriate frequency shaping, appears as a voltage referenced to V_h at the last node prior to processing by the output stage. The two voltage-controlled current sources in the output block drive two equal resistors connected to the supply rails, as with the other blocks. Here, however, the g_m of the two controlled sources is arranged so that they act as active current generators. Consequently, each g_m source generates just enough current to provide the desired voltage drop across its paralleled resistor.

When there is no load on the output, the model draws no current from either power-supply rail. It thus behaves somewhat like an ideal, unity-gain, class-B output stage with no crossover distortion. Because the two resistors are each equal to twice the open-loop output resistance, the output stage appears to act as a voltage source referenced to V_h with the correct DC output resistance. Simulating the right output resistance means that the DC open-loop gain will be properly reduced as the amplifier is loaded.

BOX 2

CALCULATION OF MODEL PARAMETERS

The following equations allow you to create an improved macro-model for simulation of any op amp. The calculations are given separately for each of the available building blocks, and some power supply considerations are discussed.

INPUT- AND GAIN-STAGE CALCULATIONS

a. General Calculations

Refer to Figure 3 to identify components and signals mentioned here. First, Choose I_{EE} such that it is somewhat less than the amp's total quiescent current. For convenience, you may set I_{EE} to 1mA, 100µA, 10µA, or 1µA. Then,

$$C_2 = C_3 = \frac{I_{EE}}{\text{SLEW RATE}}$$

$$R_7 = R_8 = \frac{1}{2\pi f_{p1} C_2},$$

were f_{p1} = dominant amplifier pole.

$$G_1 = G_2 = \frac{A_{VOL}}{R_7},$$

where A_{VOL} = open-loop DC gain

$$R_3 = R_4 = \frac{1}{G_1}$$

$$C_1 = \frac{1}{4\pi f_{p2} R_3},$$

where f_{p2} = second amplifier pole

$V_1 = V_{CC} - (+V_{OUT\ MAX}) + V_T \ln(2I_{EE}/I_S)$

$V_2 = (-V_{OUT\ MAX}) - V_{EE} + V_T \ln(2I_{EE}/I_S)$

$V_T = 0.02585V$ at $T = 27°C$

$I_S = 1 \times 10^{-12}$ A (FOR BOTH DIODES).

You can substitute some data sheet parameters directly into the model. These parameters are:

E_{OS} = Input Offset Voltage (DC component only);

I_{OS} = Input Offset Current; C_{IN} = Input Capacitance.

b. Bipolar Input-Stage Calculations

First, you must evaluate the following equation to determine whether the op amp in question can be modeled using the new macro-model:

$$A_{VOL} \le \frac{\text{SLEW RATE}}{4\pi f_{p1} V_T},$$

Where $V_T = 0.02585V$ at 27°C.

If the equation holds true, then you may proceed with the rest of the calculations. If not, then you must modify the model to accommodate this particular op amp.

$$R_5 = R_6 = R_3 - \frac{2 V_T}{I_{EE}}$$

$$\beta_F = \frac{2 I_{BIAS}}{I_{EE}},$$

where β_F is the forward current gain of the input transistors, and I_{BIAS} is the input bias current.

$$R_1 = R_2 = \frac{1}{2\left(\frac{1}{R_{ID}} - \frac{1}{2 \beta_F R_3}\right)} \le 5 \times 10^{11}\ \Omega,$$

where R_{ID} is the differential input resistance. If R_{ID} is not a specified data sheet parameter, then set both R_1 and R_2 to the value $5 \times 10^{11}\Omega$.

c. JFET Input-Stage Calculations

If your design has a JFET input stage, use the default value of –2.000V for the gate-to-source cutoff voltage V_{TO}. Also, change the name of the first-stage current source to I_{SS}. The main calculation is to determine β, the JFET gain factor:

$$\beta = \frac{(G_{1/2})^2}{2 I_{SS}},$$

where I_{SS} is the first-stage tail current.

For maximum output dV/dt, the tail current must originate from one side only of the differential pair; this condition requires a differential input voltage equal to:

$$V_{ID} = \frac{\sqrt{2}\ (\text{SLEW RATE})}{2\pi\ A_{VOL}\ f_{p1}}$$

BOX 2 *Continued*

Also, the input bias current is composed of the gate-drain and gate-source leakage currents. Thus,

$$I_S = \frac{I_{BIAS}}{2},$$

where I_{BIAS} is the input bias current at 27°C. Further,

$$R_1 = R_2 = \frac{R_{ID}}{2},$$

where R_{ID} is the differential input resistance (normally 1 x $10^{12}\Omega$.

Finally, you can set the values of R_5 and R_6 to zero, because degeneration is not normally needed with JFET input amplifiers.

Frequency-Shaping-Stage Calculations

To identify parameters of the frequency-shaping stages, refer to Figure 4. In all three types of the frequency-shaping stage, set G_3 and G_4 to 1 x 10^{-6} times A/V, for convenience. Further, f_Z is the zero frequency and f_P is the pole frequency.

Then for the pole-zero stage,

$R_{11} = R_{14} = 1 \times 10^6$

$$R_{12} = R_{13} = \frac{R_{11}}{f_Z/f_P - 1};$$

$$C_4 = C_5 = \frac{1}{2\pi f_Z R_{12}}$$

for the zero-pole stage,

$R_{16} = R_{17} = 1 \times 10^6$

$R_{15} = R_{18} = (f_P/f_Z - 1)\, R_{16}$;

$$L_1 = L_2 = \frac{R_{15/18}}{2\pi f_P}$$

for the pole stage,

$R_{21} = R_{22} = 1 \times 10^6$

$$C_6 = C_7 = \frac{1}{2\pi f_P R_{21}}.$$

Common-Mode-Gain-Stage Calculations

To identify the parameters of the common-mode gain stage, refer to Figure 4.

$R_{19} = R_{20} = 1 \times 10^6$

$$G_7 = G_8 = \frac{1}{R_{19} \times CMRR},$$

$$L_3 = L_4 = \frac{R_{19}}{2\pi f_{P(CM)}}$$

where f_{CM} is the common-mode pole.

Output-Stage Calculations

To identify the parameters of the output stage, refer to Figure 5. The breakdown voltage of diodes D_7 and D_8 is nominally set to 50V. The value of inductor L_5 is determined by experiment. R_{OUT} is that open-loop output resistance; V_T is 0.02585V at 27°C; and I_S is 1 x 10^{-12}A for all diodes. Then,

$$G_{11} = G_{12} = G_{13} = G_{14} = \frac{1}{2\ R_{OUT}}$$

$R_{23} = R_{24} = 2 \times R_{OUT}$

$V_3 = I_{SC}(+VE)R_{OUT} - V_T \ln(20 \times 10^{-6}/I_S)$

$V_4 = |I_{SC}(+VE)R_{OUT}| - V_T \ln(20 \times 10^{-6}/I_S)$

You can determine the values of resistors R_9 and R_{10} in Figure 3 by means of the following equation:

$$R_9 = R_{10} = \frac{1}{2(dI_{SY}/dV_{SY})},$$

where dI_{SY}/dV_{SY} represents the variation of supply current caused by a change in the supply voltage. The total quiescent current that flows between V_{CC} and V_{EE} in the model is thus:

$$I_{SY} = I_{EE} + (N+1)\left(\frac{V_{CC} - V_{EE}}{2R}\right) + I_{DC} + \left(\frac{V_{CC} - V_{EE}}{R_9 + R_{10}}\right),$$

where N is the total number of frequency-shaping and common-mode gain stages in the model; R is normally 1 x $10^6\Omega$; this value, along with the transconductance of the G-sources in the frequency shaping stages, can be appropriately scaled for low power op amps;

and I_{DC} is the DC offset added to the G_1 and G_2 sources to make up the difference between the current drawn by the rest of the model and the quiescent current of the

A subtle problem exists with this simple push-pull output stage, however. Regardless of whether that stage is sinking or sourcing current, the load current is always split equally between both rails – not exactly what a real output stage would do. So, with a sourced-load current, for example, the net positive supply current increases by only half the amount flowing in the load. The negative supply current decreases by the same amount. To compensate for this anomaly, you force a current from the positive rail to the negative rail exactly equal to half the load current. This correction current must always flow in the same direction – even if the output current reverses polarity.

The effect, therefore, of the two correction sources in Figure 5 is to force a unipolar compensating current between the power-supply rails that is equal to half the output current. In SPICE, because there is no easy way to implement an absolute value VCCS, there must be two linear correction sources – one for each half cycle of output current. The diodes in series with each

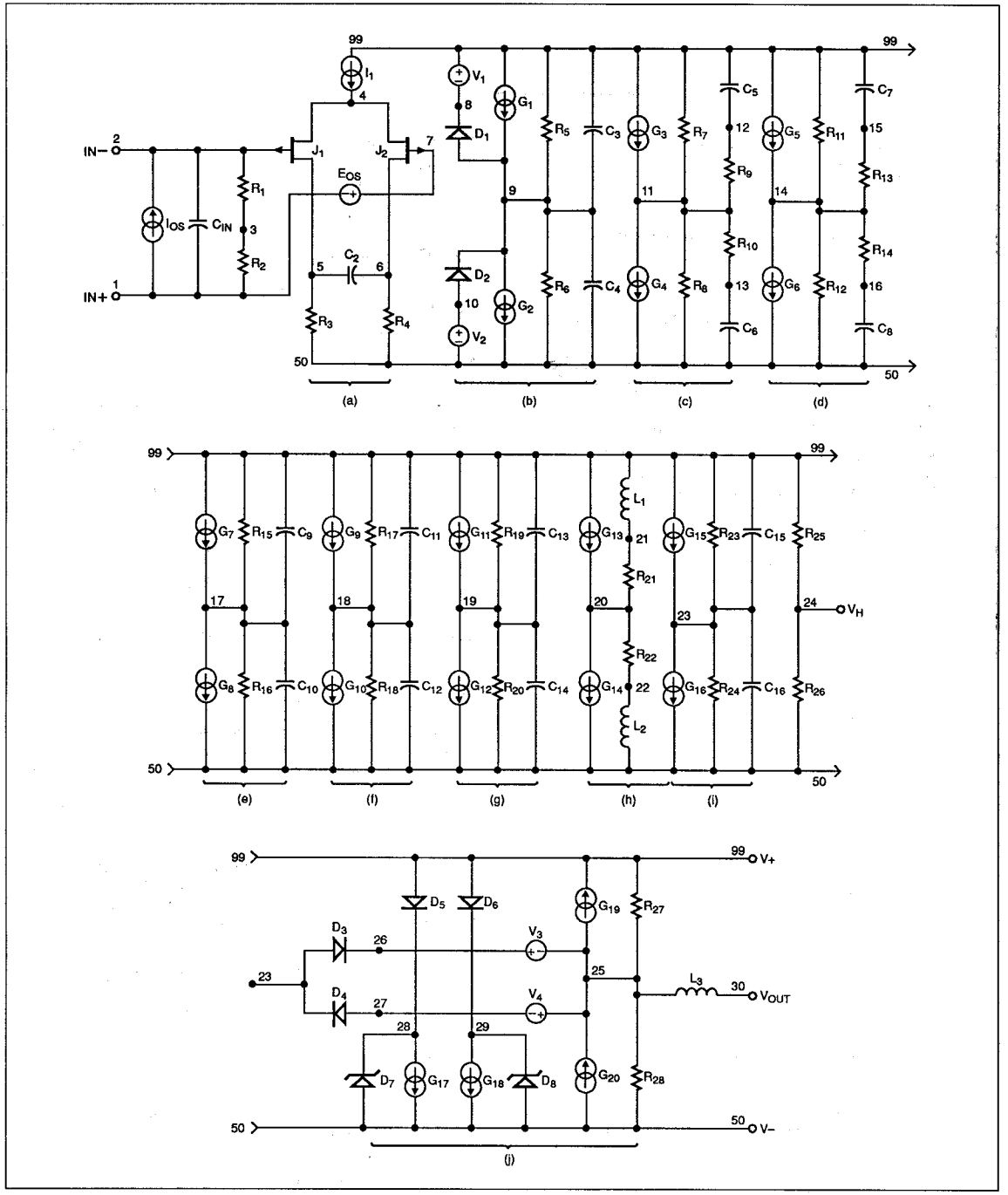

FIGURE 6: *The OP-42 macro-model is more complex than its Boyle counterpart, requires more time for simulation, but pays off in greatly improved accuracy.*

LISTING 1: OP-42 SPICE Macro-Model Net List

```
OP-42 MACRO-MODEL  ©PMI 1990
*
* SUBCKT OP-42 1  2 30  99  50
*
* INPUT STAGE & POLE AT 15.9 MHZ
*
R1    1   3        5E11
R2    2   3        5E11
R3    5   50       707.36
R4    6   50       707.36
CIN   1   2        5E-12
C2    5   6        7.08E-12
I1    99  4        1E-3
IOS   1   2        4E-12
EOS   7   1        POLY(1) 20 24 1E-3 1
J1    5   2   4    JX
J2    6   7   4    JX
*
* SECOND STAGE & POLE AT 45 HZ
*
R5    9   99       176.84E6
R6    9   50       176.84E6
C3    9   99       20E-12
C4    9   50       20E-12
G1    99  9        POLY(1) 5 6 3.96E-3 1.4137E-3
G2    9   50       POLY(1) 6 5 3.96E-3 1.4137E-3
V1    99  8        2.5
V2    10  50       3.1
D1    9   8        DX
D2    10  9        DX
*
* POLE-ZERO PAIR AT 1.80 MHZ/2.20 MHZ
*
R7    11  99       1E6
R8    11  50       1E6
R9    11  12       4.5E6
R10   11  13       4.5E6
C5    12  99       16.1E-15
C6    13  50       16.1E-15
G3    99  11       9  24  1E-6
G4    11  50       24  9  1E-6
*
* POLE-ZERO PAIR AT 1.80 MHZ/2.20 MHZ
*
R11   14  99       1E6
R12   14  50       1E6
R13   14  15       4.5E6
R14   14  16       4.5E6
C7    15  99       16.1E-15
C8    16  50       16.1E-15
G5    99  14       11 24 1E-6
G6    14  50       24 11 1E-6
*
* POLE AT 53 MHZ
*
R15   17  99       1E6
R16   17  50       1E6
C9    17  99       3E-15
C10   17  50       3E-15
G7    99  17       14 24 1E-6
G8    17  50       24 14 1E-6
*
* POLE  AT 53 MHZ
*
R17   18  99       1E6
R18   18  50       1E6
C11   18  99       3E-15
C12   18  50       3E-15
G9    99  18       17 24 1E-6
G10   18  50       24 17 1E-6
*
* POLE AT 53 MHZ
*
R19   19  99       1E6
R20   19  50       1E6
C13   19  99       3E-15
C14   19  50       3E-15
G11   99  19       18 24 1E-6
G12   19  50       24 18 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 100 KHZ
*
R21   20  21       1E6
R22   20  22       1E6
L1    21  99       1.5915
L2    22  50       1.5915
G13   99  20       3  24 1.58E-11
G14   20  50       24  3 1.58E-11
*
*POLE AT 79.6 MHZ
*
R23   23  99       1E6
R24   23  50       1E6
C15   23  99       2E-15
C16   23  50       2E-15
G15   99  23       19 24 1E-6
G16   23  50       24 19 1E-6
*
*OUTPUT STAGE
*
R25   24  99       111.1E3
R26   24  50       111.1E3
R27   25  99       90
R28   25  50       90
L3    25  30       2.5E-7
G17   28  50       23 25 11.1111E-3
G18   29  50       25 23 11.1111E-3
G19   25  99       99 23 11.1111E-3
G20   50  25       23 50 11.1111E-3
V3    26  25       0.7
V4    25  26       0.7
D3    23  26       DX
D4    27  23       DX
D5    99  28       DX
D6    99  29       DX
D7    50  28       DY
D8    50  29       DY
*
* MODELS USED
*
.MODEL JX PJF(BETA=999.3E-6  VTO=-2.000  IS=8E-11)
.MODEL DX   D(IS=1E-15)
.MODEL DY   D(IS=1E-15 BV=50)
.ENDS OP-42
```

source perform half-wave rectification, and the zeners ensure that there is always a conductive path for each source when its current reverses direction. The net result of all these additional elements is an output stage model whose DC behavior very closely mimics that of the phycial circuit.

To account for the typical rise in emitter-follower output stage impedance with frequency, the macro-model includes an output inductor connected between the intermediate output node and the actual macro-model output node (see Figure 5). You determine the value of this inductor, on a trial-and-error basis, by using capacitive loads on the model until the amount of overshoot is very close to that which you observed with the real op amp and the same load.

Short-circuit current limiting is also a necessary feature of any good op amp macro-model. In Figure 5, limiting is accomplished by clamping the output voltage (V_F) from the previous frequency-shaping stage to the intermediate output node (V_0), using diodes D_3 and D_4, and voltage sources V_3 and V_4. Remember that the signal from the previous stage is always equal to the ideal output voltage with no load, and that the output stage behaves as a voltage source with a finite output resistance. The action of the diodes and voltage sources is then equivalent to clamping the voltage drop across the effective output resistance. You can obtain the required output current limiting by an appropriate choice of each voltage source.

Because the main goal of the new structure is to provide improved AC accuracy, the model must also correctly represent the common-mode behavior. So, the modeling team selected the PMI OP-42, a JFET-input op amp, as its first guinea pig, largely because the Boyle model cannot properly accommodate a JFET input stage. Although the team had to work out all the equations pertaining to the JFET input stage before they

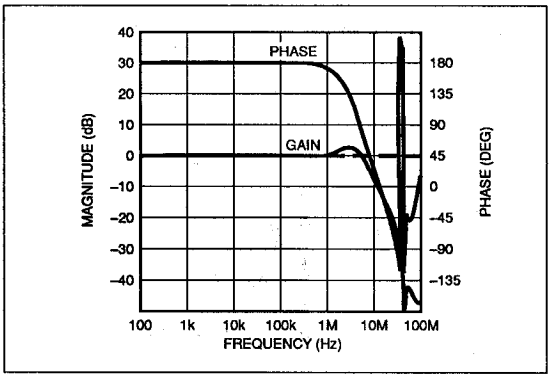

FIGURE 7: *When you connect the OP-42 in a unity-gain, inverting configuration, the gain response shows a slight peak at about 6MHz; there is a rapid increase in phase shift above 2MHz.*

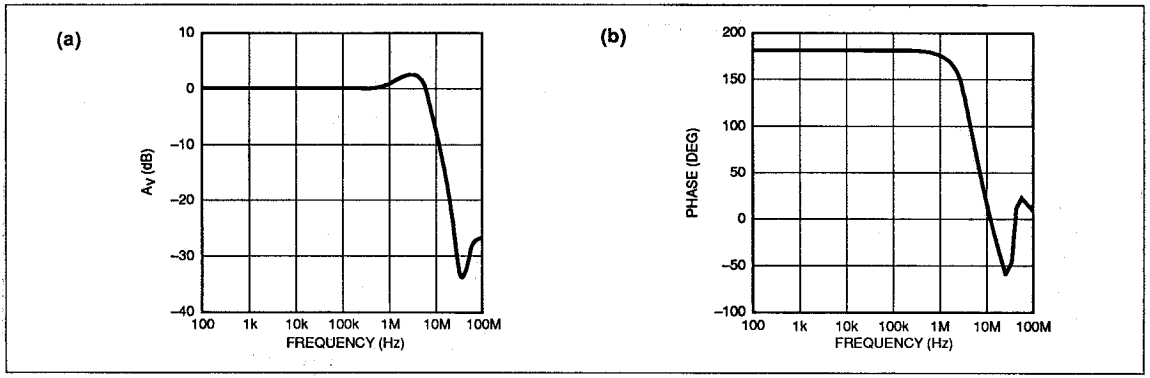

FIGURE 8: *Using the new macro-model, the simulated gain response (a) of the OP-42 is very like that of the real device, with a slight peak at 4MHz. The phase-response (b) is very good. This curve closely follows that of the real device.*

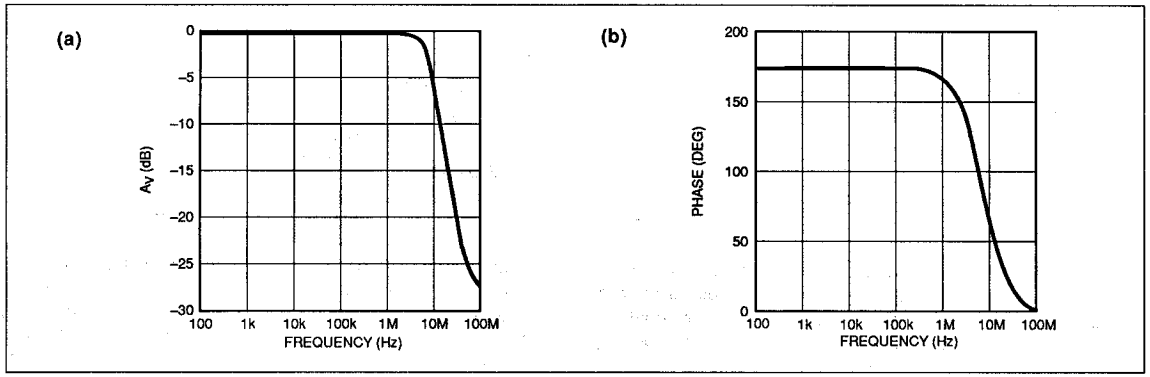

FIGURE 9: *The Boyle model of the OP-42 (a) does not show the amplitude peak at 4MHz that is characteristic of the real device. The phase response (b) also is not very accrurate, especially in the regoin beyong 10MHz.*

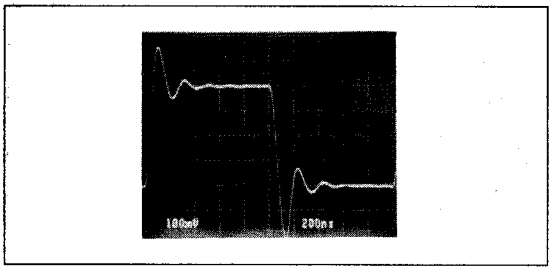

FIGURE 10: *An OP-42 with a 430pF capacitive load shows both overshoot and undershoot when driven with a 500kHz, 200mV peak square wave.*

could test the complete model, this stage turned out to be fairly easy to handle mathematically and did not hinder the development of the final macro-model structure.

Figure 6 shows the resulting implementation. The physical OP-42 has a gain-bandwidth product of approximately 10MHz and a symmetrical slew rate of 50V/μs. The CMRR-versus-frequency curve of this amplifier indicates that a zero at about 100kHz is necessary in the model's common-mode gain stage.

Listing 1 shows the net list for the OP-42 macro-model, which has 8 poles, 2 zeroes, plus a zero in the common-mode gain stage at 100kHz. The model of even a relatively stable amplifier needs that many poles and zeroes in order to accurately mimic the gain and phase behavior of the physical device at high frequencies.

Inspection of the output-stage section of the net list shows that the open-loop output resistance is 45Ω. A 250nH inductor, connected in series with the output terminal, compensates for the rise in effective open-loop output impedance at high frequencies. The current-limiting network formed by diodes D3 and D4 and voltage sources V_3 and V_4 clamps the maximum output current at approximately ±30mA.

SIMULATION-ACCURACY COMPARISONS

Figure 7 shows the gain and phase response of a physical OP-42 connected as an inverting, unity-gain amplifier that has 1kΩ input and feedback resistors and runs from ±15V supplies. You can see a small amount of peaking (about 2dB) in the closed-loop gain curve, and the phase shift increases rapidly above 2MHz. Figures 8a and 8b show the gain and phase response of the new OP-42 macro-model under the same conditions. The gain response shows the same amount of closed-loop peaking as that of the real circuit; the phase response almost exactly matches that of the real device to at least 10MHz.

Figures 9a and 9b, which show the corresponding output curves from the Boyle implementation, clearly demonstrate the deficiencies in the Boyle model's response accuracy. The gain response does not show the 2dB peak, indicates too steep a roll-off, and is quite inaccurate above 10MHz. The Boyle model's phase response does not even come close to the real circuit's response. The OP-42 macro-model, with its multiple pole-zero complement, emulates the AC response of the actual circuit more accurately.

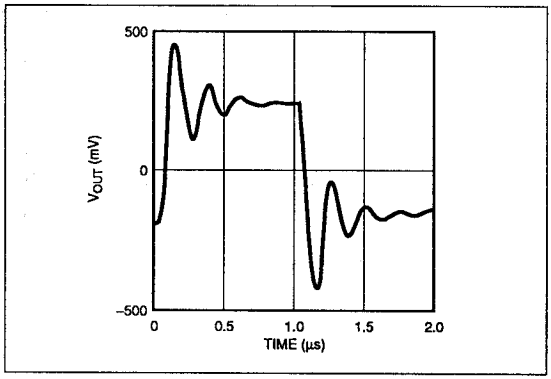

FIGURE 11: *The new macro-model's simulation of an OP-42 with a capacitive load of 430pF shows the symmetrical nature of the model's output stage.*

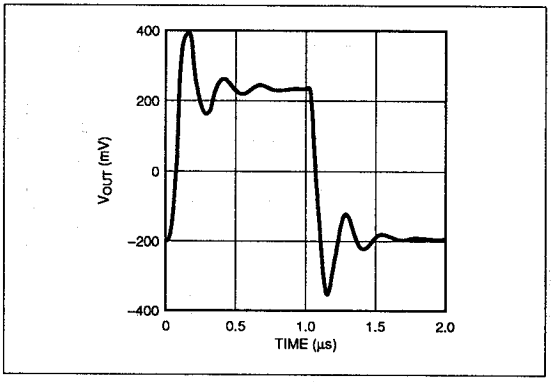

FIGURE 12: *The Boyle model of the OP-42 simulates approximately the right amount of overshoot, but its ringing frequency is too low.*

Figure 10 shows the measured transient response of the inverting, unity-gain OP-42 amplifier with a 430pF capacitive load. For a 400mV_{p-p} input signal, there is about 75 percent overshoot and 100 percent undershoot. The simulation results from the new macro-model (see Figure 11) show about 115 percent of both overshoot and undershoot. This simulated value is quite close to the actual value on the negative half of the waveform, but differs from the actual value on the positive half. The expanation for this anomaly is that although the new macro-model has a perfectly symmetrical output stage, the op amp being modeled may not. The OP-42, in fact, has an asymmetrical, all NPN-transistor output stage. As a result, the high-frequency, open-loop response is variable and depends on whether the output stage is sinking or sourcing current.

The Boyle configuration, too, models an op amp's output stage as a perfectly symmetrical voltage source and, as Figure 12 shows, it incorrectly simulates the undershoot on the negative half of the output waveform. It does come reasonably close on

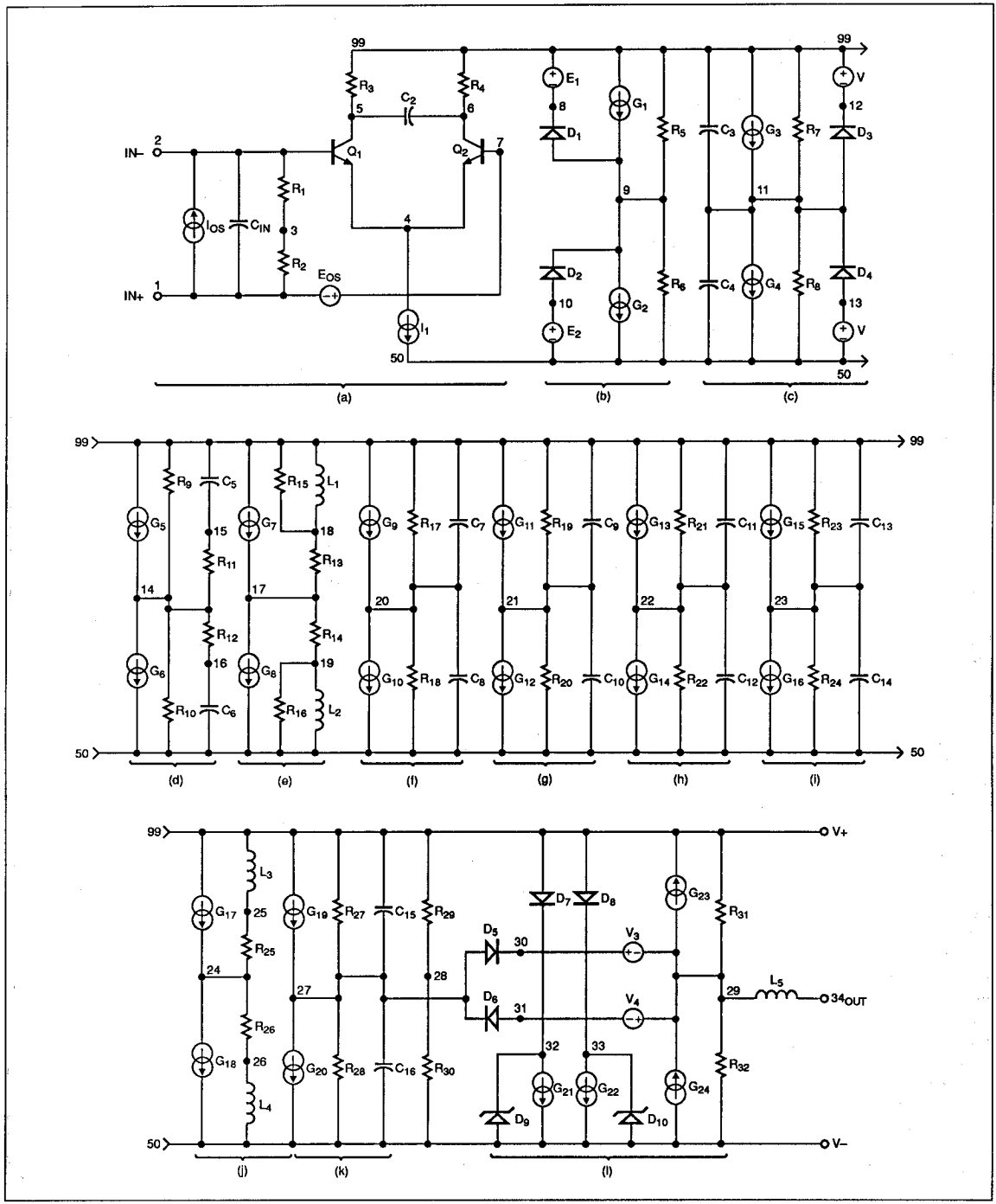

FIGURE 13: *The model schematic of the OP-61 looks similar to that of the OP-42, except that it has an additional gain stage.*

LISTING 2: OP-61 SPICE Macro-Model Net List

```
OP-61 MACROMODEL © PMI 1989
*
* SUBCKT OP-61  1  2 34 99 50
*
* INPUT STAGE & POLE AT 300 MHZ
*
R1    1    3        5E11
R2    2    3        5E11
R3    5    99       51.6
R4    6    99       51.6
CIN   1    2        5E-12
C2    5    6        5.141E-12
I1    4    50       1E-3
IOS   1    2        2E-7
EOS   7    1        POLY(1) 24 28 400E-6 1
Q1    5    2    4   QX
Q2    6    7    4   QX
*
* FIRST GAIN STAGE
*
R5    9    99       1E6
R6    9    50       1E6
G1    99   9        5 6 2E-4
G2    9    50       6 5 2E-4
E1    99   8        POLY(1) 99 28 -4.4 1
E2    10   50       POLY(1) 28 50 -4.4 1
D1    9    8        DX
D2    10   9        DX
*
* SECOND GAIN STAGE & POLE AT 2.5KHZ
*
R7    11   99       5.1598E6
R8    11   50       5.1598E6
C3    11   99       12.338E-12
C4    11   50       12.338E-12
G3    99   11       POLY(1)  9 28 4.24E-3 9.69E-5
G4    11   50       POLY(1) 28  9 4.24E-3 9.69E-5
V1    99   12       2.3
V2    13   50       2.3
D3    11   12       DX
D4    13   11       DX
*
* POLE-ZERO PAIR AT 4MHZ / 8MHZ
*
R9    14   99       1E6
R10   14   50       1E6
R11   14   15       1E6
R12   14   16       1E6
C5    15   99       19.89E-15
C6    16   50       19.89E-15
G5    99   14       11 28 1E-6
G6    14   50       28 11 1E-6
*
* ZERO-POLE PAIR AT 85MHZ / 300MHZ
*
R13   17   18       1E6
R14   17   19       1E6
R15   18   99       2.529E6
R16   19   50       2.529E6
L1    18   99       1.342E-3
L2    19   50       1.342E-3
G7    99   17       14 28 1E-6
G8    17   50       28 14 1E-6
*
* POLE AT 40MHZ
*
R17   20   99       1E6
R18   20   50       1E6
C7    20   99       3.979E-15
C8    20   50       3.979E-15
G9    99   20       17 28 1E-6
G10   20   50       28 17 1E-6
*
* POLE AT 200MHZ
*
R19   21   99       1E6
R20   21   50       1E6
C9    21   99       .796E-15
C10   21   50       .796E-15
G11   99   21       20 28 1E-6
G12   21   50       28 20 1E-6
*
* POLE AT 200MHZ
*
R21   22   99       1E6
R22   22   50       1E6
C11   22   99       .796E-15
C12   22   50       .796E-15
G13   99   22       21 28 1E-6
G14   22   50       28 21 1E-6
*
* POLE AT 200MHZ
*
R23   23   99       1E6
R24   23   50       1E6
C13   23   99       .796E-15
C14   23   50       .796E-15
G15   99   23       22 28  1E-6
G16   23   50       28 22 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 40KHZ
*
R25   24   25       1E6
R26   24   26       1E6
L3    25   99       3.979
L4    26   50       3.979
G17   99   24       3  28 1E-6
G18   24   50       28  3 1E-6
*
* POLE AT 300MHZ
*
R27   27   99       1E6
R28   27   50       1E6
C15   27   99       .531E-15
C16   27   50       .531E-15
G19   99   27       23 28 1E-6
G20   27   50       28 23 1E-6
*
* OUTPUT STAGE
*
R29   28   99       20.0E3
R30   28   50       20.0E3
R31   29   99       30
R32   29   50       30
L5    29   34       1.65E-7
G21   32   50       27 29 33.3333E-3
G22   33   50       29 27 33.3333E-3
G23   29   99       99 27 33.3333E-3
G24   50   29       27 50 33.3333E-3
V3    30   29       0.2
V4    29   31       0.2
D5    27   30       DX
D6    31   27       DX
D7    99   32       DX
D8    99   33       DX
D9    50   32       DY
D10   50   33       DY
*
* MODELS USED
*
.MODELI QX NPN(BF=1250)
.MODEL DX    D(IS=1E-15)
.MODEL DY    D(IS=1E-15 BV = 50)
.ENDS OP-61
```

the positive half, but the ringing frequency is lower than that of the real circuit.

This inability to model nonsymmetrical output-stage behavior is inherent in the Boyle approach and is still, unfortunately, shared by the new macro-model. However, it is a drawback that you can work around. If, during the model-generation process, you find that the overshoot is different from the undershoot, you should use the larger of the two values in calculations pertaining to the output inductor. Then with capacitive loads, the inductor value will yield the worst-case overshoot and undershoot results.

EXECUTION-TIME COMPARISONS

Assuming that no convergence problems exist in the macro-model, the time taken for SPICE to produce an operating-point calculation or a DC-transfer curve is largely a function of the number of circuit elements specified in the net list. Consequently, the new OP-42 macro-model was almost exactly twice as slow as its Boyle counterpart and required 2.27 times as many iterations to reach the final solution. Similar remarks apply to the AC-analysis case, where the run-time overhead of the new macro-model was almost exactly twice that of the Boyle macro-model. However, the two models required about the same number of iterations for AC-response simulation.

Evaluating the computational overhead for a transient analysis is quite difficult, because of the large number of factors involved. In particular, the new macro-model will exhibit considerably more detail than the Boyle model. The simulator must therefore use a much finer time step and perform correspondingly more calculations. However, the large number of ideal elements in the model results in a very good probability on convergence. Therefore, you can sometimes speed up the analysis by allowing more iterations per time step, a procedure which often allows the simulator to maintain a coarser time step and reduces the number of backtracks.

Most SPICE simulators default the number of transient iterations to 10. You can override this default by setting ITL4 to a larger number (say 40) in the .OPTIONS section. Additionally, relaxing RELTOL to 0.01 (the default value is usually 0.001) will also speed up the run time by slightly reducing the accuracy. This reduction is quite permissible because the macro-model is only an approximation anyway. Note, however, that Figures 11 and 12 were generated with RELTOL set to 0.001 rather than 0.01, so that the curves would be more accurate. Another way of speeding up the transient analysis is to use GEAR rather than TRAPEZOIDAL integration; however, such integration can generate results that appear considerably less oscillatory than they actually should be.

Using 0.01 for RELTOL, 40 for ITL4 and trapezoidal integration, the OP-42 macro-model proved to be 3.64 times slower on transient runs than the Boyle model and required 2.15 times as many iterations. The reduction in simulation speed, though large, is acceptable, and is outweighed by the advantage of greatly improved accuracy.

THE OP-61 MACRO-MODEL

The OP-61 is a bipolar-input, wideband, precision op amp that typically has a gain-bandwidth product of 200MHz (at a test frequency of 1MHz) and a slew rate of 40V/µs. The model of this device, shown in Figure 13, is only slightly more complicated than that of the OP-42. The OP-61's common-mode rejection starts to roll off at a lower frequency than the CMRR of the OP-42, but at 1MHz, it is still a respectable 80dB. The net list (see Lisiting 2) indicates that the OP-61 model requires 9 poles and 2 zeroes to mimic the open-loop frequency response, and a common-mode gain of zero at 40kHz.

Notice that this model has an additional gain stage (stage b in Figure 13) between the differential input stage and the main gain stage (see Figure 13c), which generates the dominant amplifier pole. The extra gain stage is necessary in this particular model because the OP-61 does not satisfy the limiting equation, which relates the slew rate, open-loop gain, and the dominant pole frequency for the bipolar input stage (see Box 1). The OP-61 model requires an open-loop gain of 100dB and slew rate of 40V/µs, but the gain-bandwidth product (and hence the dominant pole frequency) is too high to allow a single stage to generate all of the open-loop voltage gain.

Therefore, this model uses two gain stages, which together give the requisite 100dB of gain. The first gain stage has a gain of 200; the second has a gain of 500. You have to provide clamping in the first gain stage, in order to limit the maximum drive voltage applied to the voltage-controlled current sources in the second gain stage. This clamping action then limits the amount of peak current delivered to the compensation capacitors C_5 and C_6, and thus limits the maximum dV/dt in the second gain stage.

The first gain stage must provide a fair amount of gain, because the maximum differential output voltage of the input stage is only 51.6mV. To facilitate clamping with voltage sources and diodes, you need a much larger voltage. A gain of 200 in the first gain stage would result in an unclamped voltage of ±10.32V relative to V_h during slewing, but the clamping circuit limits this to approximately ±5.0V regardless of the rail voltages. This configuration allows reliable clamping action even when the power supply voltages are as low as ±4.4V. It also results in the desired slew rate of 40V/µs.

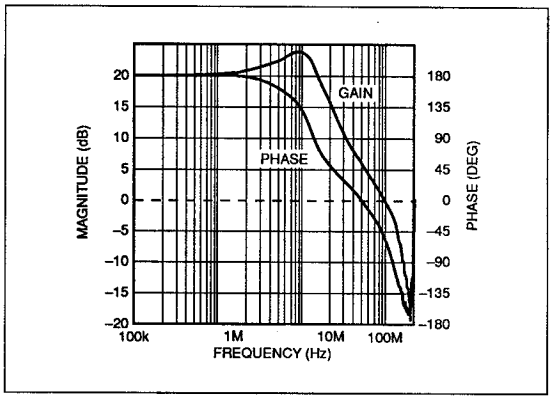

FIGURE 14: *When you connect a real OP-61 as an inverting amplifier with a gain of 10, the gain response shows a 3dB peak of 10MHz.*

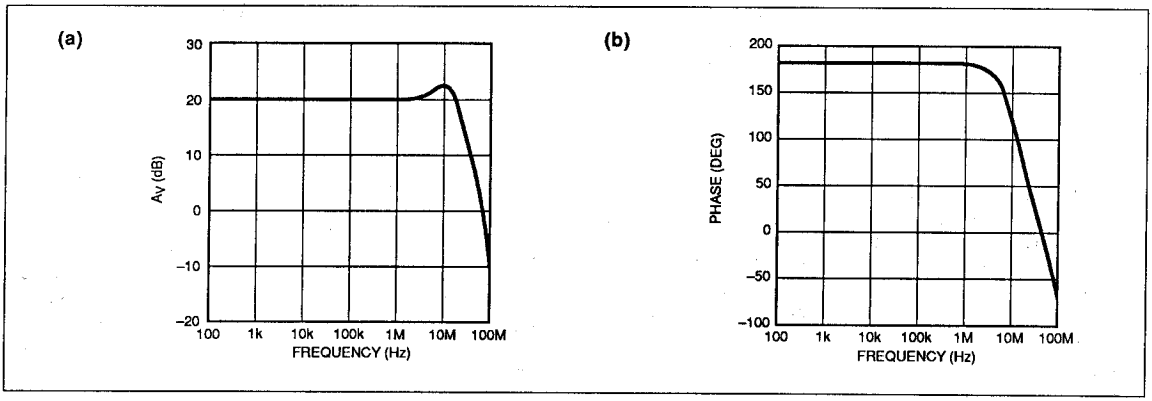

FIGURE 15: *The simulated gain (a) of the OP-61 macro-model shows the correct amount of peaking at 10MHz. Further, its phase response (b) at 40MHz differs by only 10° from that of the real device.*

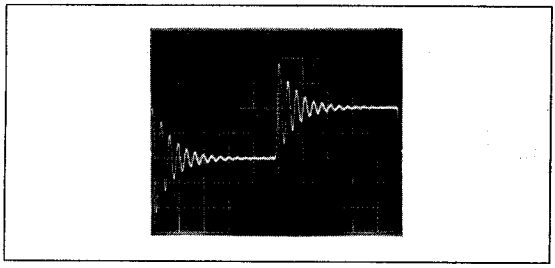

FIGURE 16: *The transient response of a real OP-61, when connected as an inverting amplifier with a gain of 10 and a capacitive load of 207pF, shows some asymmetry. The input signal is a 500kHz sqaure wave with a peak amplitude of 10mV. The vertical scale is 0.1V/div, and the horizontal scale is 0.2µs/div.*

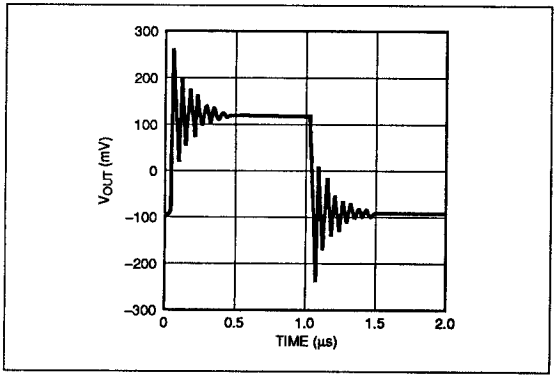

FIGURE 17: *The simulated transient response of the OP-61 macro-model quite closely matches the transient response of the real device.*

SIMULATION-ACCURACY COMPARISONS

Figure 14 shows the measured gain and phase responses of a physical OP-61 configured as an inverting amplifier with a gain of 10. Here, a 1kΩ feedback resistor, a 100Ω input resistor, and ±15V power supplies were used. The amplitude response exhibits a definite peak of about 3dB in the 10MHz region, and the phase shift also increases quite rapidly above 10MHz. The corresponding responses of the new macro-model (see Figures 15a and 15b) show excellent conformance to the measured gain response of the OP-61. The gain curve exhibits the requisite gain peak of slightly over 2dB just above 10MHz. The phase-response accuracy is also quite good; the error is only about 10° at 40MHz, and is probably within the range of variation one would expect to see on a breadboard because of parasitic capacitances and other physical effects. This new macro-model is therefore a useful tool in predicting the performance of the OP-61, even before you evaluate the breadboard.

Figure 16 shows the transient reponse of the OP-61, which might appear to be rather unstable until you notice that the device is driving a 207pF capacitive load. The waveform exhibits some asymmetry between the amounts of overshoot and undershoot (180% versus 220%), but the OP-61, like the OP-42, does not have a perfectly balanced output-stage structure. The choice of the output inductor (L_5 in the model) largely determines how closely the simulated transient response will mimic the real response. In fact, the simulation shown in Figure 17 yields symmetrical overshoot and undershoot of about 150%, which is a little low, and a ringing frequency which is a little high, compared to those of Figure 16. This discrepancy is unlikely to be of much importance to the user. If it is important, however, you could easily bring the simulated response closer to that of the real device by slightly increasing the value of the output inductor.

You can get some feeling for the performance of the new OP-61 model by comparing it to that of the OP-42 (no Boyle model of the OP-61 exists). For the DC bias point calculation, the OP-61 macro-model was faster than the OP-42 macro-model. For AC-response simulation, however, the OP-61 macro-model was slower by a factor of 1.18.

In the transient response simulations, the OP-61 macro-model took 1.76 times as long as the OP-42 macro-model and needed 1.56 times as many iterations. In this connection, you should remember that the simulation time of a transient run increases as the output becomes more oscillatory. Therefore, a direct comparison of the OP-42 and OP-61 execution times is not exactly fair because the OP-42's response is less oscillatory than that of the OP-61.

SIMULATION GOALS ARE CHANGING

The goal of any computer model is to accurately model some physical phenomenon; the more complex the phenomenon, the longer the time required for the computer to perform the necessary calculations. The goal of the Boyle op amp model was to reduce the number of nonlinear elements that required simulation, and hence to decrease the run time to an acceptable value. The Boyle model was not created with ultimate accuracy in mind, but it could correctly predict the low-frequency performance of an op amp, and was satisfactory for the relatively low-performance devices of its day.

Today, however, there is more and more demand for ever higher performance, and accurate prediction of a new device's performance can help to avoid design errors that would be expensive to correct at the manufacturing stage. Thus, accurate modeling of the high-frequency performance is essential, and in that region, the Boyle model is inadequate. The improved op amp macro-model described here not only models the high-frequency response and transient behavior of an op amp much more accurately than the Boyle model, but also does not need too much more CPU time to do its job. Today, with powerful desktop workstations available, the emphasis in modeling is on improving simulation accuracy rather than shaving every last bit from the execution times. The new macro-model is thus a good compromise.

The single most limiting factor of this new macro-model is that, for SPICE compatibility, the model must be written in the form of a net list with real circuit elements. Some new simulators (such as Saber, from Analogy Inc) allow you to define models in a specialized programming language that eliminates circuit-type constructs. The Saber modeling language, known as Mast, is very similar to C and allows powerful manipulation of internal variables. This feature would allow the output stage of the new macro-model, for example, to be completely described mathematically. A Saber model simply would not need all of the diodes and additional sources that the SPICE model requires for output-stage current correction. The defining equation for the output stage would directly take into account any load current that was being drawn from the model's output terminal. It is very likely that the new macro-model will be implemented in Saber at some time in the near future.

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