

Initial Design

1.0

Design Requirements

Parameter	Value
Minimum Input Voltage	10V
Maximum Input Voltage	14V
Nominal Input Voltage	12V
Input Voltage Ripple	1%
Output Voltage Programming	External Resistive Divider
Output Voltage	5 V
Output Current	2.5A
Load Step Start Current	1.25A
Load Step Current	2.5A
Output Voltage Ripple	2%
Output Voltage Load Step Over/Undershoot	5%
Performance Priority	Balance Efficiency and Size
BOM Priority	Cost
Inductor Current Ratio (LIR)	0.3
Mode of operation	PWM
Switching Frequency	700000Hz
Ambient Temperature	25°C



© 2018 Maxim Integrated. All rights reserved.

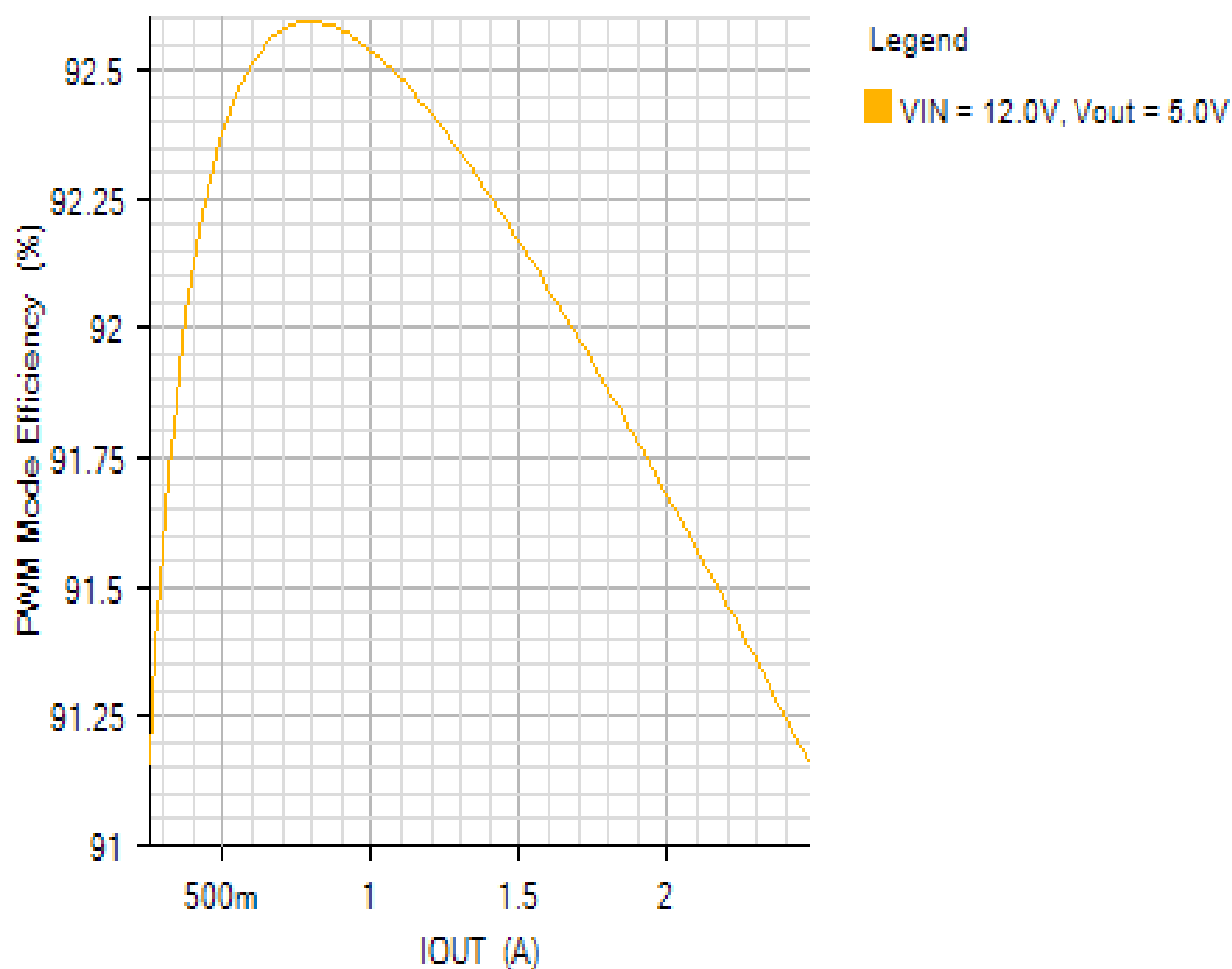
R2	1	TFCR0603-10W-E-2233FT-1K	Venkel	Res Thin Film 0603 223K Ohm 1% 0.1W(1/10W) ±25ppm/°C Pad SMD T/R
R3	1	ERJ3EKF4022V	Panasonic	Res Thick Film 0603 40.2K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
R4	1	ERJ2GEJ103X	Panasonic	Res Thick Film 0402 10K Ohm 5% 0.1W(1/10W) ±200ppm/°C Pad SMD Automotive T/R
R5	1	ERJ2RKF5622X	Panasonic	Res Thick Film 0402 56.2K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R

Simulation Results

Efficiency - Mon Nov 19 2018 18:18:11

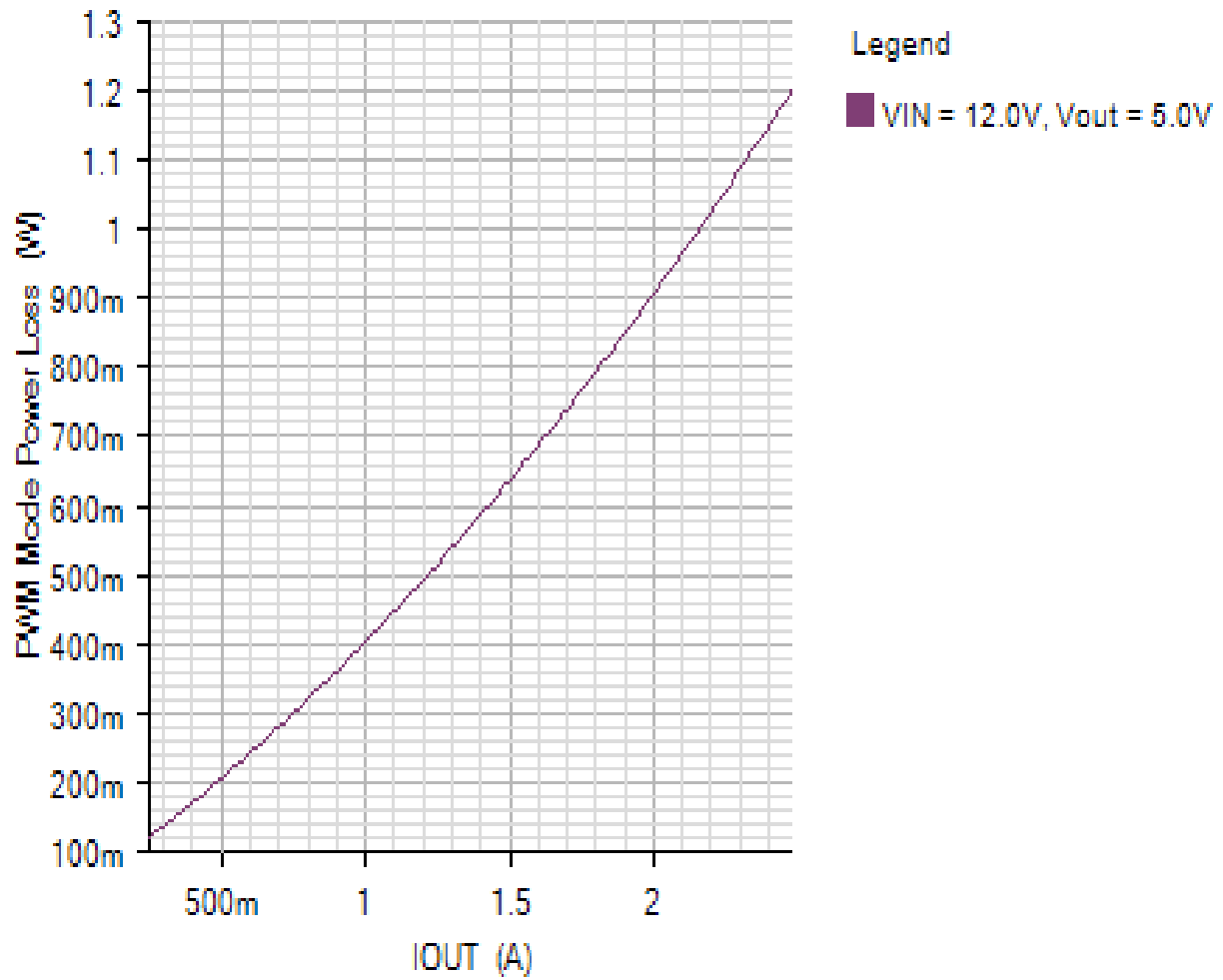
EFFICIENCY_PLOT

Default



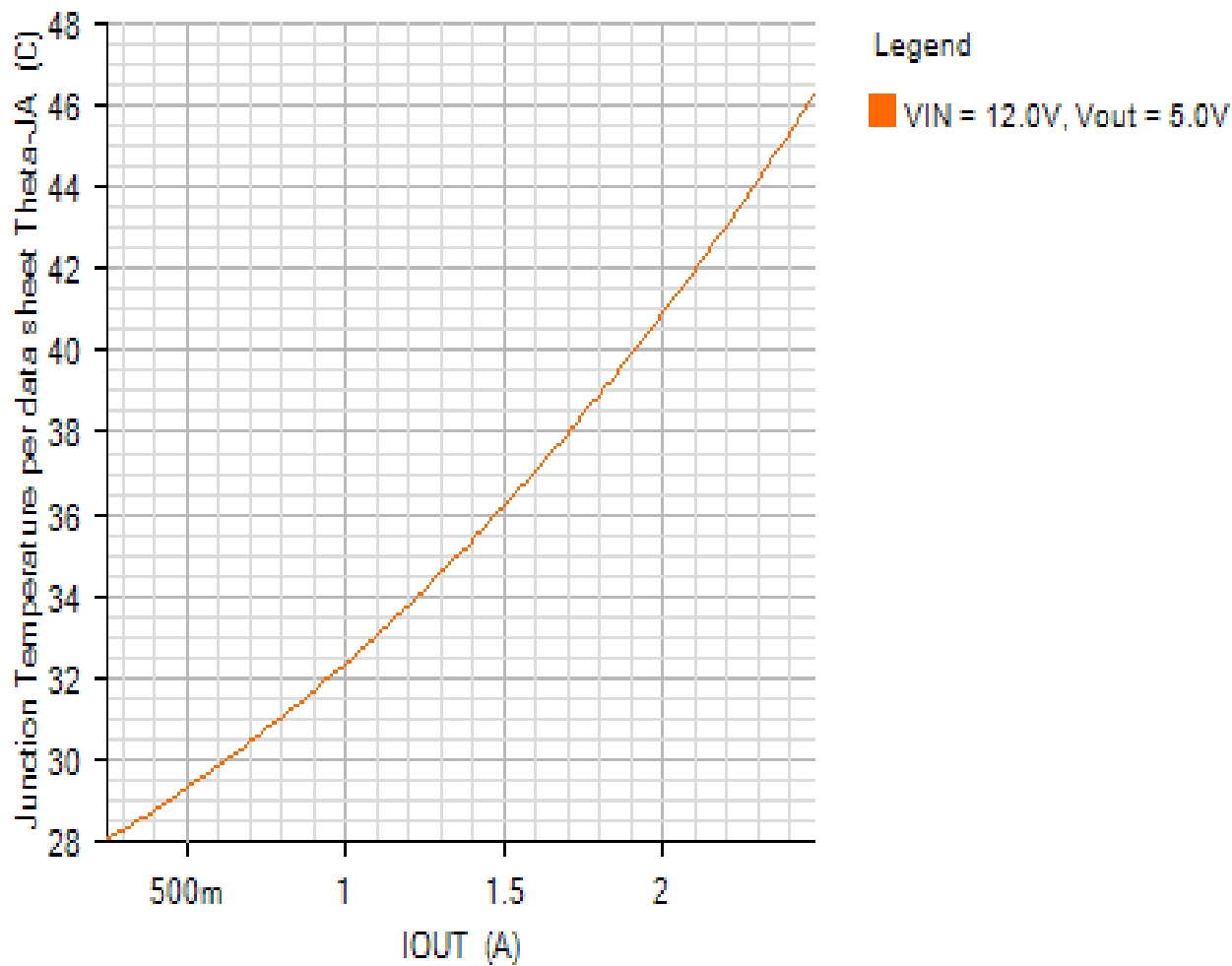
POWER_LOSS_PLOT

Default

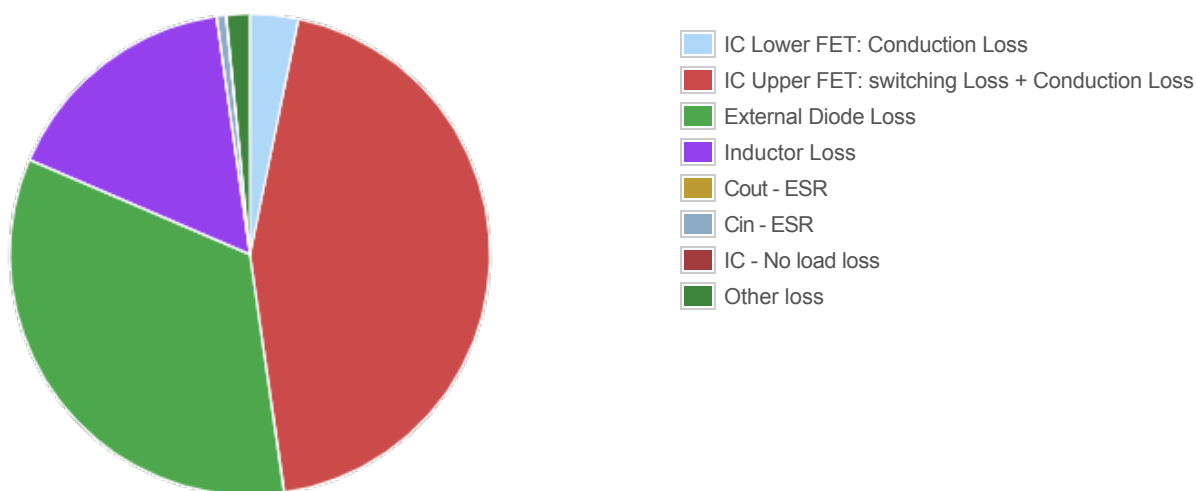


JUNCTION_TEMPERATURE_PLOT

Default



Losses



Component

Loss (W)

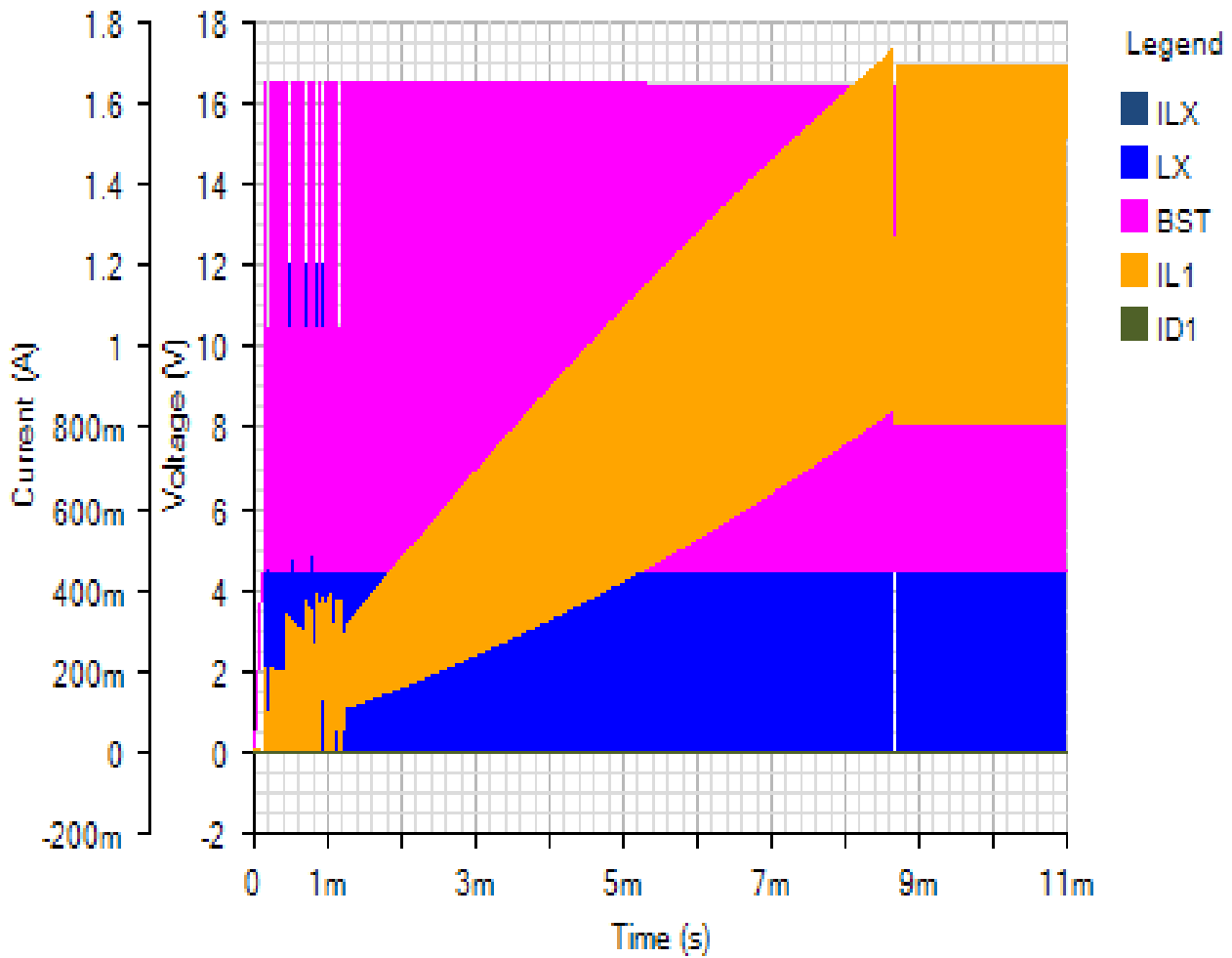
% of total

Component	Loss (W)	% of total
IC Lower FET: Conduction Loss	0.039	3.2
IC Upper FET: switching Loss + Conduction Loss	0.534	44.5
External Diode Loss	0.405	33.7
Inductor Loss	0.196	16.3
Cout - ESR	0.0001	0
Cin - ESR	0.0075	0.6
IC - No load loss	0.0003	0
Other loss	0.019	1.6
Total	1.2009	100

Start Up - Mon Nov 19 2018 18:18:11

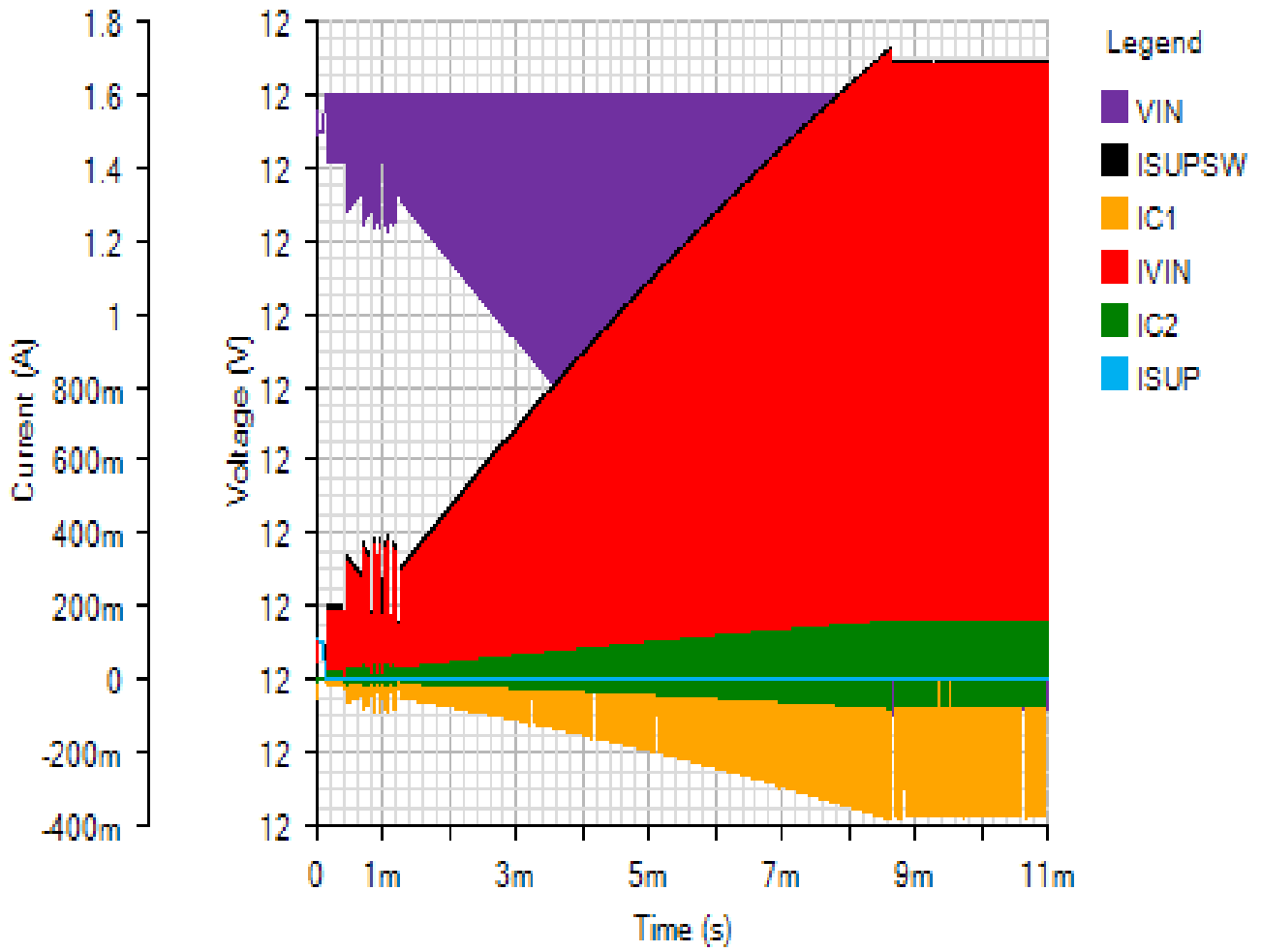
SWITCHING

Default



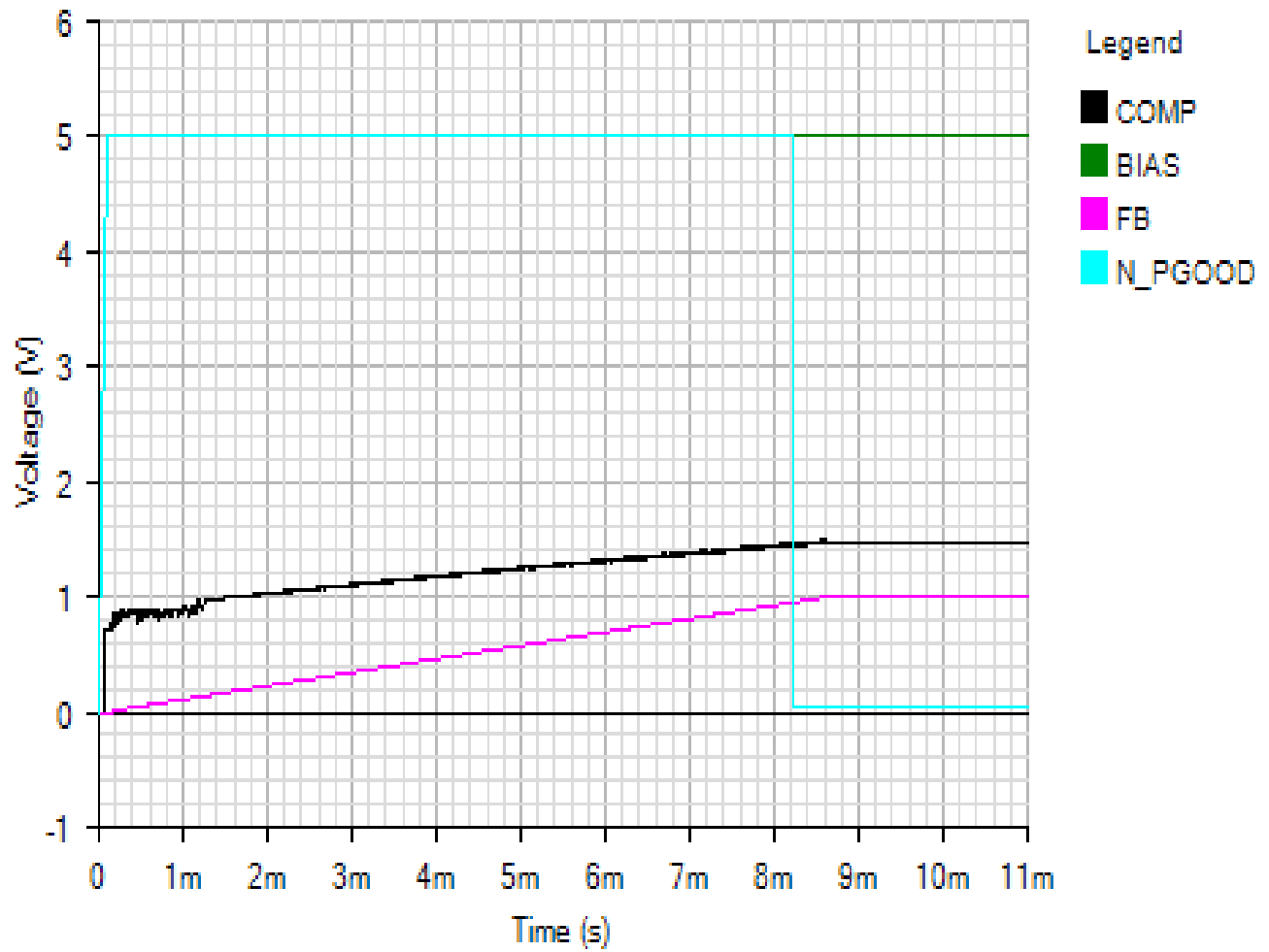
INPUT

Default



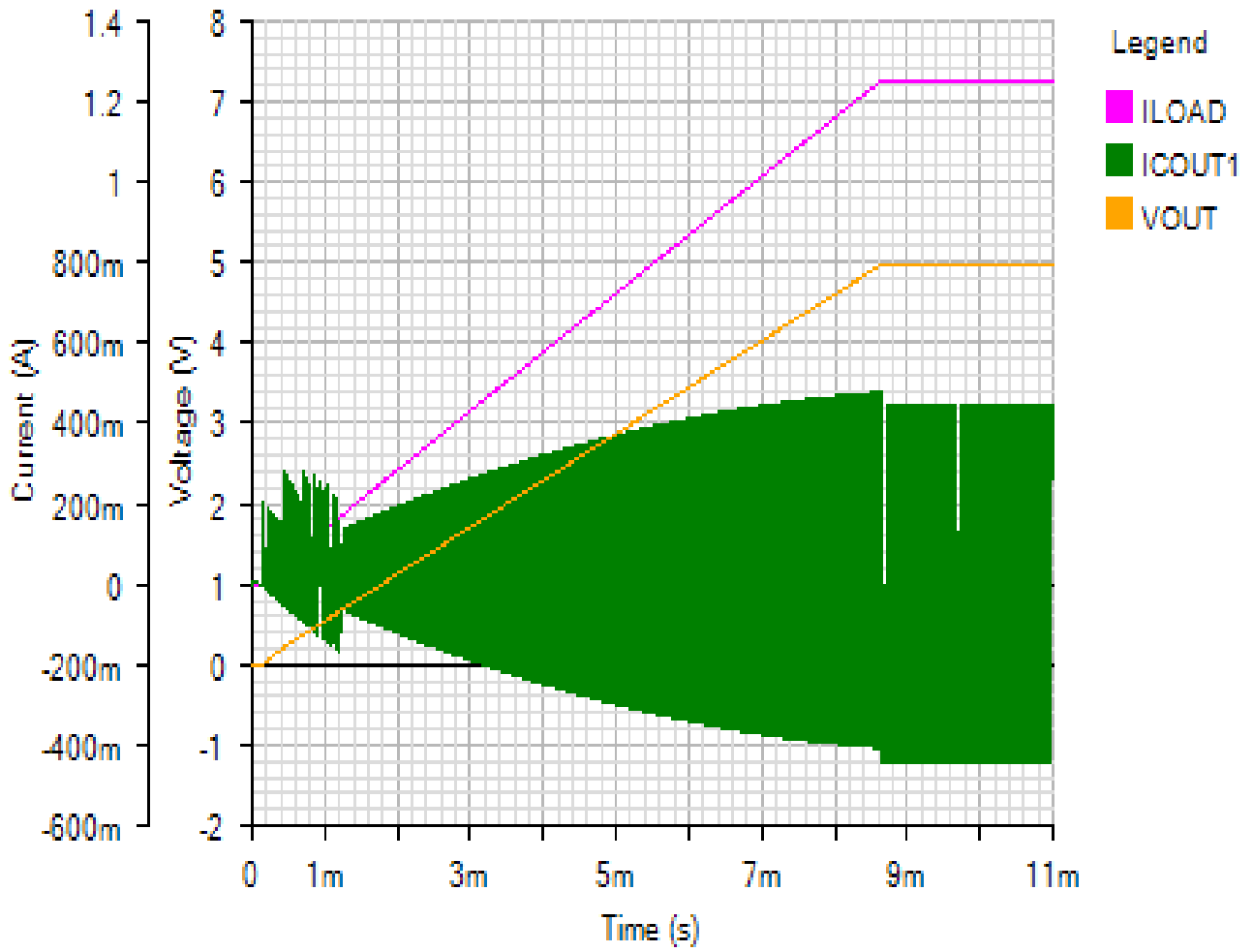
IC

Default



OUTPUT

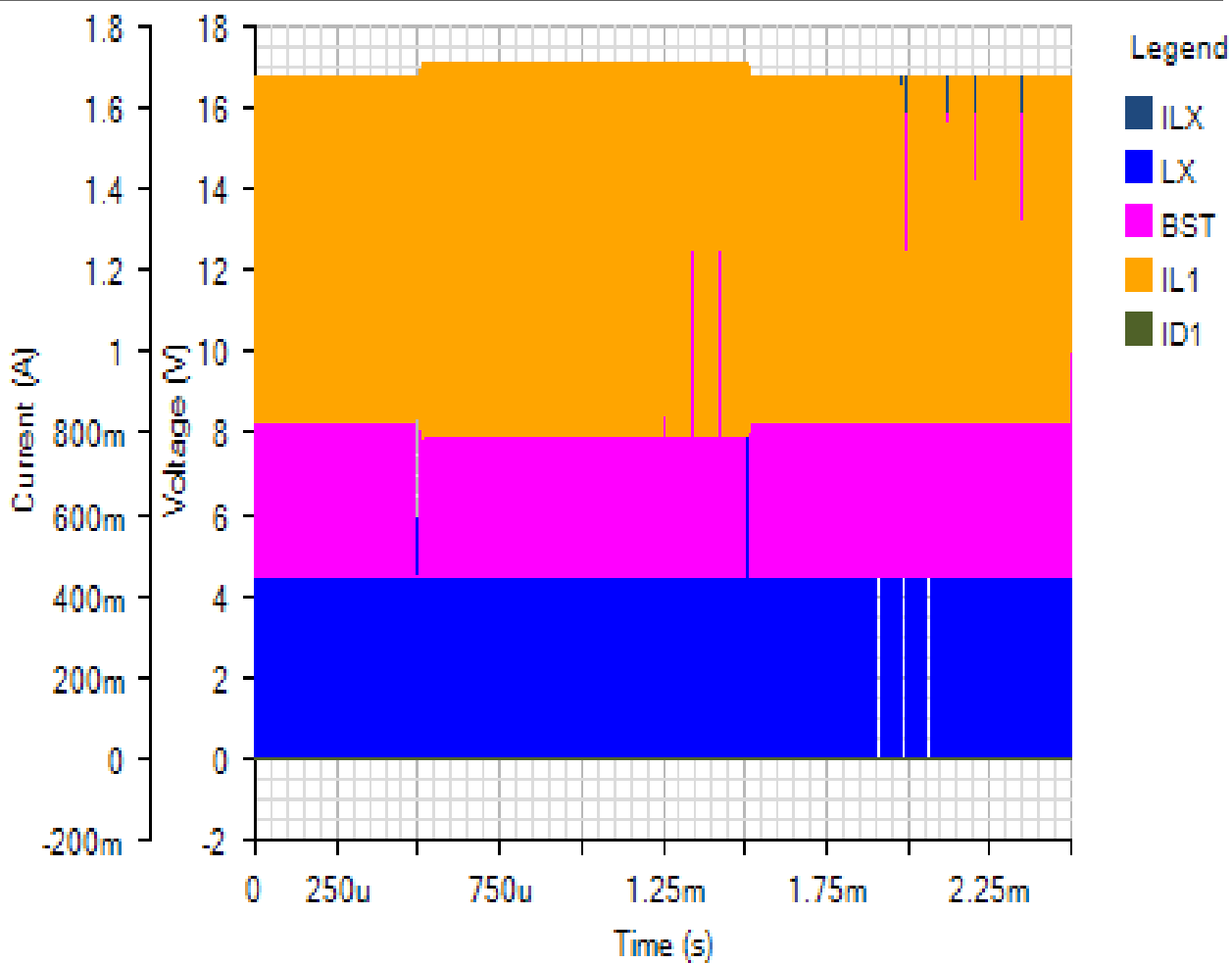
Default



Line Transient - Mon Nov 19 2018 18:18:11

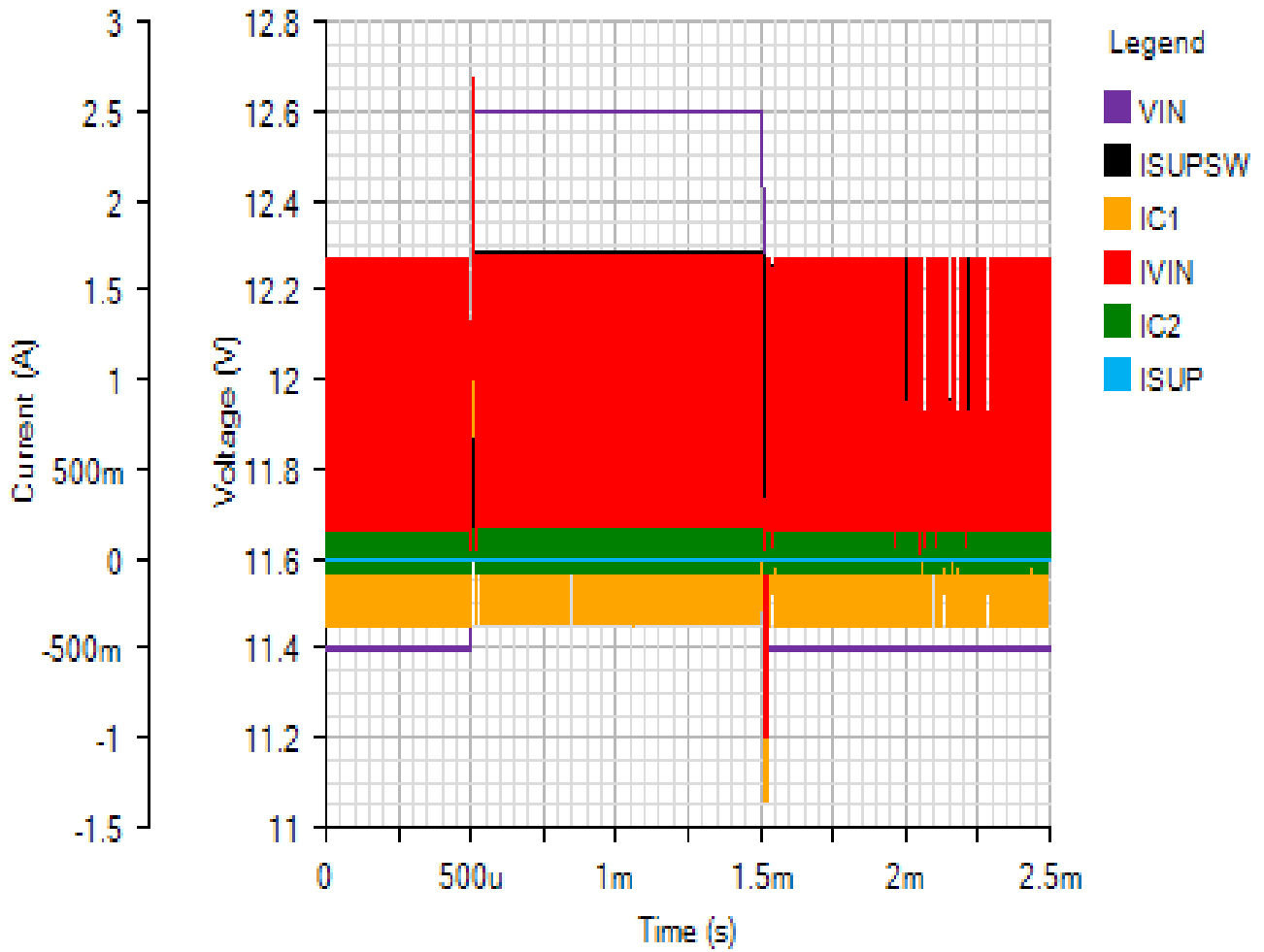
SWITCHING

Default



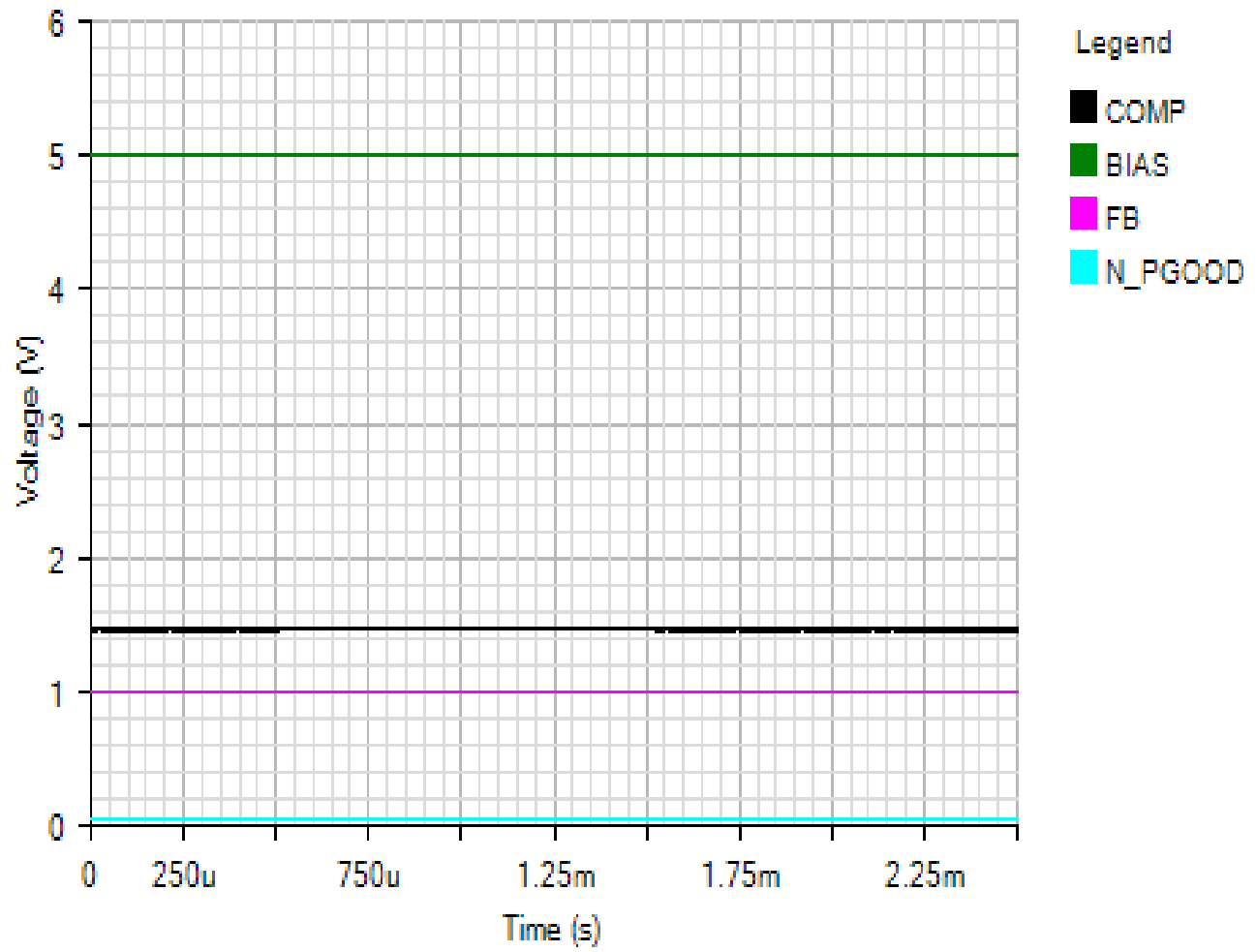
INPUT

Default



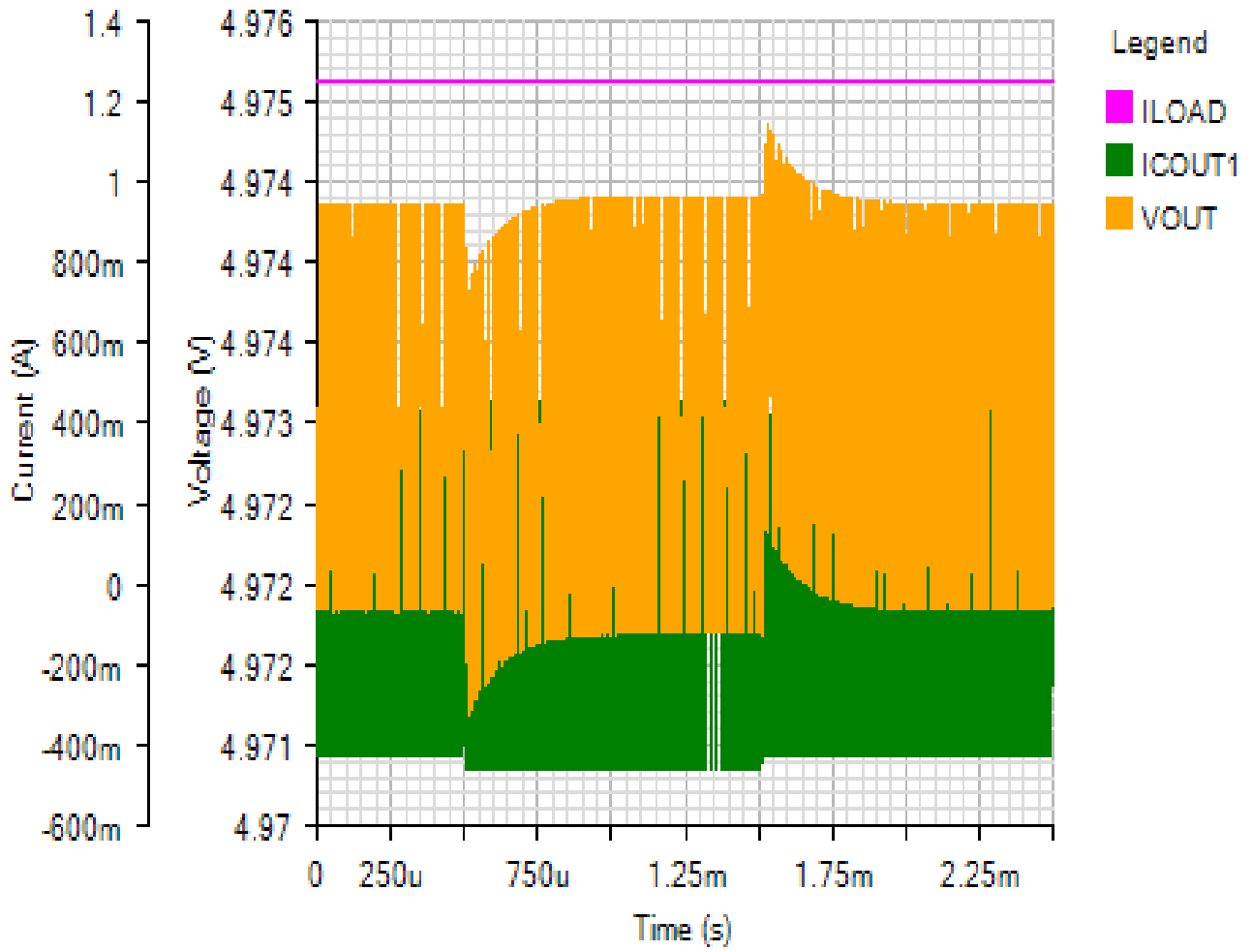
IC

Default



OUTPUT

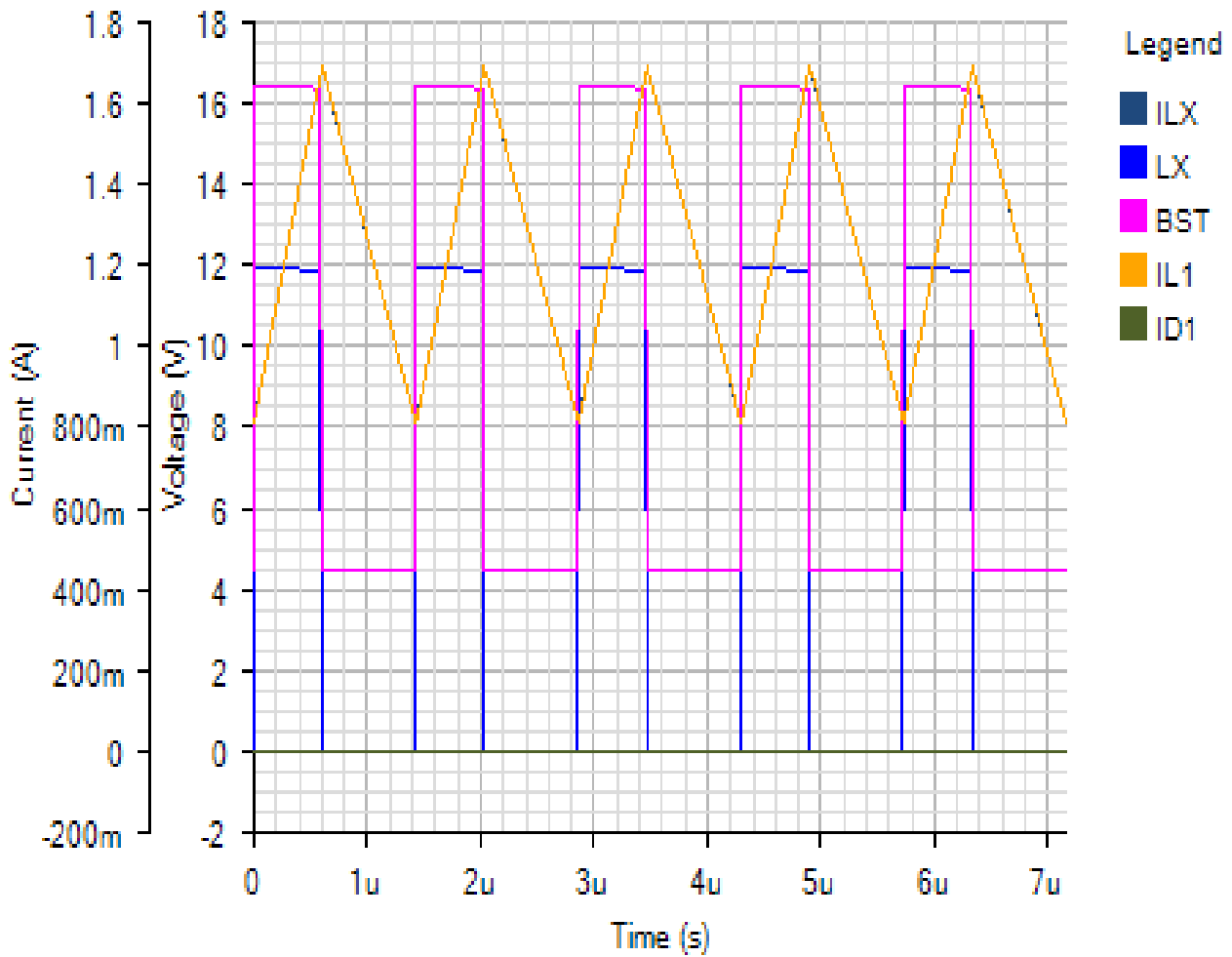
Default



Steady State - Mon Nov 19 2018 18:18:11

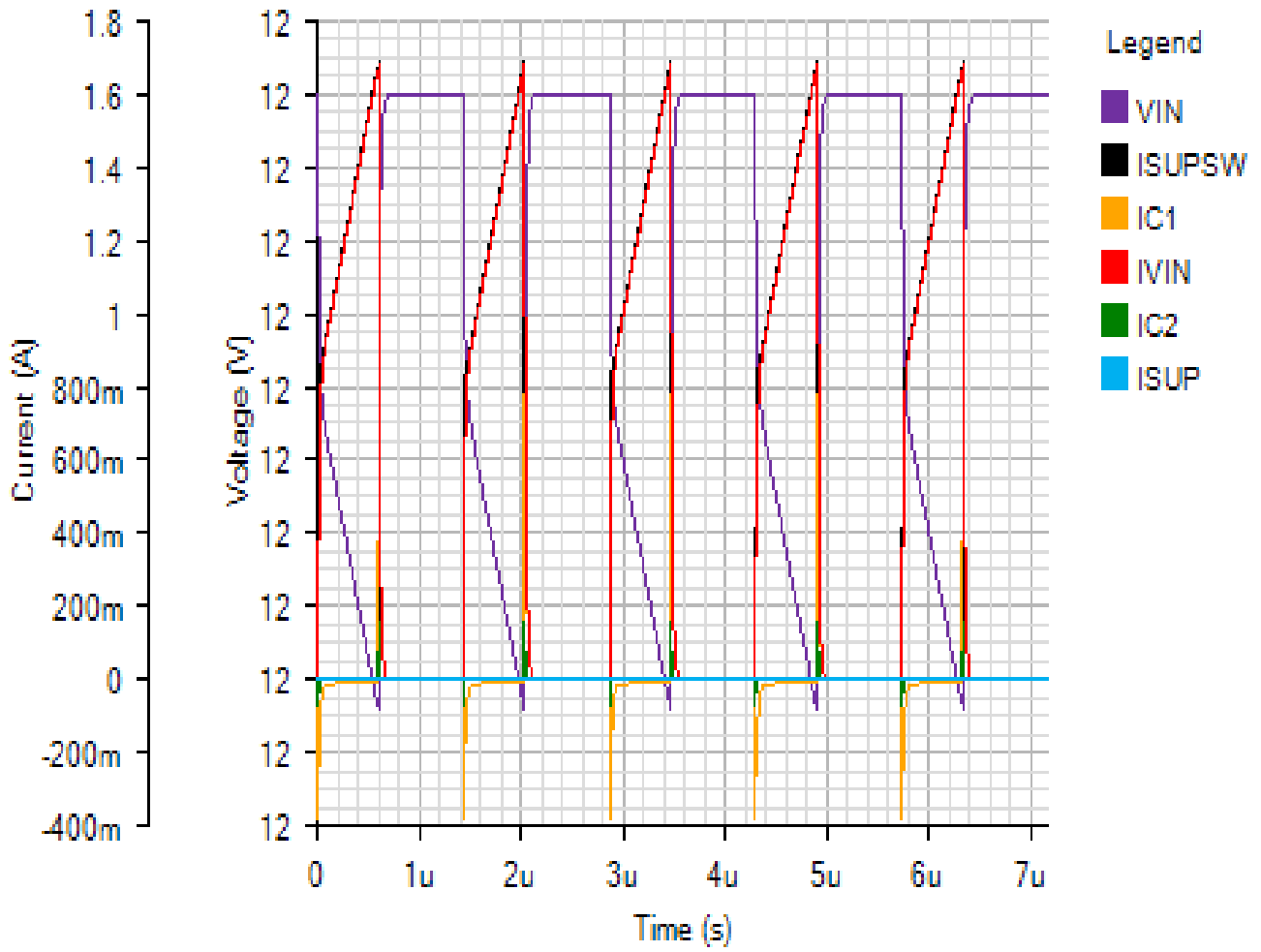
SWITCHING

Default



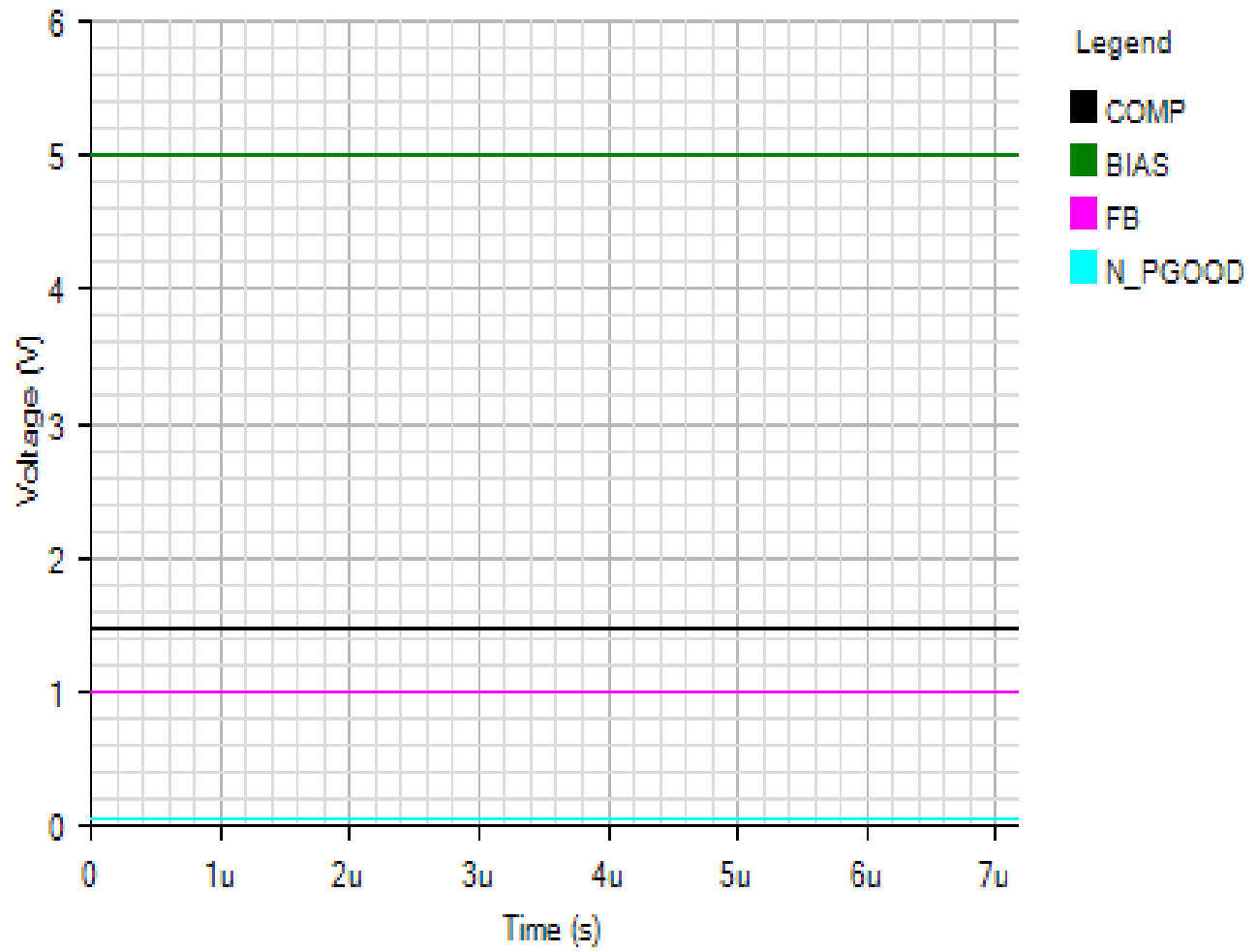
INPUT

Default



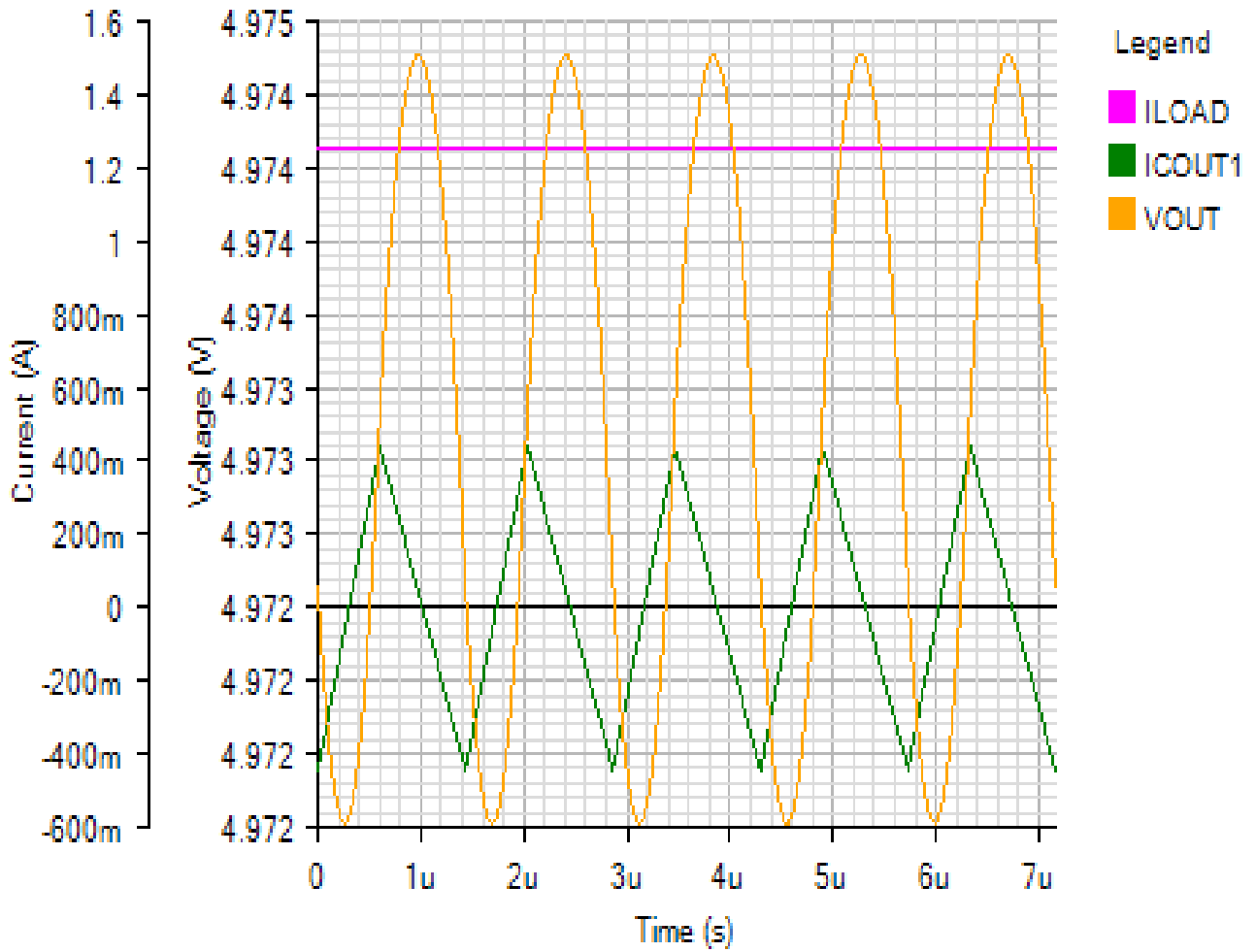
IC

Default



OUTPUT

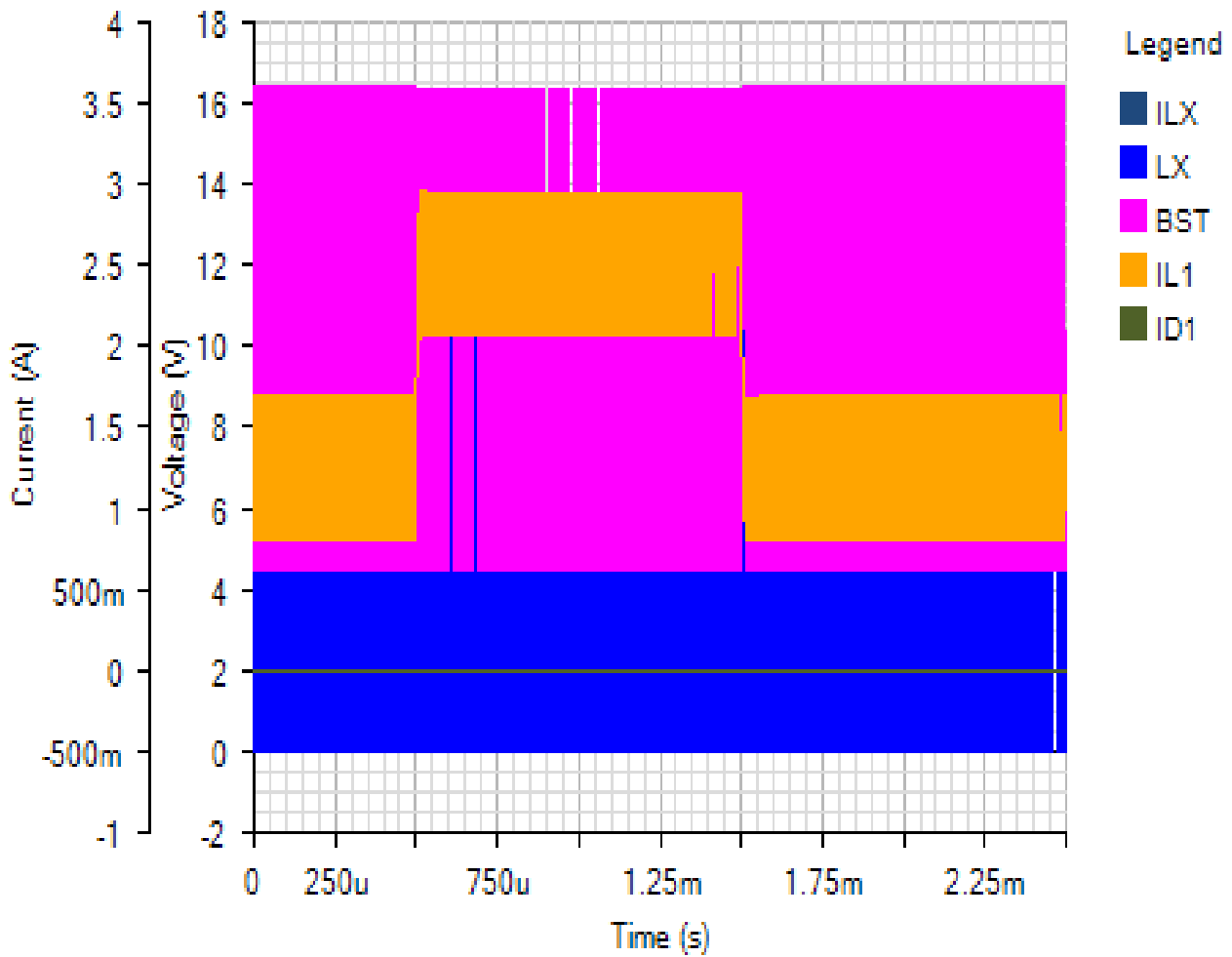
Default



Load Step - Mon Nov 19 2018 18:18:11

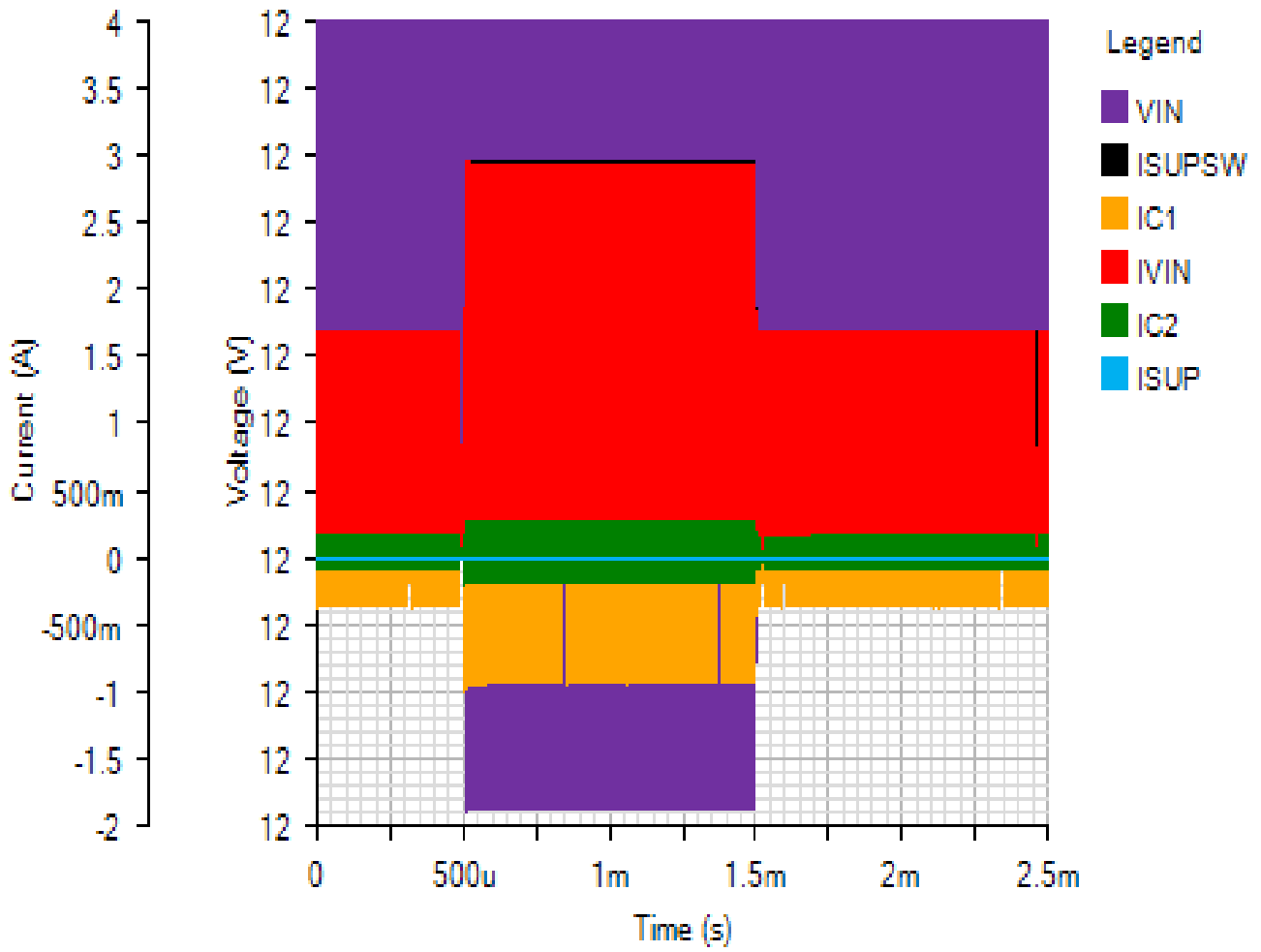
SWITCHING

Default



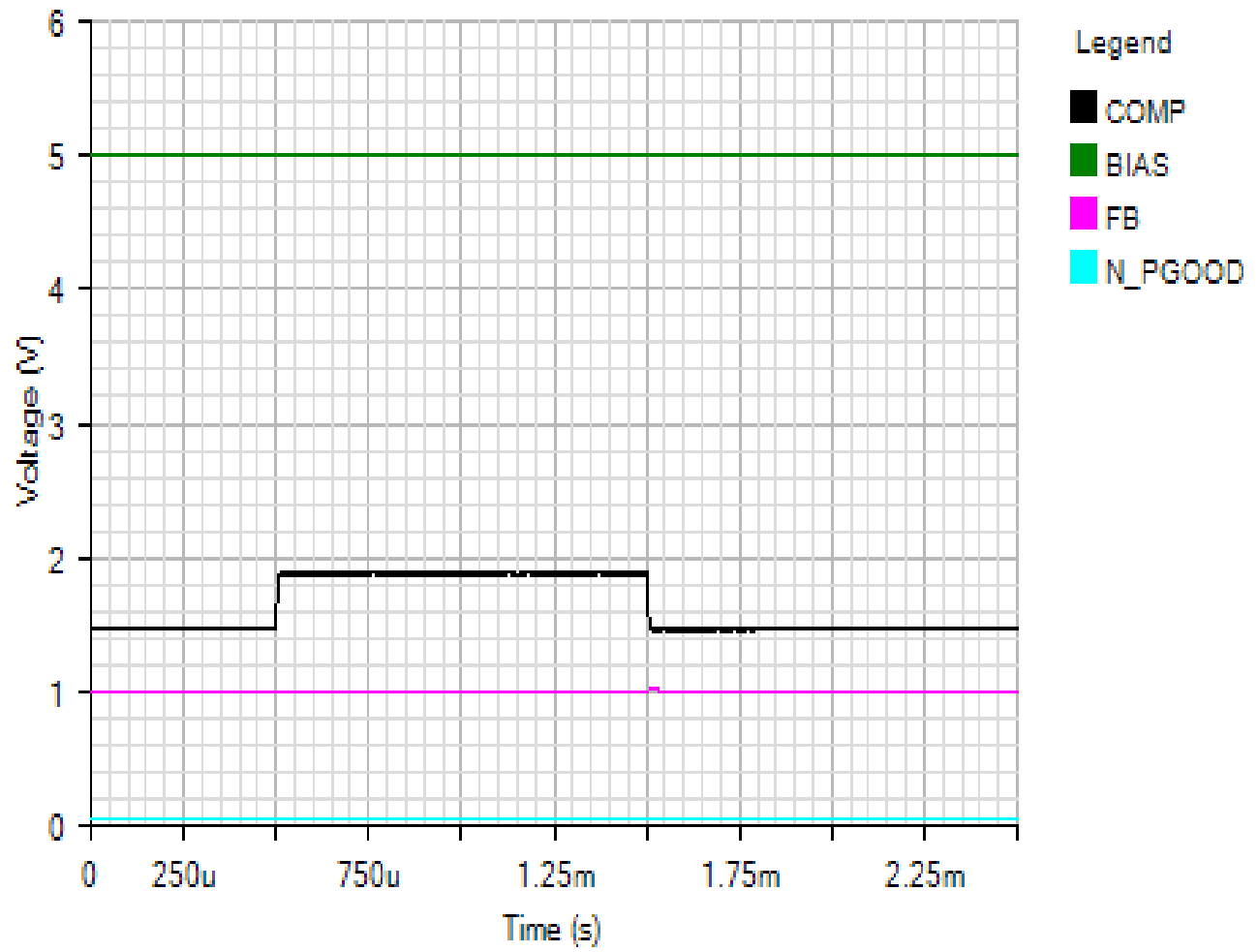
INPUT

Default



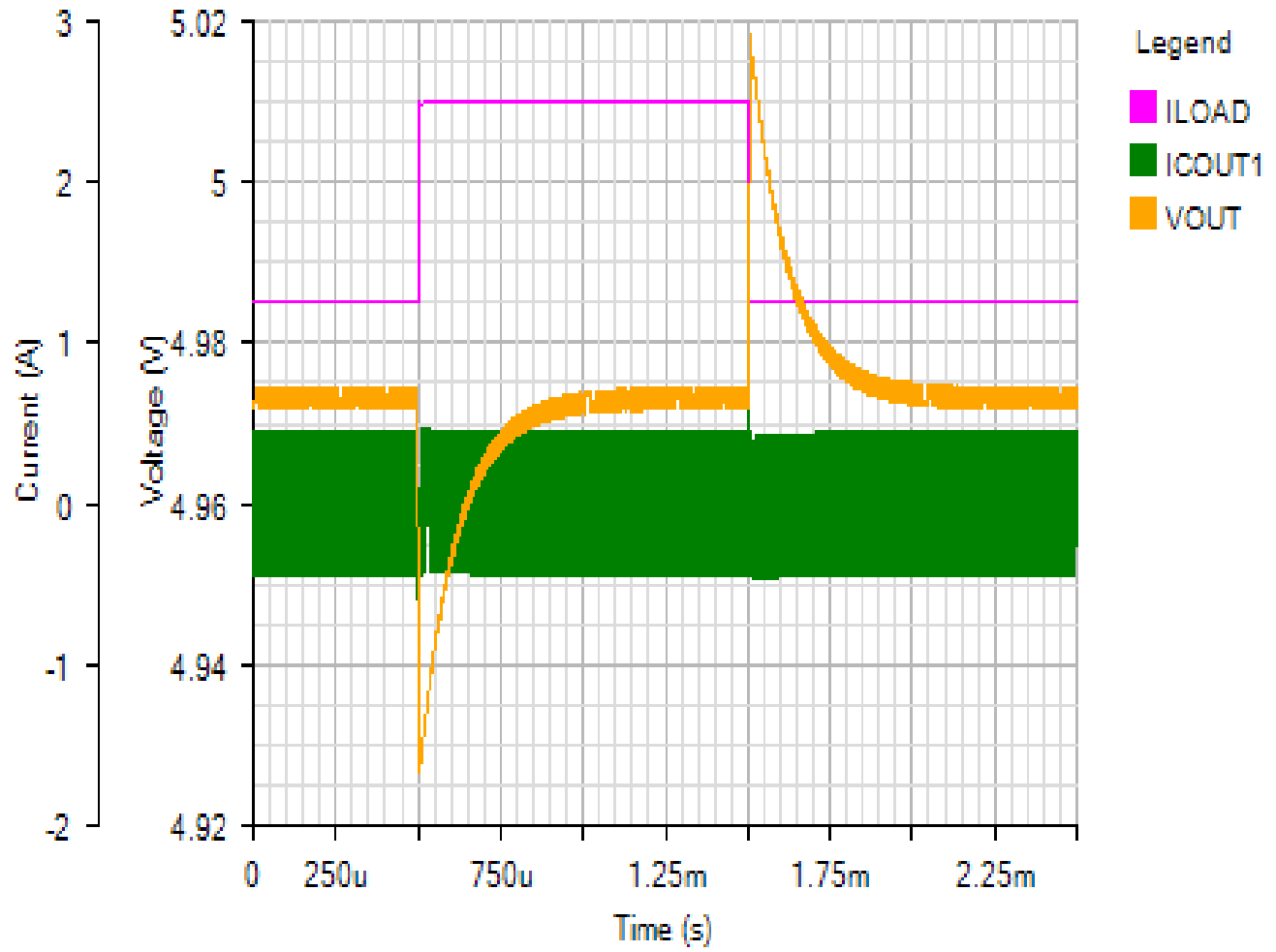
IC

Default



OUTPUT

Default



AC Loop - Mon Nov 19 2018 18:18:11

BODE

Default

