65W POE Solution Using the MAX5974A and MAX5995B

MAXREFDES1266

Introduction

The MAXREFDES1266 is a 65W, 24V Power-over-Ethernet (POE) solution that delivers up to 2.7A load current. The design is optimized for applications with a 37V to 57V input voltage range. The design is a fully assembled, surface-mount circuit board featuring an Ethernet port, network-powered device (PD) interface controller, and a downstream CCM flyback converter. The design receives power from an IEEE® 802.3bt-compliant power-sourcing equipment (PSE).

The MAXREFDES1266 employs a MAX5974A fixed-frequency, current-mode PWM controller in continuous mode flyback configuration. The MAX5974A features unique circuitry to achieve output regulation without using an optocoupler. The device features a unique feed-forward maximum duty-cycle clamp that makes the maximum clamp voltage during transient conditions independent of the line voltage, allowing the use of a power MOSFET with lower breakdown voltage. The programmable frequency dithering feature provides low-EMI, spread-spectrum operation.

The MAX5995B is used to provide a complete interface for a PD to comply with the IEEE 802.3bt standard in a POE system. It provides the PD with a detection signature, classification signature, and an integrated isolation power switch with startup inrush current control. The devices support a multi-event classification method, as specified in the IEEE 802.3bt standard. They provide a signal to indicate a Type 1 to Type 4 PSE. The devices can detect the presence of a wall adapter power source connection and allow a smooth switchover from the PoE power source to the wall power adapter. The devices also provide a power-good (PG) signal, two-step current limit, and foldback control and overtemperature protection.

Applications

- Industrial Power Supplies
- Access Control
- E-Buildings
- POE-Enabled Devices (e.g., IP phone, IP camera)

Benefits and Features

- Wide 37V to 57V input voltage range
- Highly regulated output voltage with ±1% ripple
- IEEE 802.3bt-compliant PD interface
- Multi-event classification
- Demonstrates a 65W PD design with isolated CCM flyback topology DC-DC converter
- 24V output at 2.7A
- Startup inrush current limit of 135mA (typ)
- Flyback controller internal UVLO at +16V
- Reduced BOM cost by employing primary sensing feedback
- High-efficiency flyback design using synchronous rectification

Hardware Specification

A 65W IEEE 802.3bt-compliant PD solution using the MAX5995B and MAX5974A is demonstrated for 24V DC output application. The power supply delivers up to 2.7A at 24V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	37V	57V
Frequency	f_{SW}	250kHz	
Output Voltage	V_{OUT}	24V	
Output Current	I_{OUT}	0	2.7A
Output Voltage Ripple	ΔV_{OUT}	1% of V_{OUT}	
Output Power	P_{OUT}	65W	
Maximum Efficiency	η	90%	

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Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a POE power-supply solution using the MAX5995B and MAX5974A. The power supply has been built and tested, details of which follow later in this document.

Power-Over-Ethernet (POE)

POE is a technology that delivers data and power at the same time over a single Ethernet cable. The power is delivered from the PSE and to a load through a PD controller. In the previous IEEE af/at standard, only a two-pair cable was used. In the 3bt standard, a four-pair cable is used for higher power level. For example, the new Type 4 PD is up to 71W. The POE solutions eliminate AC wall adapters and deliver data and power over a single cable. This means they are more economical and compact in size without the need of the bulky AC wall adapter. It is simple, convenient, safe, and easy to use because of the plug-and-play feature. The following are the types of POE standards and their equivalent PD output power capabilities:

1) IEEE802.3af/Type1: 12.95W
2) IEEE802.3at/Type2: 25.5W
3) IEEE802.3bt/Type3: 51W
4) IEEE802.3bt/Type4: 71W

POE technology is used in a lot of applications like wireless access points, IP cameras, IP phones, etc. These applications require less than 25W, which can be supported by af/at POE. The 3bt POE, on the other hand, delivers higher power levels and supports applications like LED lighting or IP door controls. A few examples of products that work on POE technology are shown in Figure 2.

As mentioned, the 3bt POE uses four-pair cables to deliver power. With a four-pair cable, the power delivery is increased to meet higher power demand. For the same load current, the four-pair cable is more efficient since the cable resistance is reduced by half. In addition, a four-pair cable can achieve a faster data transmission speed. Thus, the applications of four-pair POE solutions are driven by:

- Increased power demand: Products such as surveillance, RF, LED lighting that utilize high power are made possible with a four-pair cable.
- High power efficiency: For the same load currents, four-pair cables are more efficient than two-pair delivery.
- High data rate: PoE support for 10BASE-T (10Mbps), 100BASE-T (100Mbps), 1000BASE-T (1Gbps).
- Backward compatibility.

Figure 1: MAXREFDES1266 hardware.

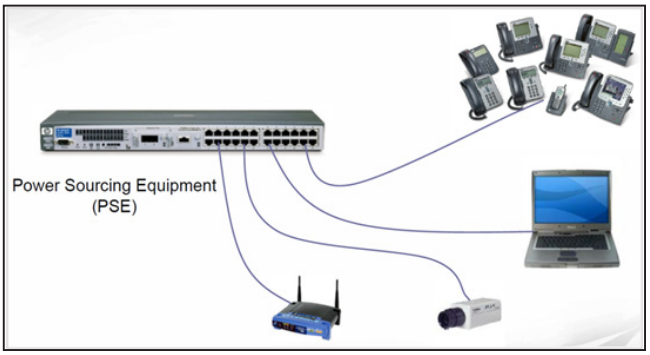

Figure 2: POE equipment examples

POE PD System Using MAX5995B and MAX5974A

A typical four-pair POE PD solution using the MAX5995B and MAX5974A is shown in Figure 3.

The PD receives its power from an IEEE 802.3at-compliant PSE. The PSE provides the required 37V to 57V DC power over a twisted-pair Ethernet network cable to the RJ45 connector on the PD device. The design features a 1 x 1Gb RJ45 connector, LAN transformer, and an active diode bridge that separates the DC power provided by the PSE end-span or midspan Ethernet system. If an active bridge is not available, then two separate diode-bridge rectifiers can also be used. The PD POE interface is provided by the MAX5995B to switch on or off the downstream MAX5974A CCM flyback.

PD Switch Using MAX5995B

The MAX5995B provides a complete interface for a PD to comply with the IEEE 802.3bt standard in a PoE system. The device supports a multi-event classification method, as specified in the IEEE 802.3bt standard, and provides a signal to indicate from Type 1 to Type 4 PSE. Depending on the input voltage (V_{IN} = V_{DD} - V_{SS}), the devices operate in four different modes:

1) PD detection
2) PD classification
3) Mark event
4) PD power

In detection mode, the PSE applies two voltages on V_{IN} in the 1.4V to 10.1V range (1V step minimum) and then records the current measurements at the two points. The PSE then computes ΔV/ΔI to ensure the presence of the 24.9kΩ signature resistor. In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. Two external resistors connected CLSA and CLSB pins to V_{SS} set classification signature to the PSE and define the power consumption requested from the PD. R_{CLSA} sets the classification current for the first- and second-class events for a 0~4-class PD compliant with the IEEE 802.3af/at standard. IEEE 802.3bt defines the physical classification that allows a PD to communicate its power classification to the connected PSE and then allows the PSE to inform the PD of the PSE's available power. The MAX5995B enters power mode when V_{IN} rises above the undervoltage-lockout threshold (V_{ON}). When V_{IN} rises above V_{ON} = 35V, the devices turn on the internal n-channel isolation MOSFET to connect V_{SS} to RTN. Thus, in power mode, the downstream flyback starts supplying power to the load. For detailed information about multi-event classification, please see the MAX5995B datasheet.

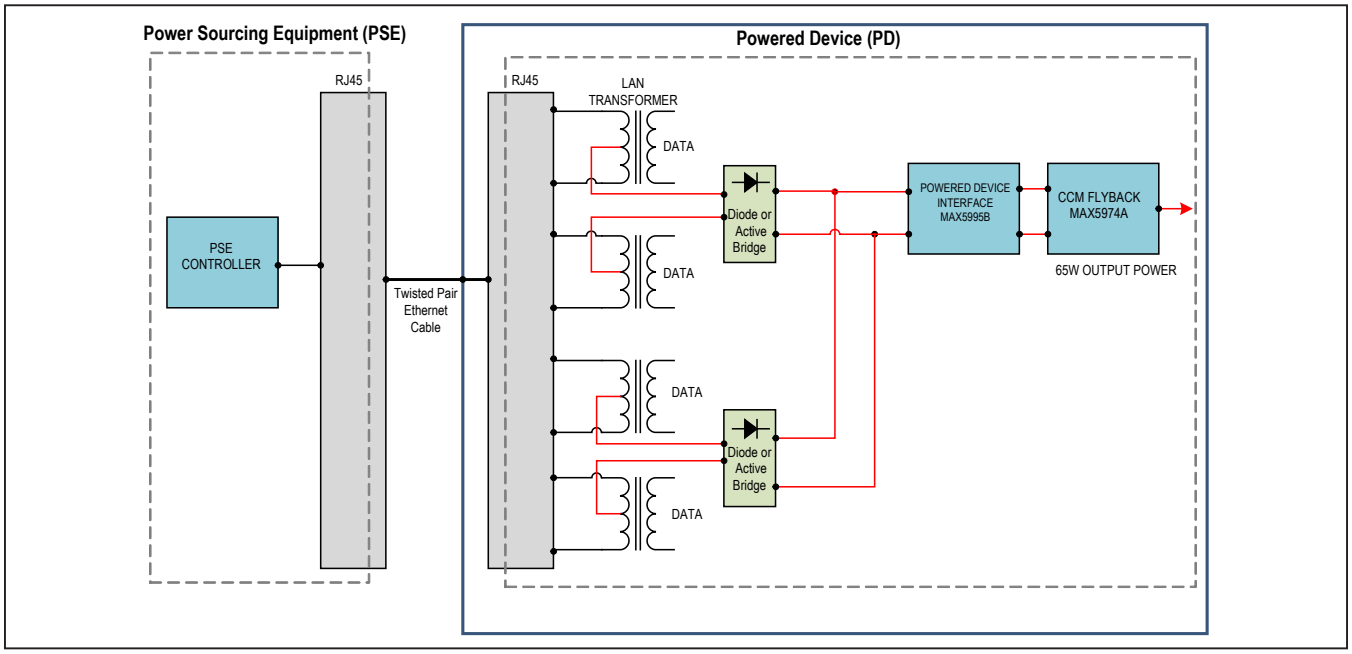

Figure 3. POE PD architecture using MAX5995B and MAX5974A.

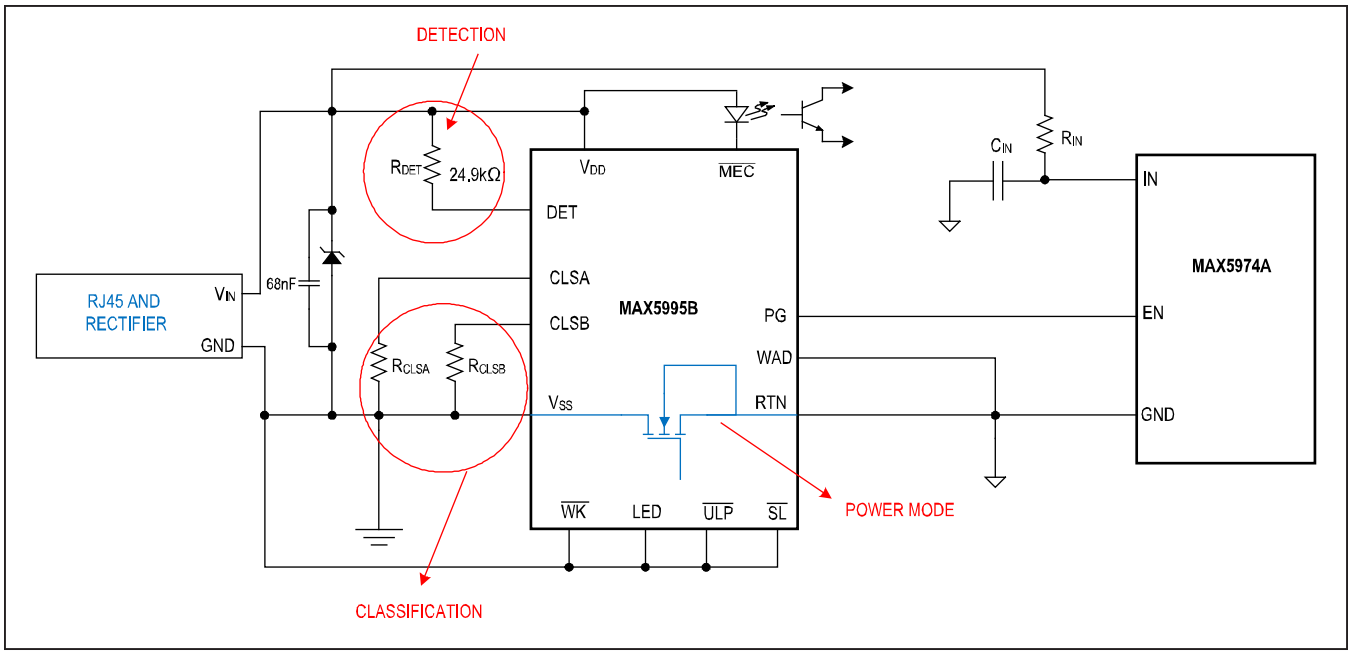

Figure 4: MAX5995B POE interface modes of operation.

Flyback Principle

A simple flyback topology consists of a transformer whose primary winding is connected to ground through a switch (usually a switching MOSFET). The switch is turned on and off by using a PWM signal. The secondary winding has a diode and an output capacitor. A simple representation schematic of a flyback is shown in Figure 5.

When the primary switch is closed, a current, I_{LP}, flows through the primary winding as shown in Figure 6. In the secondary winding, a negative voltage is induced due to the current flowing into the primary. The rectifier diode is reverse-biased and no current flows into the secondary winding during this time. The induced voltage in the primary is written as:

$$V_S = L_S \frac{dI_{LP}}{dt}$$

When the primary switch opens, the magnetic field in the primary winding collapses and the voltages at the windings reverse while current keeps flowing in the same direction until the field did fades away as shown in Figure 7. At the secondary, the diode is now forward-biased and the voltage at the secondary winding now equals the desired output voltage, V_{OUT} (ignoring diode drop). The secondary current, I_{LS}, flows and the secondary voltage, V_{OUT}, flies back to the primary side as V_{OUT}/k.

$$V_{SW} = V_{IN} + \frac{V_{OUT}}{k}$$

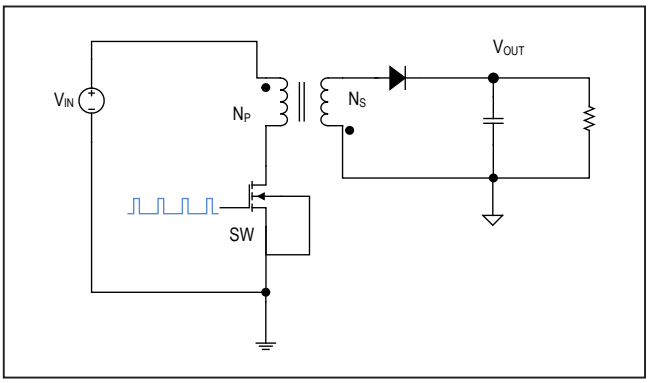

Figure 5: A simple flyback topology.

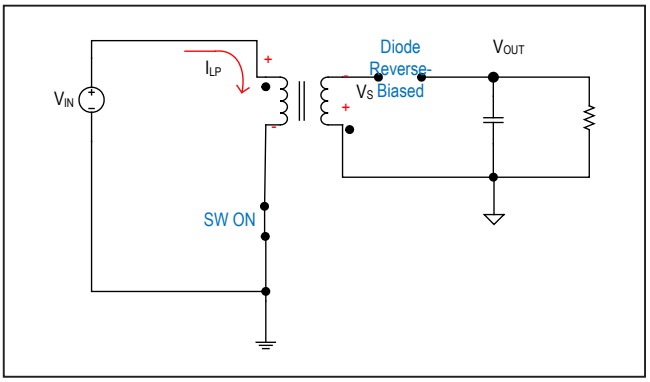

Figure 6: Flyback equivalent circuit when the primary switch is ON.

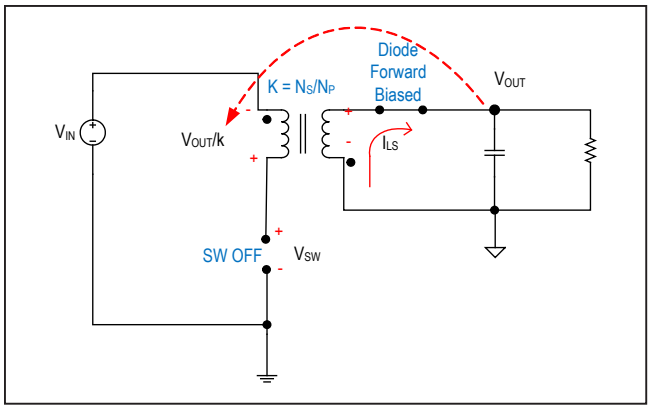

Figure 7: Flyback equivalent circuit when the primary switch is OFF.

This voltage also causes the breakdown of the magnetic flux in the primary winding (no current flows into the primary winding after this reset). In a transformer, current usually flows in both windings at the same time (it does not store energy). In a flyback topology, only one winding conducts at a time. Therefore, the transformer used in flyback circuits is also called a "coupled inductor."

Flyback DCM vs. CCM

The flyback converter can be designed to operate either in continuous or discontinuous mode of operation. In DCM, discontinuous conduction mode of operation, the transformer core completes its energy transfer during the off cycle. Thus, there is no residual energy in the inductor at the beginning and end of the switching period.

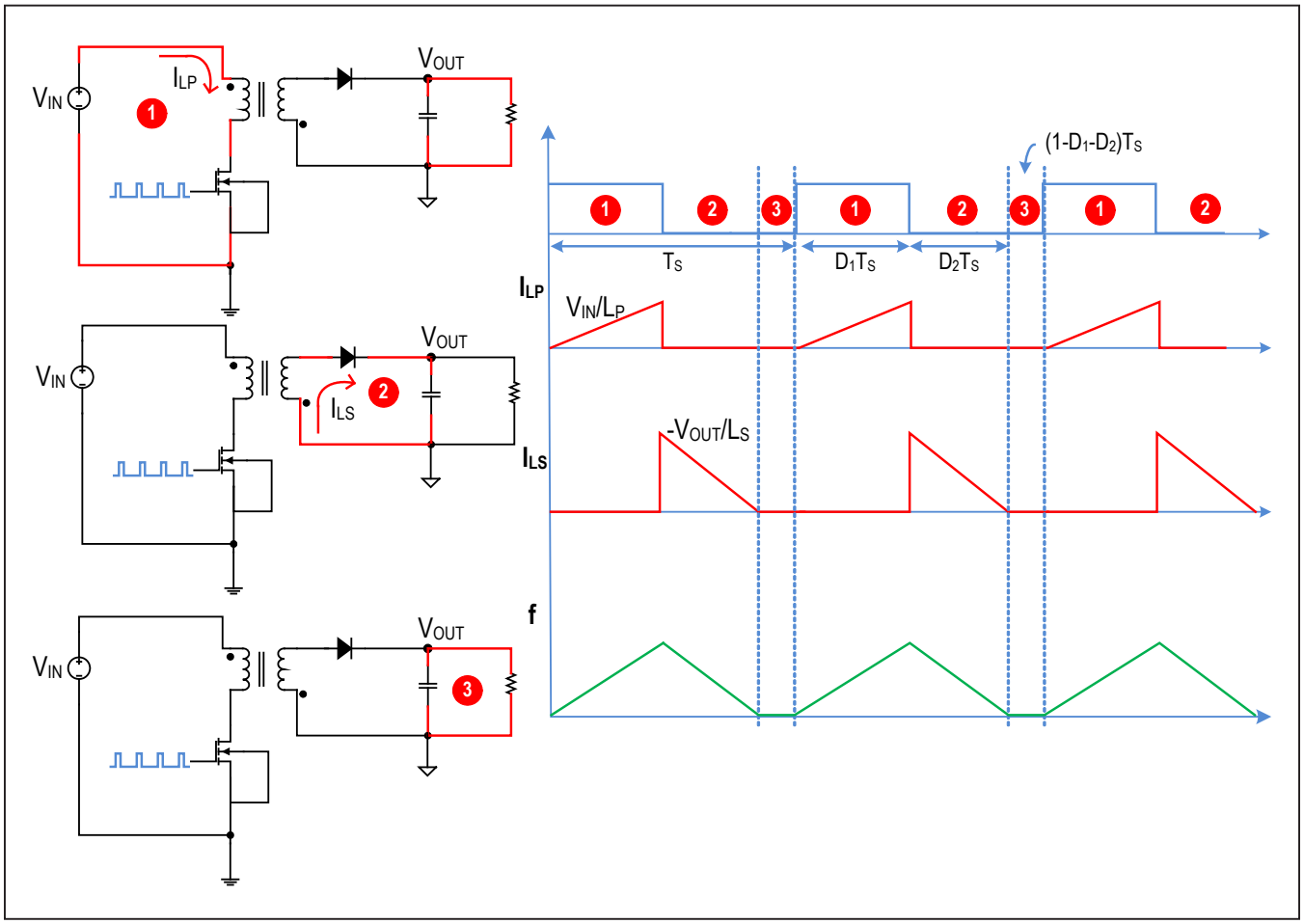

Figure 8: Discontinuous conduction mode operation of a flyback.

In CCM or continuous mode of operation, the next cycle begins before the energy transfer is complete in the inductor as shown in Figure 9. Thus, in CCM mode, the coupled inductor has residual energy at the beginning and end of the switching periods.

The DCM topology has the following salient features:

1) It maximizes the energy storage in the magnetic component, thereby reducing size.
2) DCM operation simplifies the dynamic stability compensation design with no right-half plane zero (RHP).
3) DCM flybacks have higher unity-gain bandwidth as compared to their CCM counterparts.

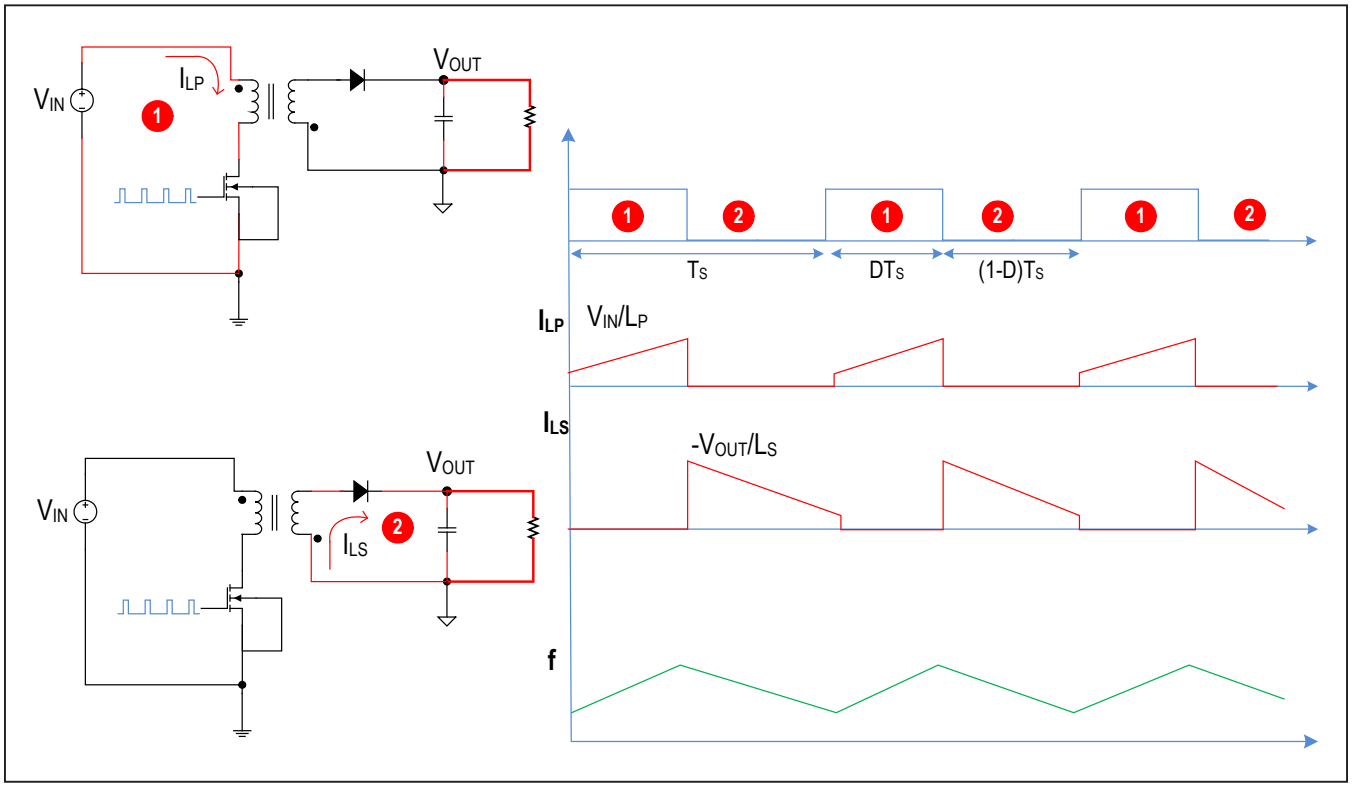

Figure 9: Continuous conduction mode operation of a flyback.

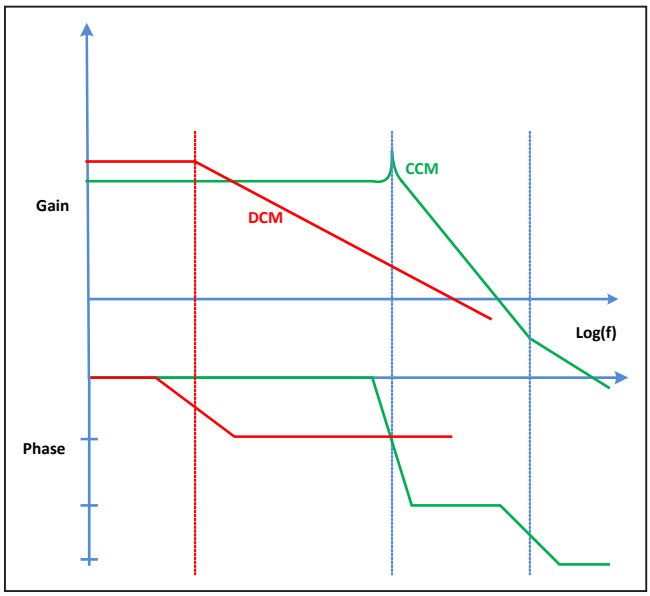

Figure 10: Dynamic stability compensation, DCM vs. CCM.

Table 2. DCM vs. CCM Flyback Comparison

VARIABLE	CCM	DCM
Peak MOSFET Voltage	Same (Assuming same k)	
Peak MOSFET Current	Lower	Higher
Peak Diode Voltage	Same (Assuming same k)	
Peak Diode Current	Lower	Higher
RMS Currents	Lower	Higher
Current Excursions	Lower	Higher
Operating Losses	Lower	Higher
Control Transfer Function	Complicated	Simple

A major disadvantage of discontinuous mode operation is the higher peak-to-average current ratio in the primary and secondary circuits as shown in Figure 11. Higher peak-to-average current means higher RMS current, and therefore, higher loss and lower efficiency. For high-power (> 50W) converters, the disadvantages of using discontinuous mode easily surpass the possible advantages.

In this design, we have chosen the CCM flyback topology with primary-side sensing and synchronous rectification for a more compact, efficient, and thermally cool power-supply design.

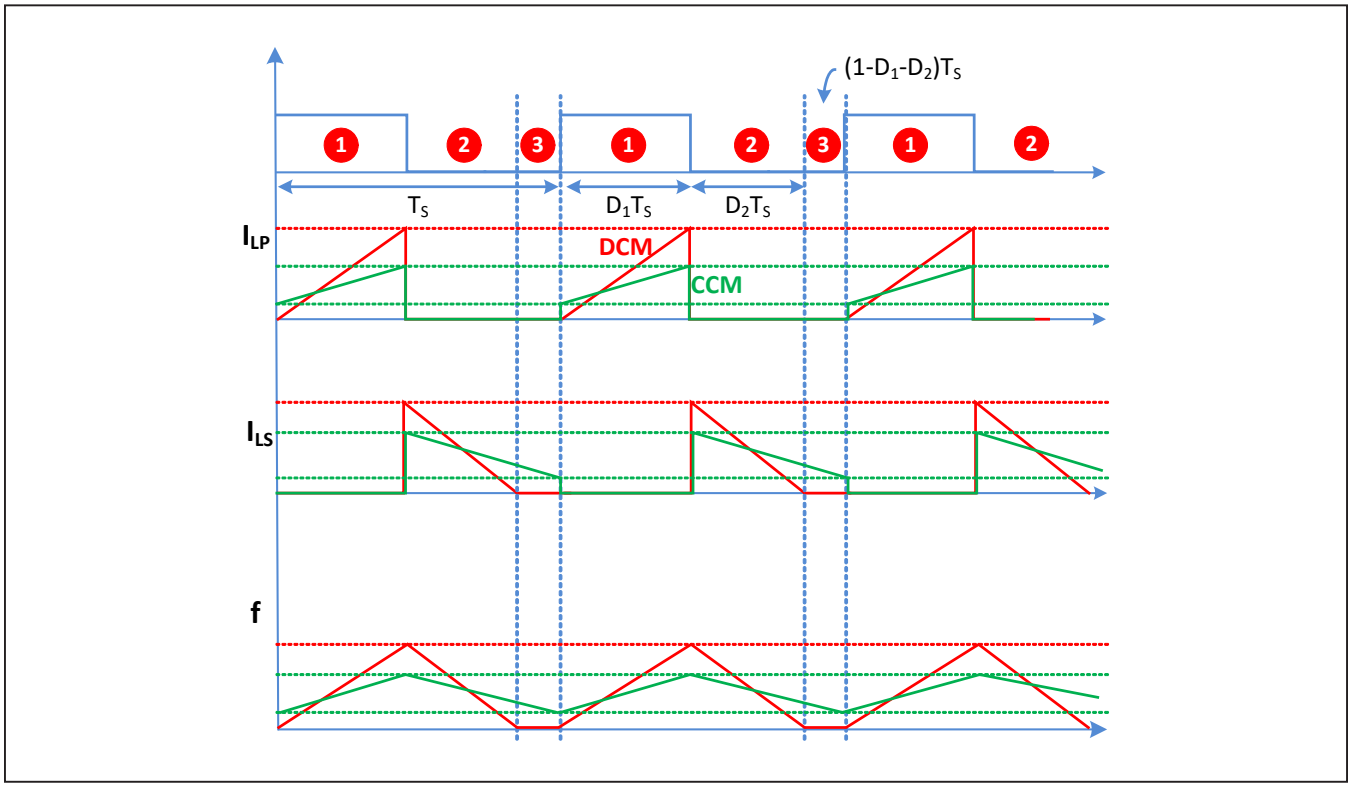

Figure 11: DCM vs. CCM peak windings currents comparison.

CCM Flyback Using the MAX5974A

The design's galvanically isolated 65W CCM flyback DC-DC converter uses the MAX5974A current-mode PWM controller. The MAX5995B provides a complete interface for the CCM flyback PD to comply with the IEEE 802.3af/at/bt standard in a PoE system. Minimal component count is achieved by using inductive feedback topology where the output voltage is regulated by using primary-side sensing. To maximize efficiency, synchronous rectification is achieved by replacing the secondary-side diode by a low-$R_{DS(ON)}$ MOSFET.

Inductive Feedback Flyback: Different from traditional direct output voltage feedback through optocoupler circuits, the MAX5974A uses an auxiliary winding to sense the voltage at the secondary output winding as shown in Figure 12. The power supply is regulated by sensing the induced auxiliary winding voltage, V_{AUX}. The auxiliary winding's circuit filters this induced voltage and regulates the output voltage (V_{OUT}) indirectly by regulating the scaled version of V_{AUX} which is fed to the FB pin of the converter using a resistor-divider network.

In practice, the voltage on the auxiliary winding consists of two parts. The first is the voltage spike generated by the transformer leakage inductance, while the second is the voltage plateau which is generated because of the reflected output voltage at the auxiliary winding. The sum of these two voltages is equal to the voltage on the filter capacitor. The inductive feedback circuit at the auxiliary winding is shown in Figure 13. It consists of a rectifier diode (D_1), an RC lowpass filter (R_F and C_F), and a resistor-divider network with resistors R_1 and R_2, respectively.

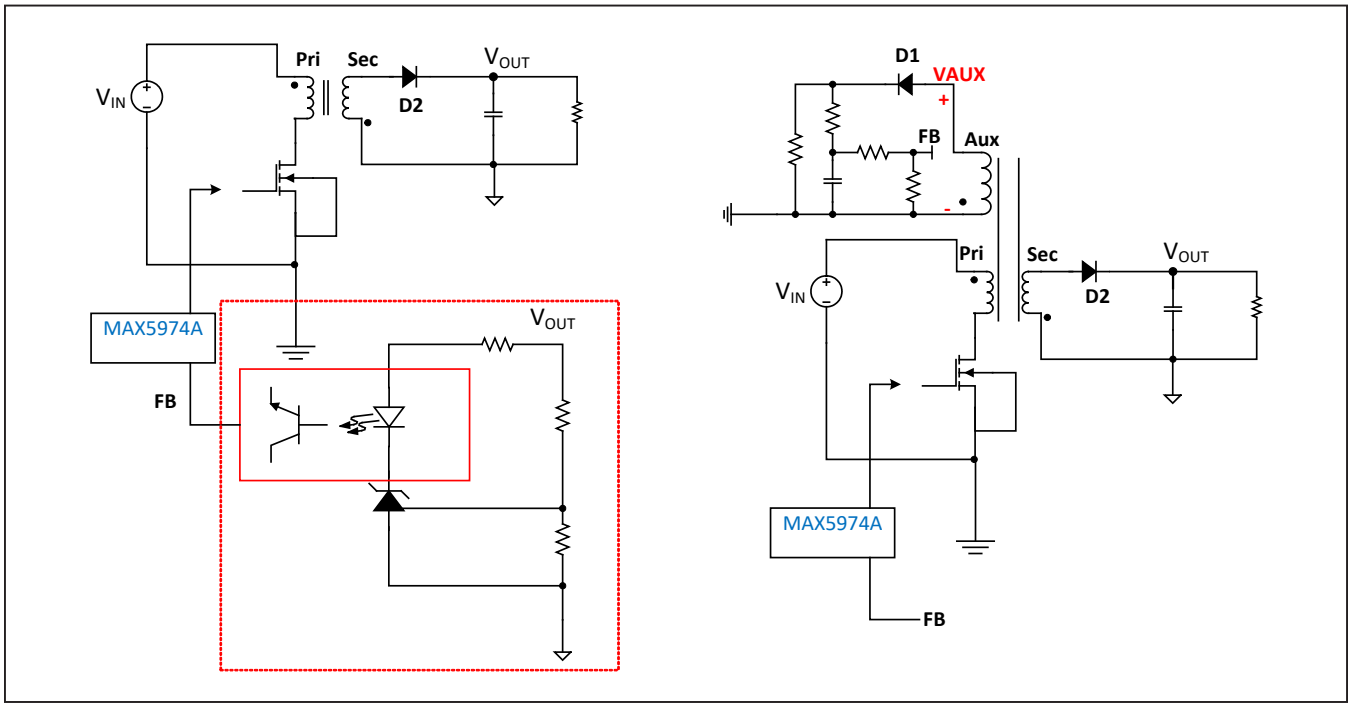

Figure 12: Inductive feedback flyback using the MAX5974A.

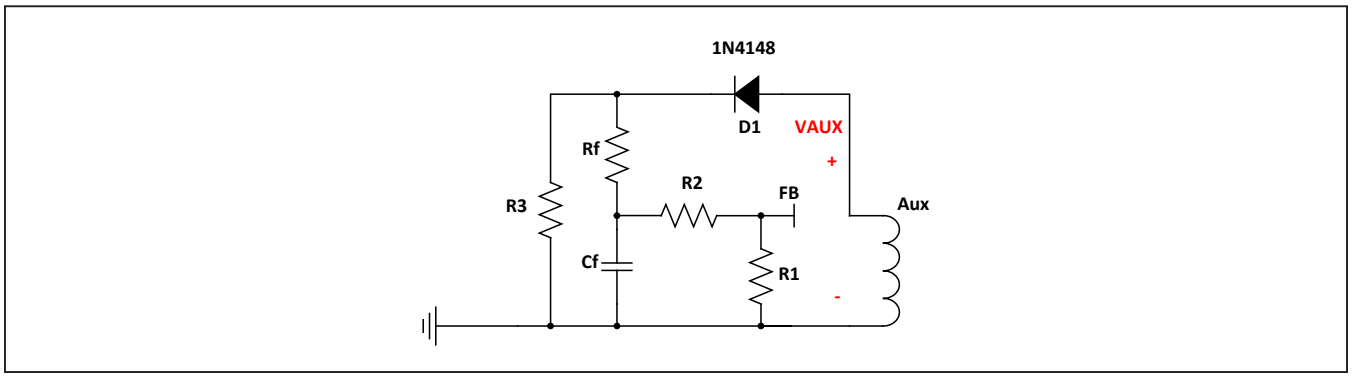

Figure 13: Inductive feedback circuit

The rectifier diode D1 is used here to avoid light-load output voltage overshoot. Under light-load conditions, the flyback converter may operate in DCM and the voltage plateau at AUX winding will not be a DC voltage but a resonant sinusoidal AC voltage. The small average value of this AC signal is fed back to the sample/hold circuit of the MAX5974A's FB pin. As a result, the MAX5974A controller will mistakenly increase the primary MOSFET duty cycle to push the output voltage high as the average voltage fed back is very small. This increase in output voltage can damage the secondary output diode and add a fast-recovery Schottky diode that can effectively prevent the large output voltage increase under light-load condition.

Inductive Feedback Regulation: The FB voltage is fed back into the MAX5974A's internal error amplifier. Therefore, it can regulate the output voltage by controlling the FB voltage at its reference value (typically 1.52V) in the closed control loop as shown in Figure 14. Since there is no direct feedback, the output voltage of an inductive feedback flyback is not as tightly regulated as a direct feedback flyback.

A tighter regulation means the output voltage drops less as the output current increases for a better load regulation. When the output current increases, the voltage spike on the auxiliary winding increases as well. This pushes the plateau voltage down, which reduces the output voltage. The factors that affect load regulation in inductively coupled flybacks are as follows:

1) The accuracy of feedback voltage reference, V_{REF}, will directly affect the output voltage. In the MAX5974A, it varies from 1.5V to 1.54V.
2) The tolerance of resistors R1 and R2 also affects the output voltage. Resistors with 1% tolerance are recommended. However, 0.1% tolerance can also be used for applications that require higher accuracy.
3) The tolerance of a transformer turns ratio and leakage inductance also plays an important role in soft voltage regulation. The higher the value of leakage inductance, the higher the voltage spike will be, which will lower the voltage plateau further and make the output voltage droop more.
4) The R_FC_F filter will affect the weight of the voltage spike. In general, the lower cutoff frequency of the filter leads to a smaller weight coefficient. A larger R_F will decrease the cutoff frequency, and thus make the droop curve more solid. Usually, the value of R_F is chosen from 5.1Ω to 50Ω.
5) The forward voltage drop of the output Schottky diode will affect the final output voltage. Synchronous rectification is recommended to control this problem.

The auxiliary winding is also used for charging the bootstrap UVLO capacitor of the MAX5974A, which further simplifies the circuit. The MAX5974A controlled inductive feedback flyback converter is very suitable for POE systems that require wide input range and high output voltage for its simplicity and low cost. Thus, the main advantages of an inductively coupled flyback using the MAX5974A is summarized as follows:

- MAX5974A with auxiliary winding ensures a compact design by minimizing the BOM cost of optocoupler and associated feedback circuitry.
- S/H capacitor samples the auxiliary winding voltage in average mode through a resistive divider which is used for output regulation.
- Higher efficiency can be achieved by using the AUXDRV pin to drive the secondary MOSFET in synchronous rectification configuration.

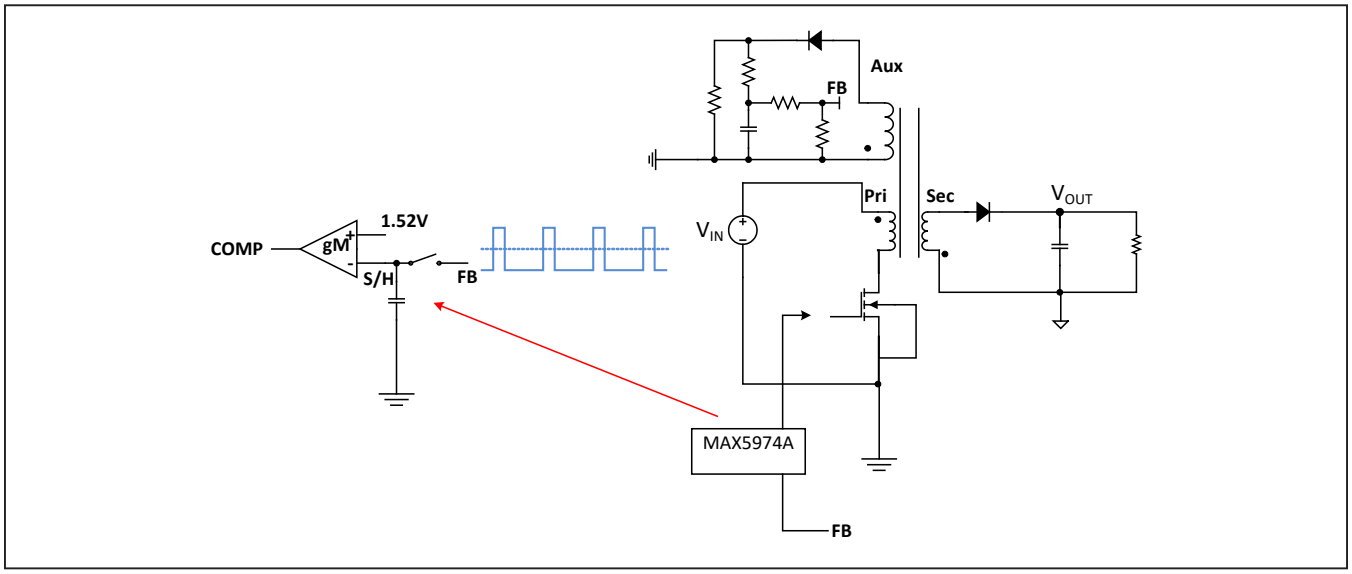

Figure 14: Inductive feedback regulation.

Synchronous Rectification in Flybacks: The synchronous flyback converters are more popular than conventional nonsynchronous designs. The use of a low voltage and low $R_{DS(ON)}$ MOSFET instead of the Schottky diode rectifiers at the secondary side offers several system advantages such as dramatic reduction in conduction losses, boost of system efficiency, and better thermal management. In synchronous flyback, the conventional secondary side diode is replaced by a secondary-side MOSFET as shown in Figure 15.

The implementation of synchronous rectification in the flyback topology ranges from conventional self-driven (secondary winding voltage detection) to a more complex control-driven solution. The selection of the driver circuitry for the secondary-side MOSFET is an important design parameter. The secondary MOSFET drive signal must be out of phase with the primary MOSFET drive signal to turn on only one MOSFET at a time and avoid cross conduction. This way, when the primary MOSFET is on, the secondary MOSFET will be off and vice versa.

Self-Driven Synchronous Rectification: In this technique, the transformer's secondary winding is used to directly drive the synchronous secondary-side MOSFET as shown in Figure 16. The self-driven technique is simpler, however, transformer leakage inductance and other parasitic inductance in the rectification loop are found to contribute to rectification loss. There may also be a delay in the turn-off signal of the synchronous MOSFET that can cause cross conduction which is detrimental to the overall performance of the design. There is always a possibility of overstressed gate-to-source voltage because of the turns ratio of the transformer. Self-driven implementation is more suited to lower output voltage designs.

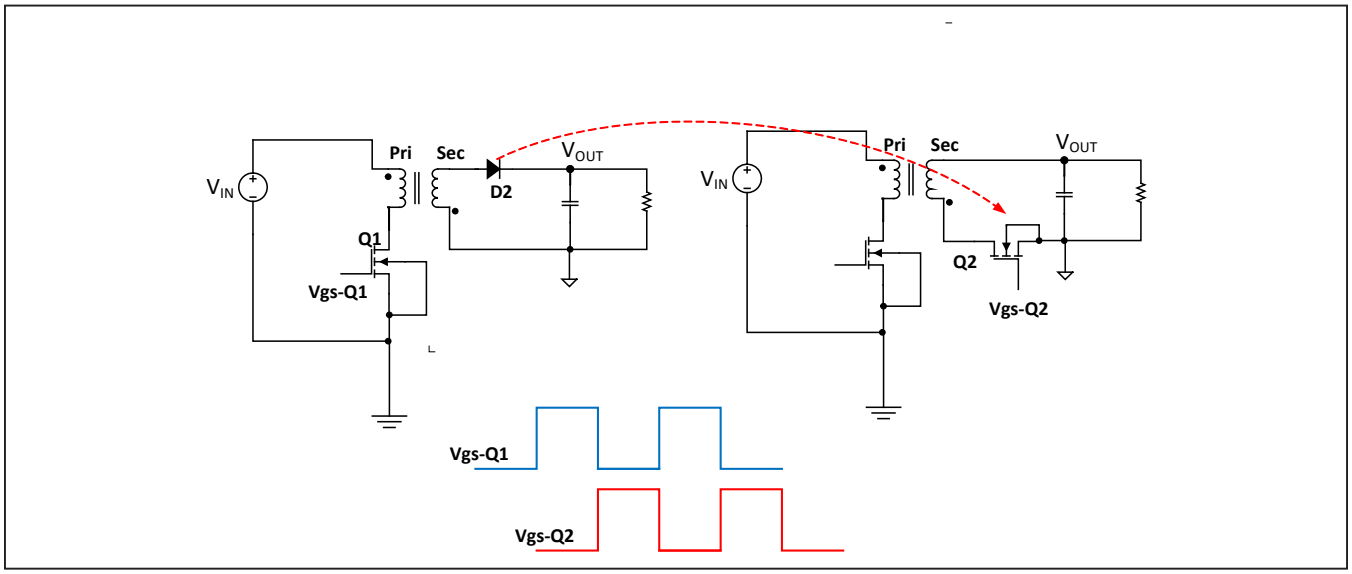

Figure 15: Nonsynchronous vs. synchronous implementation of flybacks.

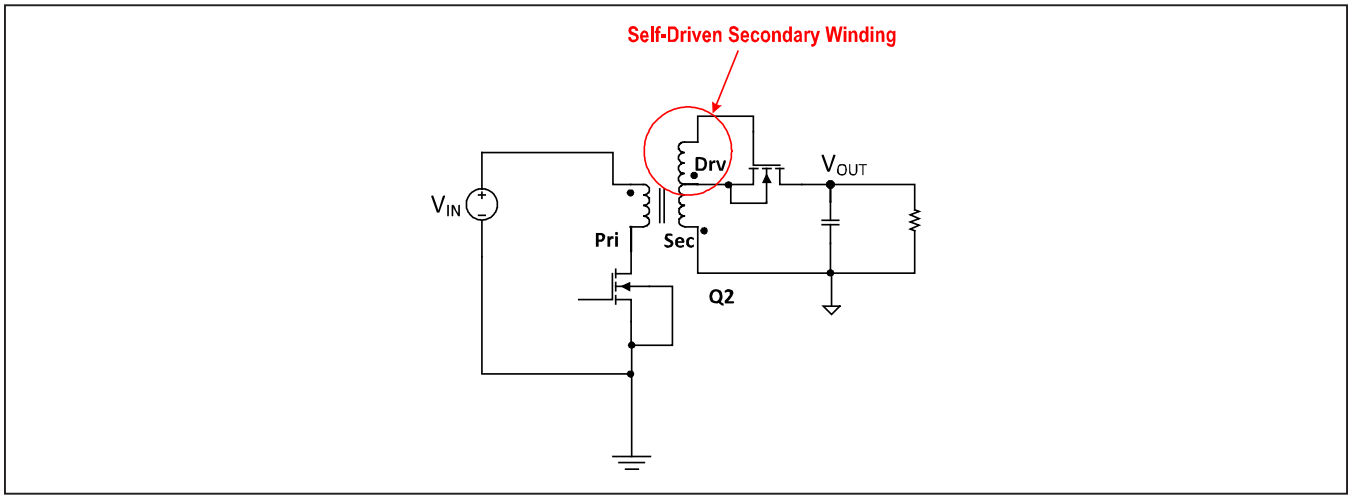

Figure 16: Self-driven synchronous rectification.

Control-Driven Synchronous Rectification: In this technique, a separate signal (AUXDRV pin in the MAX5974A) is used to drive the secondary synchronous MOSFET using a pulse transformer as shown in Figure 17. This is a very effective solution with wide input voltage range; however, it requires extra circuit elements that involve a pulse transformer, a few passive components for unipolar to bipolar signal transformation, and an extra current gain stage using a push-pull circuit. The pulse transformer should be selected so that its V-µs specification will be greater than or equal to the applied voltage-time stress. For example, if we are planning to drive a pulse transformer with a $10V_{P-P}$ bipolar signal and a duty cycle of 0.3 at the frequency of 250kHz; that transformer will need to have a V-µs specification of at least (5 x 0.3)/250k = 6Vµs.

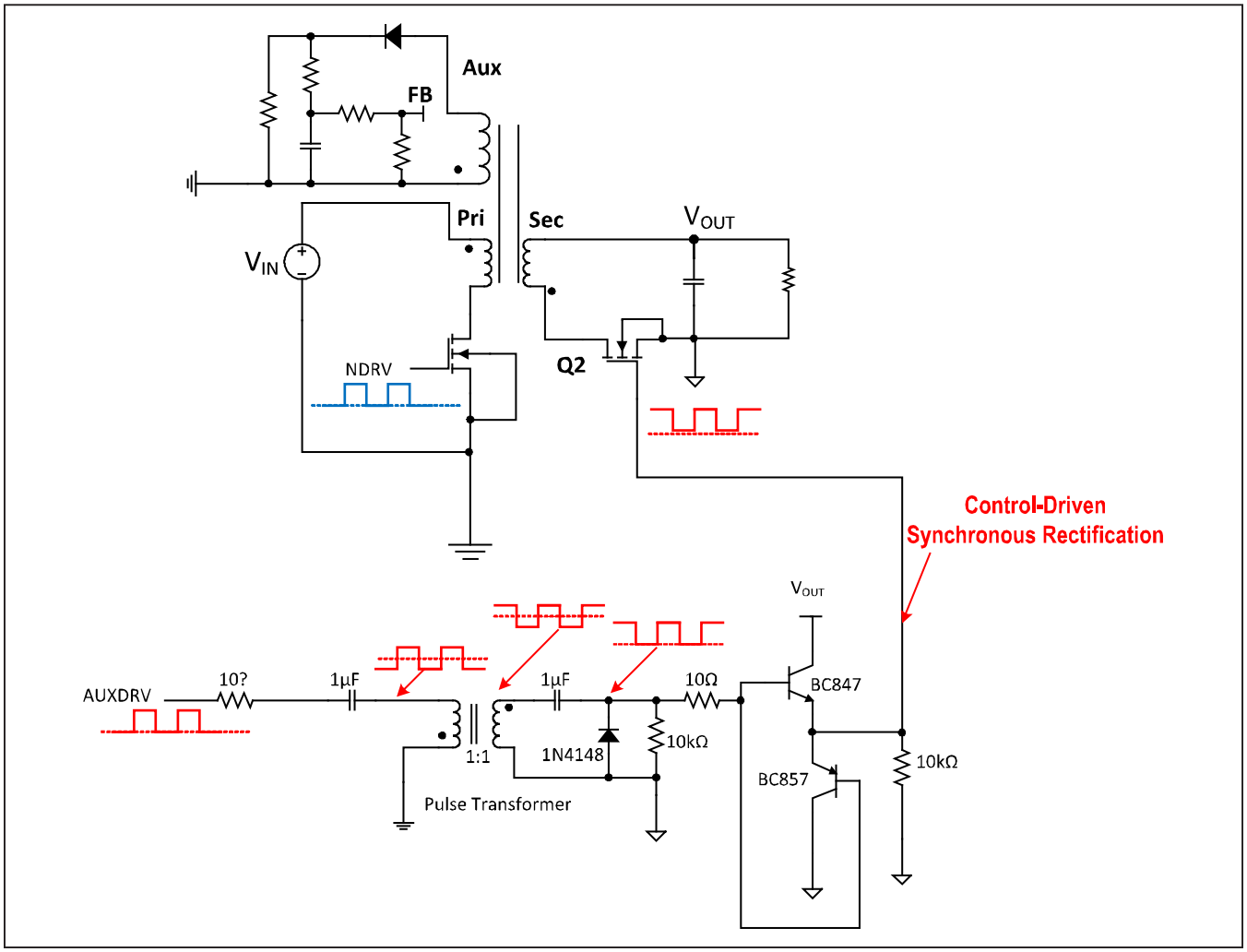

Figure 17: Control-driven synchronous rectification.

Design Procedure for CCM Flyback Using the MAX5974A

Step 1: Selection of the Switching Frequency

The selection of the switching frequency involves a trade-off between efficiency and component sizes. Low-frequency operation increases efficiency by reducing MOSFET-switching losses and gate-drive losses but requires a larger inductor and/or capacitor to maintain a low output ripple voltage. The MAX5974A's switching frequency is programmable between 100kHz and 600kHz with a resistor R_{RT} connected between the RT pin and GND. The following formula is used to determine the appropriate value of R_{RT} to generate the desired output-switching frequency (f_{SW}):

$$R_{RT} = \frac{8.7 \times 10^9}{f_{SW}} kHz$$

For this design, a switching frequency of 250kHz is selected. The required value of RRT is calculated as follows:

$$R_{RT} = \frac{8.7 \times 10^9}{250k} = 34.8k\Omega$$

A typical 1% resistor of 34.8kΩ is selected, R_{RT} = 34.8kΩ.

Step 2: Transformer Design

Turns Ratio, Duty Cycle, and Primary Inductance: The duty cycle is selected to be 40% maximum at the minimum input voltage of 57V and maximum load. Although operation beyond 40% is acceptable, it is not necessary in this design. The duty cycle will decrease only a few percent while in CCM operation because of the relatively low high-line input voltage of 57V. However, if the load is greatly reduced and the converter enters DCM operation, duty cycle will significantly decrease. The required turn ratio, k, of the transformer is calculated as follows:

$$k = \frac{N_s}{N_p} = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{D_{MAX} \times V_{IN(min)}}$$

V_{OUT} = 24V

V_D = 0.1V as synchronous rectification will be used

D_{MAX} = 0.4

$V_{IN(min)}$ = 37V

Substituting the above values in the expression of k as follows:

$$k = \frac{N_s}{N_p} = \frac{(24 + 0.1) \times (1 - 0.4)}{0.4 \times 37} = 0.977$$

For this design, a turns ratio of 1.1 is selected.

The expression for duty cycle is written as follows:

$$D = \frac{(V_{OUT} + V_D)}{V_{IN} \times k + (V_{OUT} + V_D)}$$

The nominal duty cycle for a nominal input voltage of 48V, and a maximum duty cycle with a maximum input of 57V is calculated as follows:

$$D_{NOM} = \frac{(24 + 0.1)}{48 \times 1.1 + (24 + 0.1)} = 0.3133$$

$$D_{MAX} = \frac{(24 + 0.1)}{57 \times 1.1 + (24 + 0.1)} = 0.3719$$

The primary inductance of the transformer is calculated as follows:

$$L_{PRI} = \frac{(V_{OUT} + V_D) \times (1 - D_{NOM})^2}{2 \times I_{OUT} \times \beta \times f_{SW} \times k^2}$$

The output current down to which the flyback converter should operate in CCM is determined by the selection of β. In this design as a start, we have selected β = 0.4 so that the converter operates in CCM down to 40% of the maxim output load current. The ripple in the primary current waveform is a function of the duty cycle; maximum ripple occurs at the maximum DC input voltage. Therefore, the maximum (worst-case) load current down to which the converter operates in CCM occurs at the maximum operating DC input voltage. The value of primary inductance is calculated as follows:

β = 0.4

f_{SW} = 250kHz

I_{OUT} = 2.7A

$$L_{PRI} = \frac{(24 + 0.1) \times (1 - 0.3133)^2}{2 \times 2.7 \times 0.43 \times 250k \times 1.1^2} = 16.17\mu H$$

For this design, we have selected a primary inductance of 15µH.

Peak and RMS Currents Calculation: Primary and secondary RMS and peak current calculations are needed to design the transformer in switched-mode power supplies. The peak primary current is also used in setting the current limit.

The primary current ripple, ΔI_{PRI}, is calculated as follows:

$$\Delta I_{PRI} = \frac{V_{IN(min)} \times D_{MAX}}{L_{PRI} \times f_{SW}}$$

$$\Delta I_{PRI} = \frac{37 \times 0.3719}{15\mu \times 250k} = 3.95A$$

The peak primary current, $I_{PRI(pk)}$, is calculated as follows:

$$I_{PRI(pk)} = \left[\frac{I_{OUT} \times k}{1 - D_{MAX}}\right] + \left[\frac{V_{IN(min)} \times D_{MAX}}{2 \times L_{PRI} \times f_{SW}}\right]$$

$$I_{PRI(pk)} = \left[\frac{2.7 \times 1.1}{1 - 0.3719}\right] + \left[\frac{37 \times 0.3719}{2 \times 15\mu \times 250k}\right] = 6.92A$$

The RMS primary current, $I_{PRI(rms)}$, is calculated as follows:

$$I_{PRI(rms)} = \sqrt{D_{MAX}} \times \sqrt{I_{PRI(pk)}^2 + \frac{\Delta I_{PRI}^2}{3} - \left(I_{PRI(pk)} \times \Delta I_{PRI}\right)}$$

$$I_{PRI(rms)} = \sqrt{0.3719} \times \sqrt{6.92^2 + \frac{3.95^2}{3} - (6.92 \times 3.95)} = 3.21A$$

The secondary current ripple, ΔI_{SEC}, is calculated as follows:

$$\Delta I_{SEC} = \frac{V_{IN(min)} \times D_{MAX}}{L_{PRI} \times f_{SW} \times k}$$

$$\Delta I_{SEC} = \frac{37 \times 0.3719}{15\mu \times 250k \times 1.1} = 3.59A$$

The peak secondary current, $I_{SEC(pk)}$, is calculated as follows:

$$I_{SEC(pk)} = \frac{I_{PRI(pk)}}{k}$$

$$I_{SEC(pk)} = \frac{6.92}{1.1} = 6.29A$$

The rms secondary current, $I_{SEC(rms)}$, is calculated as follows:

$$I_{SEC(rms)} = \sqrt{1 - D_{MAX}} \times \sqrt{I_{SEC(pk)}^2 + \frac{\Delta I_{SEC}^2}{3} - \left(I_{SEC(pk)} \times \Delta I_{SEC}\right)}$$

$$I_{SEC(rms)} = \sqrt{1 - 0.3719} \times \sqrt{6.29^2 + \frac{3.59^2}{3} - (6.29 \times 3.59)} = 3.58A$$

Auxiliary (Bias) Winding Turns Ratio: The required turns ratio, k_{AUX}, of the auxiliary winding of the transformer is calculated as follows:

$$\left[V_{AUX} + V_{D1}\right] = \frac{N_{AUX}}{N_{SEC}} \times \left[V_{OUT} + V_{D2}\right]$$

$$\left[V_{AUX} + V_{D1}\right] \times \frac{N_{SEC}}{N_{PRI}} = \frac{N_{AUX}}{N_{PRI}} \times \left[V_{OUT} + V_{D2}\right]$$

$$\left[V_{AUX} + V_{D1}\right] \times k = k_{AUX} \times \left[V_{OUT} + V_{D2}\right]$$

$$\left[V_{AUX} + V_{D1}\right] = \frac{k_{AUX}}{k} \times \left[V_{OUT} + V_{D2}\right]$$

For an auxiliary winding voltage of 12V, the required turns ratio k_{AUX} is calculated as follows:

$$\left[V_{AUX} + V_{D1}\right] = \frac{k_{AUX}}{k} \times \left[V_{OUT} + V_{D2}\right]$$

$$k_{AUX} = k \times \frac{\left[V_{AUX} + V_{D1}\right]}{\left[V_{OUT} + V_{D2}\right]}$$

$$k_{AUX} = 1.1 \times \frac{[12 + 0.7]}{[24 + 0.1]} = 0.579$$

For this design, we selected the bias winding turns ratio, k_{AUX} = 0.5. For a k_{AUX} = 0.5, the induced auxiliary voltage will be:

$$\left[V_{AUX} + 0.7\right] = \frac{0.5}{1.1} \times \left[24 + 0.1\right]$$

$$V_{AUX} = 10.254V$$

The leakage inductance of the transformer should be targeted as low as possible. For this design, we achieved a 1.5% leakage inductance of 0.225µH, L_{LKG} = 0.225µH. A customized transformer ZB1207-BE from Coilcraft is used. This transformer also fulfills the specification of turns ratio, auxiliary winding, and primary/secondary currents requirement of the design calculated step-by-step in this document.

Step 3: Startup Circuit Design

The device starts up when the voltage at IN exceeds 16V. During normal operation, the voltage at IN is normally derived from a bias/auxiliary winding of the transformer. However, at startup there is no energy delivered through the transformer; hence, a special bootstrap sequence is required. This circuit consists of an RC circuit involving R_{IN} and C_{IN} as shown in Figure 18. C_{IN} charges through the startup resistor, R_{IN}, to an intermediate voltage.

Only 100µA of the current supplied through R_{IN} is used by the IC, the remaining input current charges C_{IN} until V_{IN} reaches the bootstrap UVLO wake-up level. Once V_{IN} exceeds this level, NDRV begins switching the n-channel MOSFET and transfers energy to the secondary and auxiliary outputs. If the voltage on the auxiliary output builds higher than 7V (the bootstrap UVLO shutdown level), then startup has been accomplished and sustained operation commences. If V_{IN} drops below 7V before startup is complete, the device goes back to low-current UVLO.

Large values of C_{IN} increase the startup time, but also supply the gate charge for more cycles during initial startup. If the value of C_{IN} is too small, V_{IN} drops below 7V because NDRV does not have enough time to switch and build up sufficient voltage across the auxiliary winding, which powers the device. The device goes back into UVLO and does not start. To calculate the approximate amount of capacitance required, the following formula is used:

$$I_G = Q_{GTOT} \times f_{SW}$$

$$C_{IN} = \frac{[I_{IN} + I_G]}{V_{HYS}} \times t_{SS}$$

Q_{GTOT} = Total gate charge of primary-side and secondary-side (synchronous) MOSFET = 2 x 22nC = 44nC

I_{IN} = device internal supply current= 1.8mA

t_{SS} = soft-start time = 10ms

V_{HYS} = bootstrap UVLO hysteresis = 9V

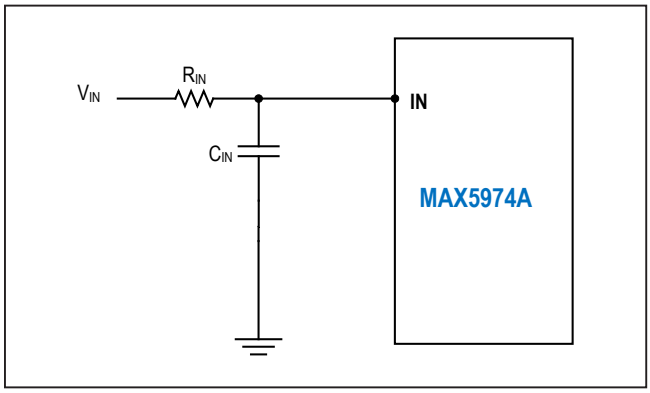

Figure 18: MAX5974A startup circuit.

Substituting the above values:

$$I_G = 44n \times 250k = 11mA$$

$$C_{IN} = \frac{[1.8m + 11m]}{9} \times 10m = 14.2\mu F$$

Two capacitors of 22µF each are selected as C_{IN}. C_{IN} = 2 x 22µF.

To calculate the approximate value of R_{IN}, use the following formula:

$$V_{IN} = \frac{V_{IN(min)} - V_{INUVR}}{I_{START}}$$

V_{INUVR} = bootstrap UVLO wakeup level = 16V.

I_{START} = device supply current at startup = 150µA.

Substituting the above values:

$$V_{IN} = \frac{37 - 16}{550\mu A} = 38.18k\Omega$$

A typical value of 39kΩ is selected as R_{IN}. R_{IN} = 39kΩ.

Step 4: Dead Time Selection

Dead time between the NDRV and AUXDRV output edges allow zero voltage switching (ZVS) to occur, minimizing conduction losses and improving efficiency. The dead time, t_{DT} is applied to both leading and trailing edges of the NDRV and AUXDRV outputs as shown in Figure 19.

Connect a resistor R_{DT} between DT and GND to set t_{DT} to any value between 40ns and 400ns by using the following expression:

$$R_{DT} = \frac{10k}{40n} \times t_{DT}$$

In this design, a deadtime of 68ns is selected. The required value of R_{DT} is calculated as follows:

$$R_{DT} = \frac{10k}{40n} \times 68n = 17k\Omega$$

A typical value of 16.9kΩ is selected as R_{DT}. R_{DT} = 16.9kΩ.

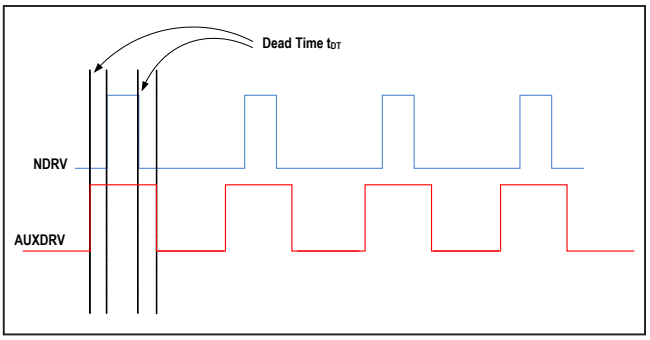

Figure 19: Dead time between AUXDRV and NDRV.

Step 5: Secondary-Side Synchronous MOSFET Selection

The key selection parameters to choose MOSFETs include:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Miller Plateau voltage
- Total gate charge (Q_{Gate})
- Output capacitance (C_{OSS})
- Power dissipation rating and package thermal resistance

Secondary-side MOSFET selection criteria include maximum drain voltage, peak/RMS currents into the secondary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits.

The maximum operating drain-source voltage rating of the synchronous MOSFET must be higher than the sum of the output voltage and the reflected input voltage. This voltage is calculated by the expression below:

$$V_{DS(sec)} = 1.25 \times (k \times V_{IN(max)} + V_{OUT})$$

$$V_{DS(sec)} = 1.25 \times (1.1 \times 57 + 24) = 108.375V$$

The current rating of the MOSFET should be selected to be at least twice the peak secondary winding's calculated current. For this design, we selected a 200V, 36A MOSFET BSC320N20NS3 G from Infineon Technologies as the secondary-side MOSFET.

Step 6: Primary-Side MOSFET Selection

Primary-side MOSFET selection criteria include maximum drain voltage, peak/RMS currents into the primary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET' s maximum V_{DS} rating must be higher than the worst-case drain voltage which is calculated as follows:

$$V_{DS(pri)} = V_{IN(max)} + \left(\frac{2.5 \times \left(V_{OUT} + V_{DS(sec)} \right)}{k} \right)$$

$$V_{DS(pri)} = 57 + \left(\frac{2.5 \times (24 + 0.1)}{1.1} \right) = 111.727V$$

The current rating of the MOSFET should be selected to be at least twice the peak primary winding's calculated current. For this design, we selected 200V, 34A MOSFET IPD320N20N3 G from Infineon Technologies as the primary-side MOSFET.

Step 7: Output Capacitor Selection

The output capacitor is usually sized to support a step load of a certain percentage of the rated output current so that the output voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated by using the following expressions:

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}} \right)$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, and f_C is the target closed-loop crossover frequency. In continuous conduction mode flyback designs, f_C is chosen to be less than at least 1/5 of the worst-case (lowest) right-half-plane (RHP) zero frequency f_{ZRHP}. The right-half-plane zero frequency is calculated as follows:

$$f_{ZRHP} = \frac{[1 - D_{MAX}]^2 \times V_{OUT}}{2 \times \pi \times D_{max} \times L_{PRI} \times I_{OUT} \times k^2}$$

$$f_{ZRHP} = \frac{[1 - 0.4]^2 \times 24}{2 \times \pi \times 0.4 \times 15\mu \times 2.7 \times 1.1} = 70.15kHz$$

In this design, we have selected f_C = 5kHz. The value of $t_{RESPONSE}$ is calculated as follows:

$$t_{RESPONSE} \cong \left(\frac{0.33}{5k} + \frac{1}{250k} \right) \cong 70\mu s$$

For a 50% load step, the value of I_{STEP} is calculated as follows:

I_{STEP} = 0.5 × I_{OUT} = 0.5 × 2.7 = 1.35A (50% of I_{OUT})

Similarly, a 3% voltage deviation value ΔV_{OUT} is calculated as follows:

ΔV_{OUT} = 0.03 × 24 = 720m V (3% of V_{OUT})

Finally, the required value of output capacitance is calculated as follows:

$$C_{OUT} = \frac{1.35 \times 70\mu}{720m} = 131.25\mu F$$

Due to the DC-bias characteristics, 2 x 47µF 50V MLCC capacitors along with 3 x 47µF 35V tantalum capacitors are selected for this design. MLCC capacitor values change with temperature and applied voltage. Refer to the capacitor data sheets to select capacitors that guarantee the required output capacitance across the operating range. For design calculations, use the worst-case derated value of capacitance, based on temperature range and applied voltage. In our case, the total worst-case derated

value of capacitors is 122.8µF. For CCM flyback converters, the output capacitor supplies the load current when the main switch is on, and therefore, the output voltage ripple is a function of load current and duty cycle. Use the following expression to estimate the output voltage ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times C_{OUT}}$$

$$\Delta V_{COUT} = \frac{2.7 \times 0.4}{250k \times 122.8\mu} = 35.18mV$$

Step 8: Soft-Start Capacitor Selection

When powering up MAX5974A, the IC will detect the voltage at the SS pin in 1024 clock cycles. The internal soft-start circuit will not work if the detected SS voltage is larger than 0.15V. A higher value of the soft-start capacitor is recommended to avoid the startup failure. A capacitor from SS to GND, C_{SS}, programs the soft-start time. Soft-start voltage V_{SS} controls the oscillator duty cycle during startup to provide a slow and smooth increase of the duty cycle to its steady-state value. In this design, the soft-start time is selected as t_{SS} = 20ms. The required value of C_{SS} is calculated follows:

$$C_{SS} = \frac{10\mu \times t_{SS}}{2V}$$

$$C_{SS} = \frac{10\mu \times 20m}{2V} = 100nF$$

A typical value of 100nF is selected as C_{SS}, C_{SS} = 100nF.

Step 9: Duty-Cycle Clamping

To set D_{MAX} using supply voltage feed-forward, connect a resistive divider that consists of R_{DCLMP1} and R_{DCLMP2} between the supply voltage, DCLMP, and GND as shown in Figure 20.

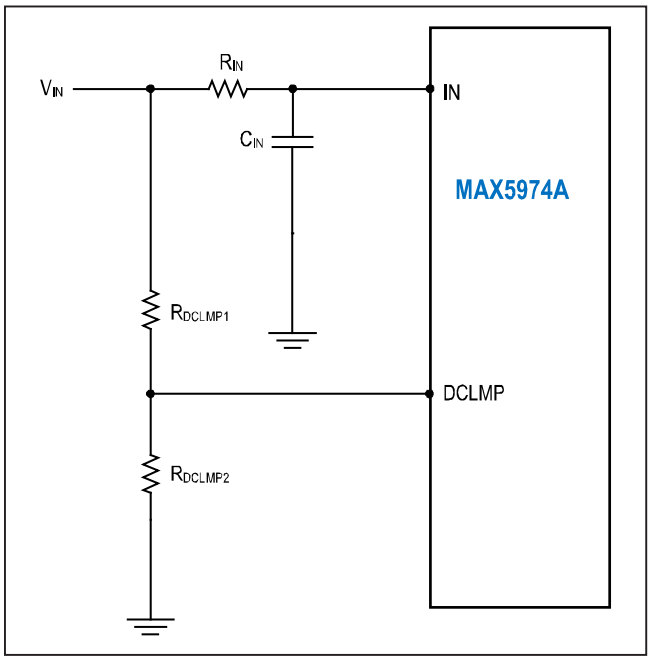

Figure 20: Setting of DMAX using supply voltage feed-forward.

This feed-forward duty-cycle clamp ensures that the external n-channel MOSFET is not stressed during supply transients. For a maximum duty-cycle clamp of 66%, the graph MAXIMUM DUTY CYCLE vs. V_{DCLMP} on page 8 of the datasheet shows a V_{DCLMP} voltage of approximately 0.8V. Selecting R_{DCLMP2} = 34kΩ, the value of R_{DCLMP1} is calculated as follows:

$$V_{DCLMP} = \frac{R_{DCLMP2}}{R_{DCLMP1} + R_{DCLMP2}} \times V_{IN(min)}$$

$$0.8 = \frac{34k}{R_{DCLMP1} + 34k} \times 37$$

$$R_{DCLMP1} = 1538.5k\Omega$$

A typical value of 1.5MΩ is selected as R_{DCLMP1}, R_{DCLMP1} = 1.5MΩ.

Step 11: EN Pin Connection

In this design, the EN pin of the MAX5974A is externally controlled by the power-good pin PG of MAX5995B. This PG is a high-voltage open-drain output. In this scenario, we must connect the IN and EN pins of MAX5974A through a resistor REN and then connect the EN pin to the PG pin of MAX5995B as shown in Figure 21 .

Select R_{EN} such that the voltage at IN, when EN is low, is less than 20V (i.e., the maximum gate voltage of the primary and secondary side MOSFET):

$$V_{IN(max)} \times \frac{R_{EN}}{R_{EN} + R_{IN}} < 20V$$

Selecting R_{EN} = 10kΩ will ensure that the above inequality holds as follows:

$$57 \times \frac{10k}{10k + 39k} < 20$$

$$11.6 < 20$$

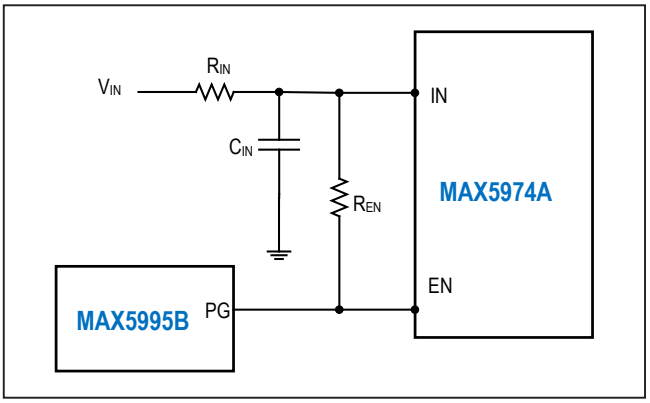

Figure 21: Logic control of the EN input.

A typical value of 10kΩ is selected as R_{EN}, R_{EN} =10kΩ.

Step 12: Output Voltage Setting

The MAX5974A includes an internal error amplifier with a sample-and-hold input. The noninverting input of the error amplifier is connected to the internal reference and feedback is provided at the inverting input as shown in Figure 22. Both high open-loop gain and unity-gain bandwidth allow good closed-loop bandwidth and transient response.

By selecting R_1 = 10kΩ, the value of R_2 is calculated by using the following expression:

$$R_2 = \left[\frac{V_{AUX}}{1.52} - 1\right] \times 10k$$

$$R_2 = \left[\frac{10.254}{1.52} - 1\right] \times 10k = 57.46k\Omega$$

A typical value of 57.6kΩ is selected as R_2, R_2 = 57.6kΩ.

Step 13: Current-Sense Resistor Selection

The current-sense resistor, R_{CS}, connected between the source of the primary-side MOSFET and PGND, sets the current limit. The current-limit comparator has a voltage trip level V_{CS} of 375mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS(peak)}}{I_{PRI(pk)}}$$

$$R_{CS} = \frac{0.375}{7} = 53m\Omega$$

A typical value of 36mΩ 1W is selected as R_{CS}, R_{CS} = 36mΩ.

Step 14: Programmable Slope Compensation

The devices use a current-mode control loop where the scaled output of the error amplifier (COMP) is compared to a slope-compensated current-sense signal at CSSC. The device generates a current ramp at the CSSC pin such that its peak is 50µA at 80% duty cycle of the oscillator. An external resistor R_{CSSC} connected from CSSC pin to the CS pin then converts this current ramp into programmable slope compensation amplitude, which is added to the current-sense signal for stability of the peak current-mode control loop. For a 25mV/µs ramp rate, the required value of the resistor R_{CSSC} is calculated as follows:

$$m = \frac{R_{CSSC} \times 50\mu A \times f_{SW}}{0.8}$$

$$25\frac{mV}{\mu s} = \frac{R_{CSSC} \times 50\mu A \times 250k}{0.8}$$

$$R_{CSSC} = 1.6k\Omega$$

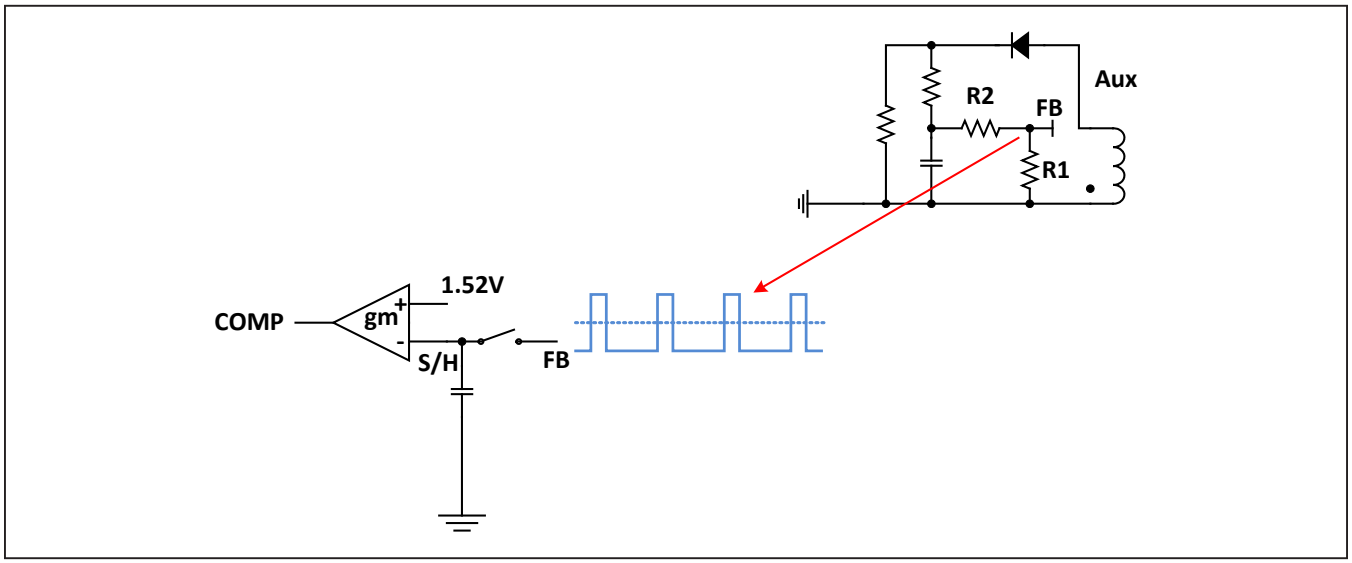

Figure 22: Setting output voltage.

A typical value of 1.5kΩ is selected as R_{CSSC}, R_{CSSC} = 1.5kΩ.

Step 15: Loop Compensation

A Type II loop compensation network of MAX5974A is shown in Figure 23.

In the CCM flyback converter, the primary inductance and the equivalent load resistance introduces a right-half-plane zero. The right-half-plane zero frequency is calculated as follows:

$$f_{ZRHP} = \frac{[1-D_{MAX}]^2 \times V_{OUT}}{2 \times \pi \times D_{max} \times L_{PRI} \times I_{OUT} \times k^2}$$

$$f_{ZRHP} = \frac{[1-0.4]^2 \times 24}{2 \times \pi \times 0.4 \times 15\mu \times 2.7 \times 1.1} = 70.15kHz$$

The pole frequency (f_P), the pole due to output capacitor, and the load are calculated as follows:

$$f_P = \frac{(1+D_{MAX}) \times I_{OUT}}{2 \times \pi \times C_{OUT} \times V_{OUT}}$$

$$f_P = \frac{(1+0.4) \times 2.7}{2 \times \pi \times 122.8\mu \times 24} = 0.204kHz$$

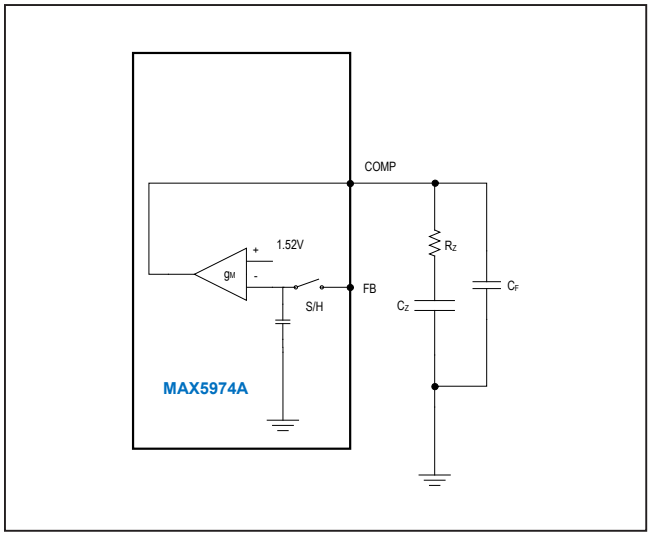

Figure 23: MAX5974A Type II compensation network.

Calculate the compensation resistor R_Z using the following expression:

$$R_Z = 924 \times \frac{1+D_{MAX}}{1-D_{MAX}} \times R_{CS} \times I_{OUT} \times k \times \sqrt{1+\left[\frac{f_{ZRHP}}{5k}\right]^2}$$

$$R_Z = 924 \times \frac{1+0.4}{1-0.4} \times 36m \times 2.7 \times 1.1 \times \sqrt{1+\left[\frac{70.1k}{5k}\right]^2} = 3.2k\Omega$$

Typical resistor value of 2.7kΩ is selected as R_Z, R_Z = 2.7kΩ.

With the control loop zero placed at twice the load pole frequency, the value of C_Z is calculated by using the following expression:

$$C_Z = \frac{1}{2 \times \pi \times 2 \times f_P \times R_Z}$$

$$C_Z = \frac{1}{2 \times \pi \times 2 \times 0.2k \times 2.7k} = 147nF$$

A typical capacitor of 100nF is selected as C_Z, C_Z = 100nF.

With the high-frequency pole placed at half the switching frequency, the value of C_P is calculated as follows:

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}}$$

$$C_P = \frac{1}{\pi \times 2.7k \times 250k} = 471pF$$

A typical capacitor of 100pF is selected as C_P, C_P = 100pF.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/22	Initial release	—