1.8V/10A Core Power Supply for CPUs, Microcontrollers, FPGAs, or DDR2 Interfaces Using the MAX20710

MAXREFDES1233

Introduction

The MAXREFDES1233 provides the internal core voltage (V_{CCINT}) for CPUs, microcontrollers, FPGAs, or DDR2 interfaces. This reference design targets CPUs, microcontrollers, FPGAs, or DDR2 interfaces that require 1.8V for V_{CCINT} from a 12V intermediary bus. The converter supports a maximum load of 10A at a 600kHz switching frequency. The MAXREFDES1233 is centered around the MAX20710 step-down regulator, which is configured for standalone operation. However, the PMBus™ interface allows for monitoring and control of various converter parameters. All circuitry for the PMBus interface is provided and the MAXPOWERTOOL002# can be used to communicate with the MAXREFDES1233.

The MAXREFDES1233 uses the MAX20710 synchronous step-down regulator. The internal FETs and control loop compensation allow for a compact design with minimal external resources. Additionally, the differential sense lines allow for accurate sensing of the CPU core voltage when located remotely from the MAX20710 IC. The loop gain is selectable to allow design flexibility between stability and output capacitance. A programmable soft-start limits inrush currents during startup. The MAX20710 also offers protections such as input UVLO, output overvoltage/undervoltage alerts, output overvoltage protection, over-temperature, and current limiting. Moreover, the PMBus interface allows additional parameters to be monitored such as input voltage, output voltage, output current, and temperature. For a full list of PMBus commands, see **Application Note 6042**.

Other features include the following:

- PMBus Interface
- Soft-Start
- Protections
  - Output under/over-voltage alert
  - Current limit and short-circuit protection
  - Input UVLO at 3.9V
  - Over-temperature protection

Hardware Specification

A synchronous buck converter design using the MAX20710 is demonstrated for a 1.8V/10A output. Table 1 provides an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX
Input Voltage	V_{IN}		11.4	12V	12.6V
Output Voltage	V_{OUT}			1.8V	
Load	I_{OUT}				10A
Frequency	f_{SW}			600kHz	
Peak Efficiency	η			85%	
Overshoot	V_{OS}	I_{STEP} = 5A			90mV
Undershoot	V_{US}	I_{STEP} = 5A			90mV
Output Ripple	V_{RIPPLE}				36mV

Designed–Built–Tested

The power supply has been built and tested. This document describes the design of the hardware shown in Figure 1.

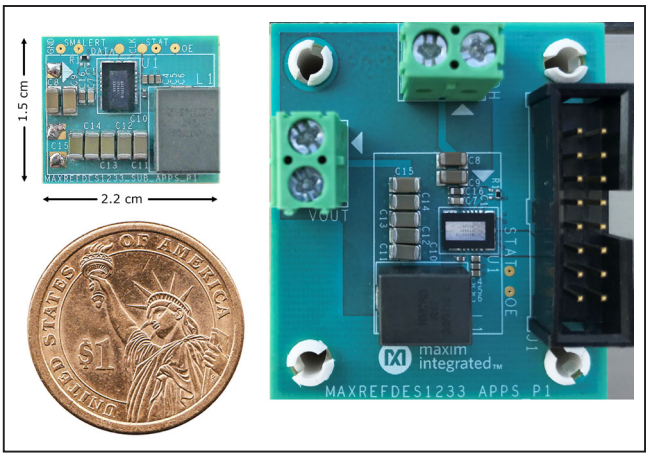

Figure 1. MAXREFDES1233 hardware.

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Synchronous Buck

In recent low-voltage, high-current power converters, the synchronous buck converters are more efficient than conventional buck converters because the synchronous buck converters use a low-side MOSFET, rather than a conventional catch diode. As a result, the power dissipated in the low-side MOSFET is minimized. The low-side MOSFET is always driven opposite to the high-side MOSFET. In other words, whenever one of these switches is on, the other is off. In steady-state conditions, the complementary switching of the high-side and low-side MOSFETs regulates the output to its set value.

Figure 2 illustrates the basic operation of a synchronous buck converter. The switching period begins with S1 turning on while S2 is off, which creates a conduction path from V_{IN} to the load. While S1 is on, the magnetic field within the inductor charges up. S1 is on for as long as the control algorithm dictates. When S1 has been on for the time commanded by the controller, S1 turns off in a break-before-make scheme that ensures S1 and S2 are never on at the same time. While both S1 and S2 are off, current flows through the body diode in the low-side switch. This is because the stored energy in the inductor must be discharged, and the low-side FETs body diode acts as a free-wheeling diode. The period where both S1 and S2 are off is known as dead time. After the dead time, S2 is turned on, and the inductor discharges through the on-resistance of S2 for the remainder of the switching period. Discharging the inductor through the low on-resistance of the low-side FET significantly reduces conduction losses when compared to a conventional buck converter that uses a diode in place of the low-side FET. The control algorithm uses these three states to regulate the output based on feedback signals from the converter.

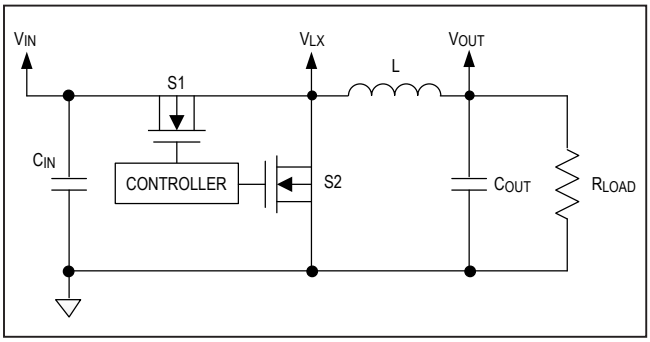

Figure 2. Synchronous buck converter topology.

PWM Valley Current-Mode Control

The MAX20710 is a synchronous buck regulator that uses a pulse-width-modulation (PWM), valley current-mode control scheme. PWM control allows for regulation of the output voltage by modulating the high-side switch on-time (i.e., S1 in Figure 2), while maintaining a constant switching frequency. The control algorithm uses the output voltage as feedback to determine the high-side switch on-time. Typical waveforms for the output voltage (V_{OUT}), inductor current (I_L), and switch-node (V_X) are shown in Figure 3.

Moreover, the MAX20710 also monitors the inductor current through the low-side switch. While the low-side switch is on, the V_X node is connected to ground, and the inductor is in a discharging state. The inductor reaches its minimum current at the end of the low-side switch on-time, which is known as the valley of the inductor current. The valley current-mode control limits the valley current of the inductor based on the device's OCP setting and limits the amount of energy that is delivered to the load, which provides an inherent form of output current limiting. For more details on valley current protection, see **Application Note 6498**.

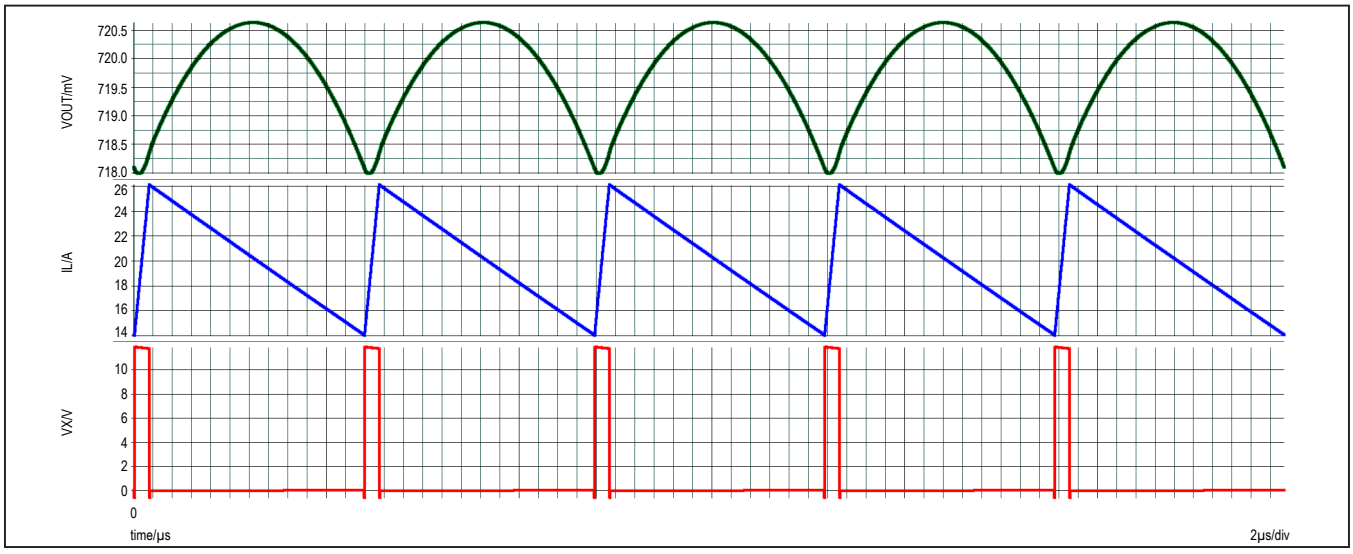

Figure 3. Synchronous buck waveforms showing output voltage (V_{OUT}), inductor current (I_L), and the switch-node (V_X).

Design Procedure for the MAXREFDES1233

The design procedure provides a step-by-step process for power supply designers to select components. The component designators reference to the MAXREFDES1233 schematic. All other terms and variables are from the *MAX20710 data sheet*. The MAX20710 uses V_{DDH} and V_{IN} interchangeably to reference the input voltage. This document uses V_{IN} to describe the input voltage, and the reader should acknowledge that $V_{IN} = V_{DDH}$, per the *MAX20710 data sheet*.

Step 1: Boot Voltage, Soft-Start, and PMBus Slave Address

The boot voltage, soft-start, and PMBus slave address are programmed through the PGMA pin.

The boot voltage is programmed using a capacitor from PGMA to GND, as shown in the PGMA Pin C_SELA Capacitor Values table in the *MAX20710 data sheet*. The output voltage cannot be less than the boot voltage, so we must select the boot voltage to be less than the desired output voltage (i.e., V_{OUT} = 1.8V). The capacitor on PGMA is left open to provide a 0.6484V boot voltage.

C1 = Open

The soft-start time and PMBus slave address are programmed through a resistor from PGMA to GND. It is expected that the MAXREFDES1233 requires a high output capacitance due to the low switching frequency and required low output voltage ripple. During startup, the output capacitors are discharged and appear as a short to the input. Large inrush currents are drawn from the supply during startup due to the bulk output capacitance. To minimize current draw during startup, we select the longest startup time of 3ms. The PMBus slave address is not a concern for this design, so a 1.78kΩ resistor (R1) is used to set the 3ms soft-start and to provide a slave address of 0x50. See the PGMA Pin R_SELA Values table in the *MAX20710 data sheet* for more information.

R1 = 1.78kΩ ±1%

Step 2: Output Voltage

The output voltage is programmed using a resistor divider from V_{OUT} to PGND. The MAX20710 uses differential sense lines to measure the feedback voltage. The differential sense lines accurately measure the output voltage at the point of load to minimize the effect of PCB parasitic impedances on the feedback signal. The MAXREFDES1233 uses external feedback resistors to set the output voltage, so the differential sense lines must be connected to the low-side resistor in the resistor divider network. However, the differential sense lines must still be routed to the point of load. Use the layout for this design as reference when designing the PCB layout.

The voltage across the low-side resistor is regulated to V_{BOOT} upon startup but can be adjusted using the internal DAC. Per the MAX20710 data sheet recommendations, where $V_{REF} = V_{Boot}$ = 0.6484V upon startup, and R_{PAR} is approximately 1kΩ, calculate the feedback resistor divider values as follows:

$$R_4 = \frac{V_{OUT} \times R_{PAR}}{V_{REF}} = \frac{1.8V \times 1k\Omega}{0.6484V} \approx 2.77k\Omega$$

$$R_5 = \frac{R_1 \times R_{PAR}}{R_1 - R_{PAR}} = \frac{2.77k\Omega \times 1k\Omega}{2.77k\Omega - 1k\Omega} \approx 1.56k\Omega$$

The feedback resistors must be at least 1% tolerance, so resistors are chosen based on available values from the standard E96 series of resistors. For this design, we select R4 = 3.09kΩ and R5 = 1.74kΩ because this combination of standard E96 resistors yields the lowest error in output voltage.

Step 3: Switching Frequency

The switching frequency is hardware selectable or overridden through the PMBus. This design does not require any PMBus programming, so the switching frequency is set by placing a resistor from PGMB to GND. The switching frequency is chosen for high-efficiency, so we select the lowest possible switching frequency of 600kHz. We must also ensure the minimum on-time is not violated based on the required duty cycle and set switching frequency. The absolute minimum on-time of the MAX20710 converter is 50ns. A 600kHz switching frequency with 12V input and 1.8V output results in 250ns of on-time, as shown by the following equation:

$$t_{H\_ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} = \frac{1.8V}{12V \times 600kHz} = 250ns$$

The operating on-time is much greater than the 50ns minimum, so there is no concern for a minimum on-time violation. The 600kHz switching frequency is set by leaving the capacitor open on the PGMB pin. See the *MAX20710 data sheet* for the PGMB Pin C_SELB Capacitor Values table.

C3 = 220pF

Step 4: Average Input Current

The average input current of the converter must be less than 6A. The following equation is used to calculate the average input current and ensure it does not violate the 6A limit.

$$I_{VIN(MAX)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} = \frac{1.8V \times 10A}{12V \times 0.85} = 1.76A$$

For a 600kHz switching frequency, see the MAX20710 data sheet for the typical system efficiency. For V_{IN} = 12V, V_{OUT} = 1.8V, and 10A max output current, the efficiency is around 85%. This gives a ball park figure for the maximum average input current and ensures we are less than the 6A limit.

Step 5: Inductor and Valley OCP Limit

The inductor is chosen based on the inductor current ripple. The ratio between the peak-to-peak and the average inductor current is known as the inductor current ratio (i.e., LIR). The recommend LIR is between 25% to 50% of the full rated load for the MAX20710 (i.e., $I_{OUT(MAX)}$ = 10A). A higher LIR results in less output capacitance and greater efficiency but also a slow transient response and a physically larger inductor. In contrast, a lower LIR has better transient performance and a smaller inductor but requires greater output capacitance to maintain a low ripple and generally results in lower efficiency. To obtain a balanced performance, the LIR is selected to be 50% of the full rated load.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times LIR \times I_{OUT(MAX)} \times f_{SW}}$$
$$= \frac{1.8V \times (12V - 1.8V)}{12V \times 0.5 \times 10A \times 600kHz} \approx 510nH$$

The peak current flowing through the inductor must also be calculated to ensure the inductor core does not saturate. To determine the peak inductor current, we first need to determine the valley OCP limit setting. The valley OCP limit is chosen based on the inductor current ripple and the desired output current limit. Calculate the ripple current based on the high-side switch on-time (t_{H_ON}) as follows:

$$I_{OUTRIPPLE} = \frac{t_{H\_ON} \times (V_{IN} - V_{OUT})}{L_1}$$
$$= \frac{250ns \times (12V - 1.8V)}{510nH} = 5A$$
$$I_{VALLEY} = I_{OUT} - \frac{I_{OUTRIPPLE}}{2}$$
$$= 10A - \frac{5A}{2} = 7.5A$$

We must select a valley OCP limit above the minimum calculated (7.5A) to ensure that the OCP limit does not trip at full load. Choose the OCP setting 0, which provides a typical valley threshold of 11.6A. Moreover, use a 3.6mΩ transimpedance gain, which allows a compromise between required output capacitance and loop stability. For more information on RGAIN selection, see the Control-Loop Stability section in the *MAX20710 data sheet*.

Using the known positive valley current limit (i.e., I_{OCP}) and inductor current ripple, calculate the absolute peak inductor current. The valley OCP limit has some tolerance, so the maximum positive valley current for the OCP setting 0 is used in the calculation.

$I_{PEAK} = I_{VALLEY(MAX)} + I_{OUTRIPPLE} = 14.1A + 5A \approx 19.1A$

The chosen inductor is found in the Recommended Inductors table in the *MAX20710 data sheet*. The FP1007 family of inductors from Eaton/Cooper provide a small size for the required inductance. The FP1007R6-R47-R is chosen for the 470nH inductance and 23.5A saturation current, which is well above the expected peak current. Additionally, FP1007R6-R47-R provides the lowest DCR and height from the list of recommended inductors shown in Table 9 of the *MAX20710 data sheet*. This ultimately results in a higher efficiency by using a smaller inductor.

Step 6: Output Capacitance

The output capacitors are chosen based on the desired peak-to-peak voltage ripple on the output. The peak-to-peak ripple is chosen to be 2% of the output voltage for a peak-to-peak ripple of 36mV. The output capacitors cumulative capacitance, ESR, and ESL contribute to the output voltage ripple. To simplify the design, the ESL component is assumed to be minimal since the switching frequency is relatively low. The output capacitance and ESR are each assumed to contribute to 50% to the ripple voltage. These voltage ripples are out of phase but combining them provides a conservative estimate of the output voltage ripple. For the selected inductance, the inductor current ripple is re-calculated to determine the output capacitance.

$$I_{OUTRIPPLE} = \frac{t_{H\_ON} \times (V_{IN} - V_{OUT})}{L_1}$$
$$= \frac{250ns \times (12V - 1.8V)}{470nH} \approx 5.42A$$
$$ESR = 50\% \times \frac{V_{PP}}{I_{OUTRIPPLE}} = 50\% \times \frac{36mV}{5.42A} = 0.33m\Omega$$
$$C_{OUT(MIN)} = \frac{I_{OUTRIPPLE}}{8 \times f_{SW} \times 50\% \times V_{PP}}$$
$$= \frac{5.42A}{8 \times 600kHz \times 50\% \times 36mV} \approx 63\mu F$$

Another aspect of output capacitor selection is the overshoot and undershoot that occurs during a transient loading event. If the slew rate of the load current greatly exceeds the slew rate of the inductor, the output capacitors must deliver charge during a loading event or absorb charge during an unloading event. This causes the output voltage to momentarily sag during loading or soar during an unloading event. The design must ensure there is no more than 5% over/undershoot for a quick transient load that exceeds the slew rate of the inductor based on a 5A step load.

Determine the minimum capacitance for both loading and unloading events by using the following equations:

Output Voltage Sag:

$$C_{OUT(MIN)} = \frac{L_1 \times \left(I_{STEP} + \frac{I_{OUTRIPPLE}}{2}\right)^2}{2 \times V_{SAG} \times (V_{IN} - V_{OUT})}$$

$$= \frac{470nH\left(5A + \frac{5.42A}{2}\right)^2}{2 \times 90mV \times (12V - 1.8V)} \approx 15\mu F$$

Output Voltage Soar:

$$C_{OUT(MIN)} = \frac{L_1 \times \left(I_{STEP} + \frac{I_{OUTRIPPLE}}{2}\right)^2}{2 \times V_{SAG} \times V_{OUT}} + \frac{I_{STEP} \times t_{H\_ON}}{V_{SOAR}}$$

$$= \frac{470nH \times \left(5A + \frac{5.42A}{2}\right)^2}{2 \times 90mV \times 1.8V} + \frac{5A \times 250ns}{90mV} = 100\mu F$$

Lastly, we must consider the effects of the control loop response time. The control loop takes time to respond to changes in the output voltage. This response time results in some error in the output voltage during loading and unloading events. The magnitude of the error voltage is dependent on both the magnitude of the step load and the loop gain. The effective loop gain is calculated below based on the RGAIN setting and feedback divider ratio.

$$K_{DIV} = \frac{R_5}{R_5 + R_4} = \frac{1.74k\Omega}{1.74k\Omega + 3.09k\Omega} = 0.36$$

$$R_{GAIN\_EFF} = \frac{R_{GAIN}}{K_{DIV}} = \frac{3.6m\Omega}{0.36} = 10m\Omega$$

Using the effective loop gain, we then calculate the error produced based on a 5A step from 50% to 100% load. The error produced is 50mV, which is below the 5% over/undershoot specification.

$V_{OUT\_ERROR} = I_{STEP} \times R_{GAIN\_EFF} = 5A \times 10m\Omega = 50mV$

With a cumulative capacitance greater than 100µF and a total ESR less than 0.33mΩ, the desired output voltage ripple and over/undershoot can be achieved. To achieve the 100µF output capacitance and low ESR, multiple capacitors are placed in parallel. Five 100µF/4V ceramic capacitors are used for the bulk capacitance. The combined capacitance is 500µF.

Step 7: Input Capacitance

The input capacitor is chosen based on the desired input voltage ripple. The input voltage ripple is typically between 2% to 3% of the input voltage. However, this design has a 2% ripple for a total output voltage ripple of 240mV. Calculate the input capacitance as shown in the following equation.

$$C_{IN} = \frac{I_{MAX} \times V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times V_{IN}^2 \times V_{IN\_PP}}$$

$$= \frac{10A \times 1.8V \times (12V - 1.8V)}{600kHz \times 12V^2 \times 0.24V} \approx 8.8\mu F$$

The input capacitors provide current to the buck converter during switching transitions. Calculate the expected RMS current through the input capacitors to determine the RMS current rating the capacitors need to support by using the following equation:

$$I_{CIN\_RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{DDH} - V_{OUT})}}{V_{DDH}}$$

$$= \frac{10A \times \sqrt{1.8V \times (12V - 1.8V)}}{12V} \approx 3.57A$$

To achieve the required input capacitance and RMS current rating, multiple ceramic capacitors are placed in parallel. The selected bulk capacitor is the Murata® GCG31CR71E475JA01. The nominal capacitance for this capacitor is 4.7µF. Based on the capacitance calculation, a total of two capacitors are used in parallel.

In addition, one 1µF and one 0.1µF capacitors are placed in parallel with the bulk capacitance to support any high frequency currents. These capacitors are placed closest to the IC pins to minimize the parasitic impedance between the capacitors and IC.

Step 8: BST Capacitor

The BST capacitor supplies charge to the high-side FET gate during switching. The high-side switch is internal, so the gate driver requirements are fixed. Use the 0.22µF ceramic capacitor recommended by the data sheet. The maximum voltage across the BST capacitor is the same as the input voltage, so a 16V rated capacitor is chosen based on the 12V input requirement.

Murata is a registered trademark of Murata Manufacturing Co.

Step 9: V_{CC}, STAT, and OE

Capacitors are required at the V_{CC} pin to stabilize the internal LDO. These capacitors are placed as close as possible to the device. Three 10µF X5R ceramic capacitors are recommended for the V_{CC} pin.

The STAT pin is an open-drain alert that requires a pullup resistor to the V_{CC} rail. The recommended value for the pullup resistor is 20kΩ.

The OE pin enables the output when raised above the rising threshold voltage. The rising threshold voltage is precise to allow the sequencing of multiple regulators. However, this pin is pulled to V_{CC} through a 20kΩ resistor to allow the output voltage to start up when the input voltage is applied.

Step 10: SDA, SCL, and SMALERT

The SDA, SCL, and SMALERT are open-drain pins that require pullup resistors for PMBus communication. The PMBus interface is designed to be compatible with Maxim's MAXPOWERTOOL002#, which uses 3.3V logic.

Description of MAXPOWERTOOL002# GUI

The MAXREFDES1233 provides hardware connections to the PMBUS interface of the MAX20710 using the standard MAXPOWERTOOL002# connectors. The MAXPOWERTOOL002# GUI is used to monitor and control the MAX20710 buck converter. Figure 4 shows the MAXPOWERTOOL002# GUI when connected to the MAXREFES1233. For more information on using the MAXPOWERTOOL002# GUI, see the **MAXPOWERTOOL002# Quick Start Guide**. For a full list of allowed PMBus commands, see **Application Note 6042**.

The MAX20710 device only reports the differential voltage measured across the V_{SENSE+} and V_{SENSE-} pins. When feedback resistors are used to program the output voltage, the voltage measured on these pins is a scaled down version of the output. To obtain the correct output voltage reading, the resistor divider scaling factor must be set in the "PMBus Command" tab of the GUI. Figure 5 demonstrates where the resistor divider ratio is set. The scaling factor is the same as the previously calculated K_{DIV} value.

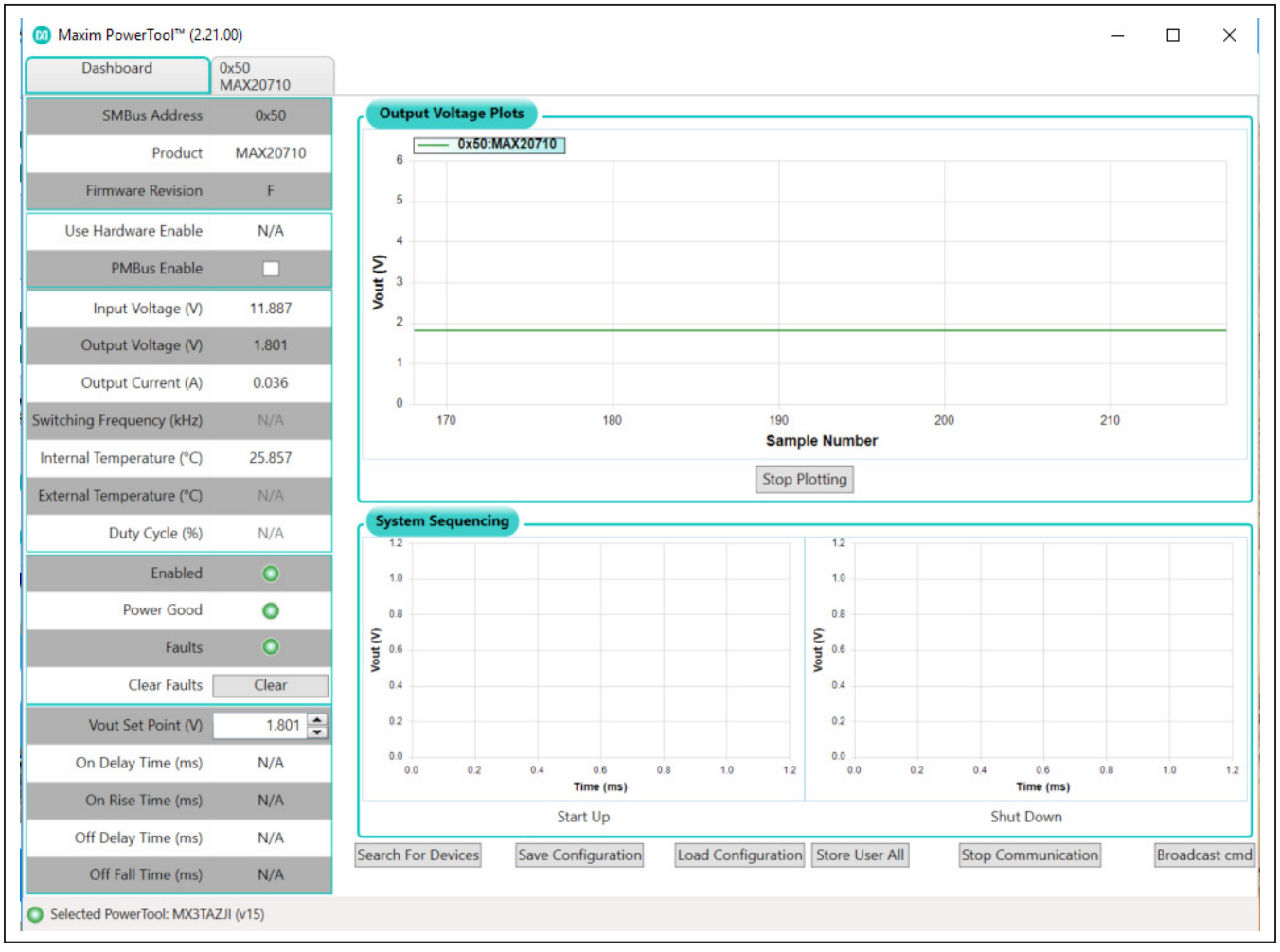

Figure 4. MAXPOWERTOOL002# GUI connected to the MAXREFDES1233.

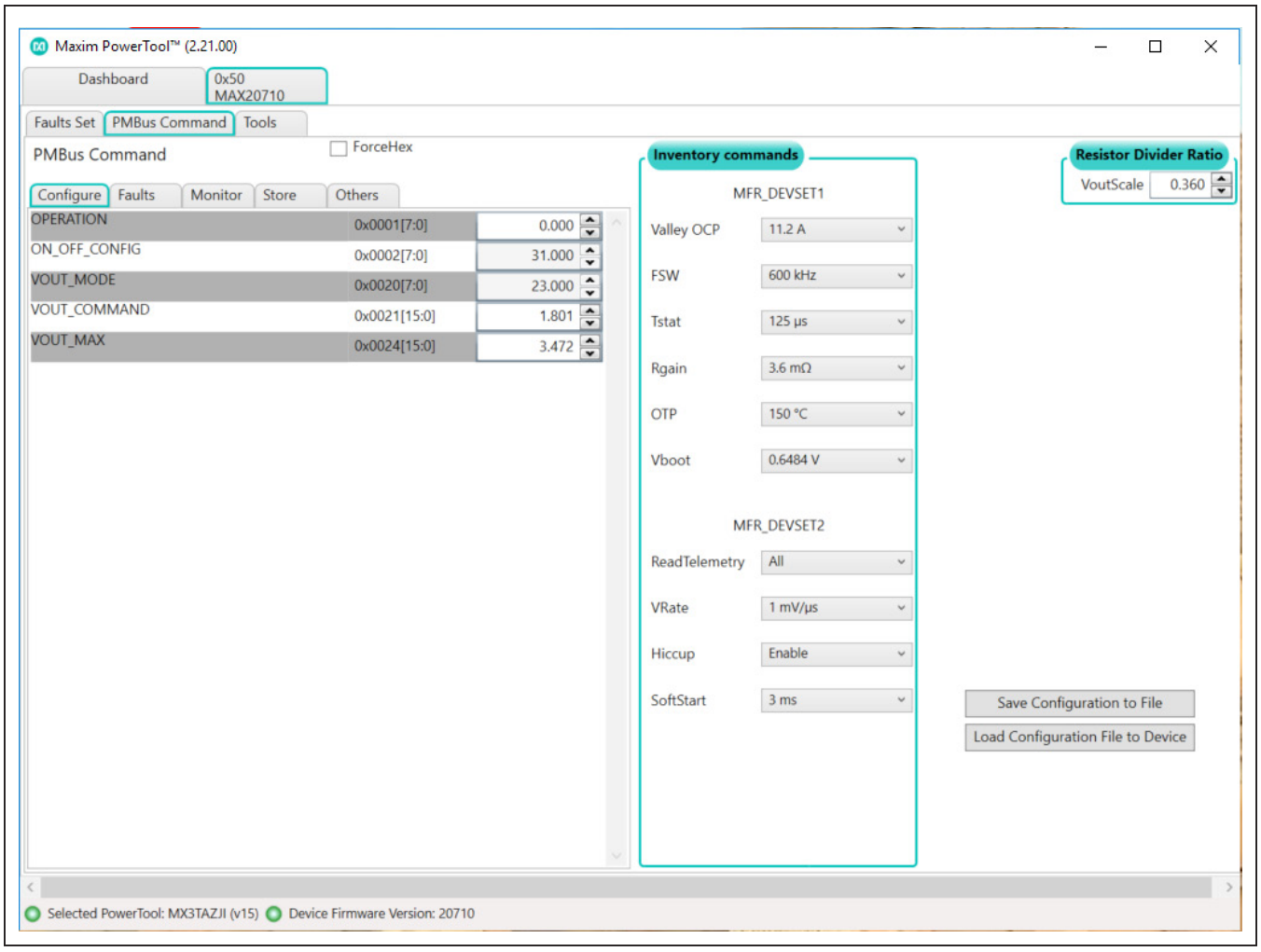

Figure 5. MAXPOWERTOOL002# GUI showing the output voltage scaling factor circled in red.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—

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