ADP1829 Reference Design

Preliminary Technical Data

FCDC 00054

FEATURES

Two Output Voltages: 3.3 V, 1.0 V
Output Current: 3.0 A, 8.0 A
Input voltage: 10.8 V – 13.2 V
Ripple <2% ppk of Output Voltage
Transient step ±5%, 80% max load

ADP1829 REFERENCE DESIGN DESCRIPTION

This ADP1829 Reference Design uses 10.8 V to 13.2 V for the input voltage. The output voltages and currents are as follows:

- V_{OUT1} = 3.3 V with a maximum output current of 3.0 A
- V_{OUT2} = 1.0 V with a maximum output current of 8.0 A

The ripple and transient assumptions are 2% or less peak to peak voltage ripple and 5% deviation due to 80% instantaneous load step (10% to 90%). The switching frequency is fixed at 300 kHz. All components are surface mount.

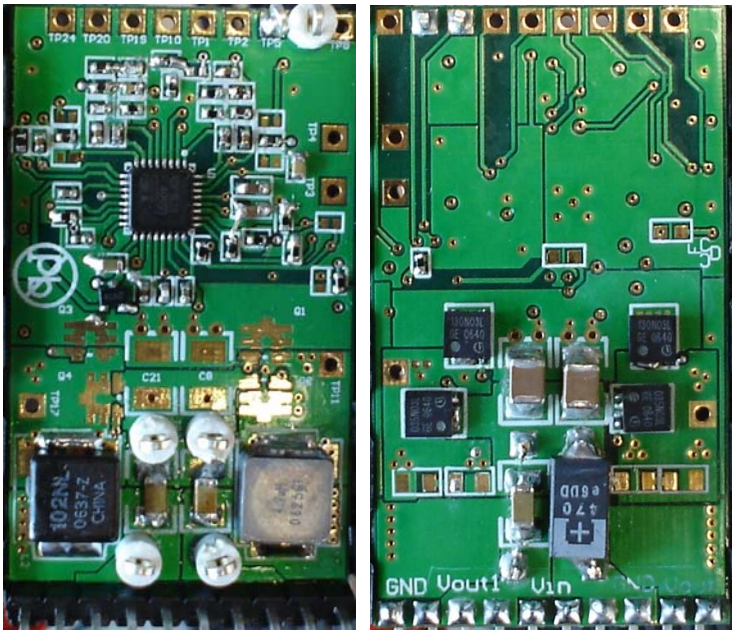

Figure 1. ADP1829 Evaluation Board

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REVISION HISTORY

8/27/2007—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADP1829 is a versatile, dual output, interleaved, synchronous PWM buck controller that generates two independent outputs from an input voltage of 3.0 V to 18 V. Each channel can be configured to provide output voltage from 0.6 V to 85% of the input voltage. The two channels operate 180° out of phase, which reduces the current stress on the input capacitor and allows the use of a smaller and lower cost input capacitor.

The ADP1829 operates at a pin-selectable fixed switching frequency of either 300 kHz or 600 kHz. For some noise sensitive applications, it can also be synchronized to an external clock to achieve switching frequency between 300 kHz and 1 MHz. The switching frequency chosen is 300 kHz to get good efficiency over a wide range of input and output conditions.

The ADP1829 includes an adjustable soft start to limit input inrush current, voltage tracking for sequencing or DDR termination, independent power-good output, and a power enable pin. It also provides current-limit and short-circuit protection by sensing the voltage on the synchronous MOSFET.

SCHEMATIC

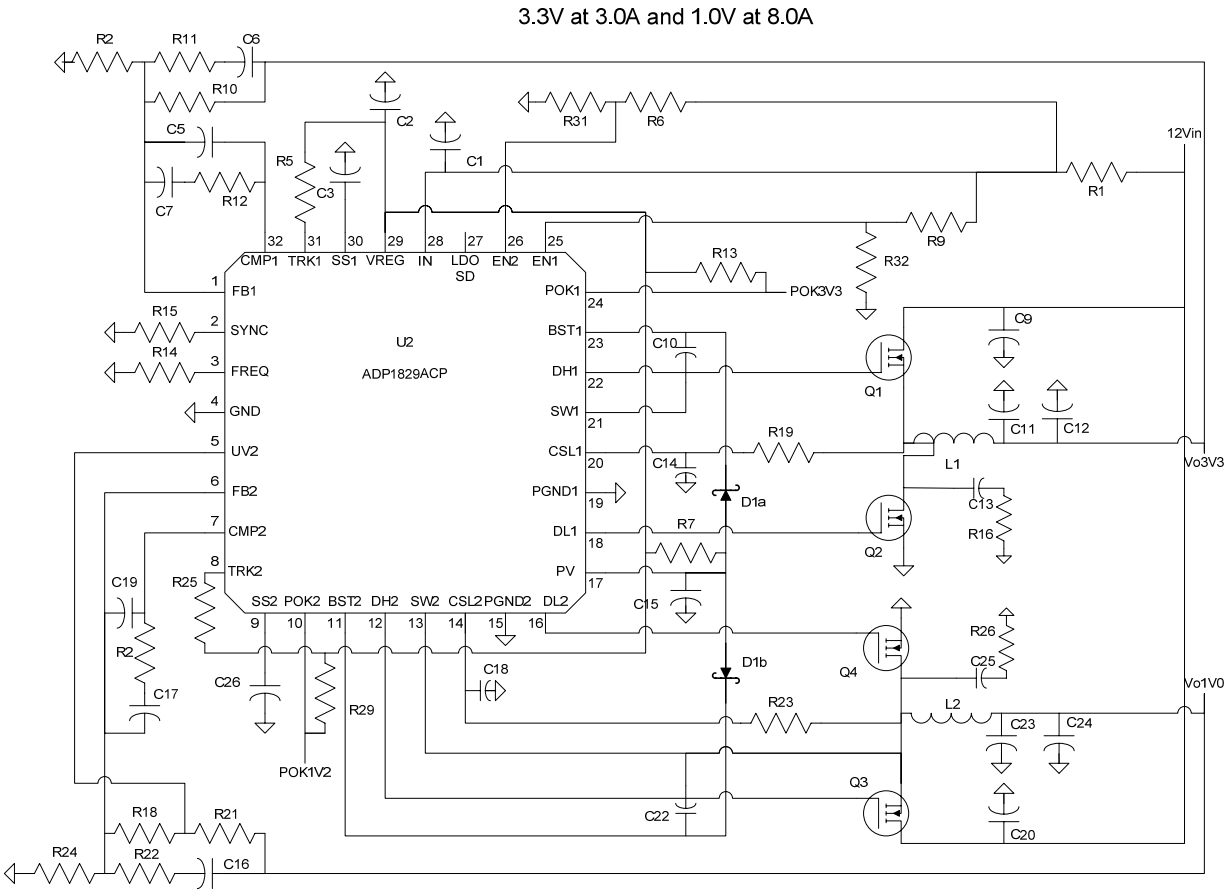

Figure 2. Schematic V_{OUT1} V_{OUT2}: 12V -> 3.3 V @ 3.0 A , 1.0 V @ 8.0 A

Bill of Materials

Table 1. V_{OUT1} and V_{OUT2}

Description	Designator	Qty	Manufacturer	MFR#
Cap Ceramic C0G 22p 0402 50V	C5, C19	2	Vishay	Generic
Cap Ceramic X7R 1u 0603 16V	C1, C2	2	Murata	GRM188R71C105KA12D
Cap Ceramic X7R 47n 0402 10V	C3	1	Vishay	Generic
Cap Ceramic X5R 10u 1206 25V	C9, C20	2	Murata	grm31cr61e106k
Cap POSCAP 470u 6.3V 7343 2.5V	C23	1	Sanyo	2R5TPD470M5
Cap Ceramic X5R 47u 1206 6.3V	C11, C12, C24	3	Murata	grm31cr60j476m
Cap Ceramic X7R 100n 0402 16V	C10, C22	2	Murata	GRM155R71C104KA88D
Cap Ceramic C0G 33p 0402 50V	C14, C18	2	Vishay	Generic
Cap Ceramic X7R 15n 0402 16V	C26	1	Vishay	Generic
Cap Ceramic X7R 1.5n 0402 50V	C16, C17	2	Vishay	Generic
Cap Ceramic X7R 2.2n 0402 50V	C7	1	Vishay	Generic
Cap Ceramic COG 680p 0402 50V	C6	1	Vishay	Generic
Diode Dual Schottky 200mA SOT-323 30V	D1	1	Diodes inc	BAT54AW
Inductor Powder 4.7uH 7.25mm x 6.75mm	L1	1	Vishay	IHLP25CZER4R7M01
Inductor Powder 1.0uH 7.5mm x 7.0mm	L2	1	Pulse	PG0426.102NL
Single N-Channel MOSFET PG-TSDSON-8 30V	Q1, Q3	2	Infineon	BSZ130N03LS G
Single N-Channel MOSFET PG-TSDSON-8 30V	Q2, Q4	2	Infineon	BSZ035N03LS G
Res 5% Thick Film 10 Ohms 0402	R1, R7	2	Vishay	Generic
Res 1% Thick Film 10.0k 0402	R12, R13, R29	3	Vishay	Generic
Res 1% Thick Film 20.0k 0402	R10, R20, R21, R31, R32	5	Vishay	Generic
Res 1% Thick Film 634 Ohms 0402	R19	1	Vishay	Generic
Res 1% Thick Film 1.62k 0402	R23	1	Vishay	Generic
Res 1% Thick Film 4.42k 0402	R2	1	Vishay	Generic
Res 1% Thick Film 30.1k 0402	R24	1	Vishay	Generic
Res 1% Thick Film 200 Ohms 0402	R11, R22	2	Vishay	Generic
Res 1% Thick Film 100k 0402	R6, R9	2	Vishay	Generic
2 chan 300k to 600k PWM LFCSP-32	U1	1	Analog	ADP1829ACPZ
Res 0 Ohm jumper 0402	R5, R14, R15, R18, R25	5	Vishay	Generic
No Stuff	C13, C25, R16, R26	4		

ASSEMBLY DRAWING

Figure 3. Top Assembly Drawing for 1829 Evaluation Board

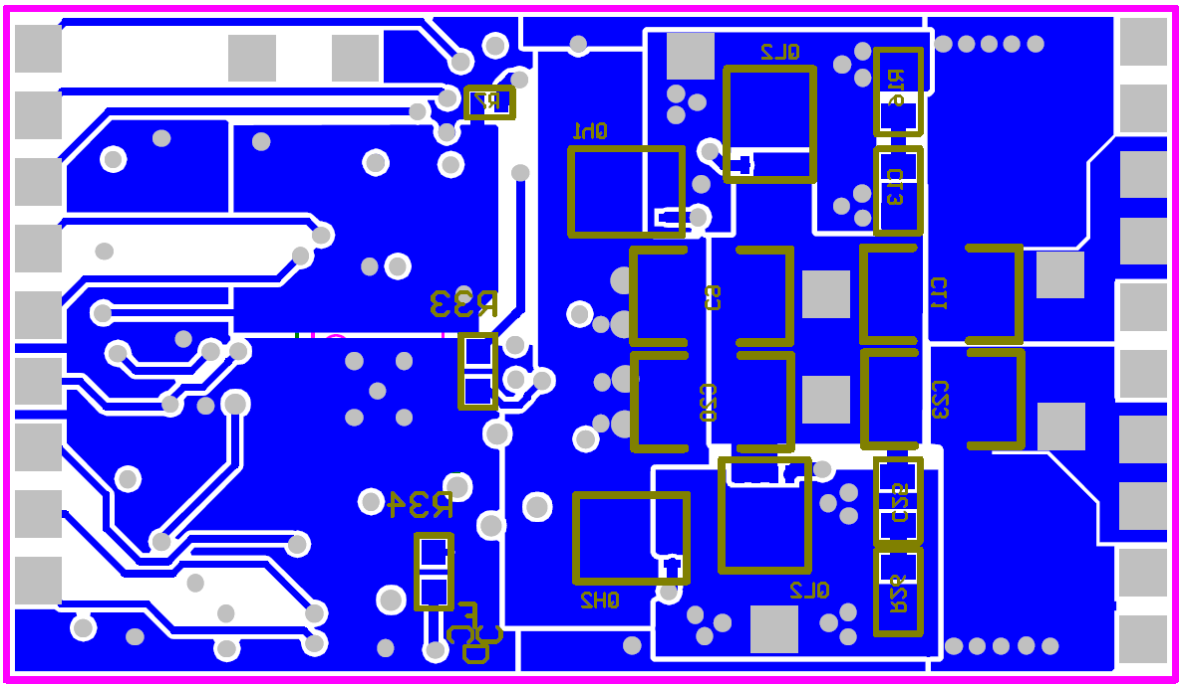

Figure 4. Bottom Assembly Drawing for 1829 Evaluation Board (looking through from top)

POWERING THE ADP1829 REFERENCE DESIGN

The ADP1829 Reference Design is supplied fully assembled.

INPUT POWER SOURCE

1. Before connecting the power source to the ADP1829 Reference Design, make sure that it is turned off. If the input power source includes a current meter, use that meter to monitor the input current.
2. Connect the positive terminal of the power source to the VIN terminal on the evaluation board, and the negative terminal of the power source to the GND terminal just below the VIN terminal.
3. If the power source does not include a current meter, connect a current meter in series with the input source voltage.
4. Connect the positive lead (+) of the power source to the ammeter positive (+) connection, the negative lead (−) of the power source to the GND pins on the board, and the negative lead (−) of the ammeter to the VIN pins on the board.

OUTPUT LOAD

1. Although the ADP1829 Reference Design can sustain the sudden connection of the load, it is possible to damage the load if it is not properly connected.
2. Make sure that the board is turned off before connecting the load.
   a) If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board with the positive (+) load connection to the V_{OUT} pins and negative (−) load connection to the GND pins next to the V_{OUT} pins.
   b) If an ammeter is used, connect it in series with the load; connect the positive (+) ammeter terminal to the evaluation board V_{OUT} pins, the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to the evaluation board GND pins next to the V_{OUT} pins.
   c) Repeat for the other V_{OUT} channel.

Once the loads are connected, make sure that they are set to the proper current before powering the ADP1829 Reference Design.

INPUT AND OUTPUT VOLTMETERS

Measure the input and output voltages with voltmeters.

1. Connect the voltmeter measuring the input voltage with the positive (+) lead connected to the VIN pins on the test board and the negative lead (−) connected to the GND test point between the inductors.
2. Connect the voltmeter measuring V_{OUT1} with the positive lead (+) connected to the test point near the V_{OUT1} pins on the test board and the negative lead (−) connected to the adjacent GND test point.
3. Connect the voltmeter measuring V_{OUT2} in the same manner.
4. Make sure to connect the voltmeters to the appropriate evaluation board terminals and not to the load or power source themselves.
5. If the voltmeters are not connected directly to the evaluation board at these connection points, the measured voltages will be incorrect due to the voltage drop across the leads connecting the evaluation board to both the source and load.

TURNING ON THE EVALUATION BOARD

Once the power source and loads are connected to the ADP1829 Reference Design, the board can be powered for operation. Slowly increase the input power source voltage until the input voltage exceeds the minimum input operating voltage of 10.8 V. If the load is not already enabled, enable the load and check that it is drawing the proper current and that the output voltage maintains voltage regulation.

TYPICAL PERFORMANCE CHARACTERISTICS

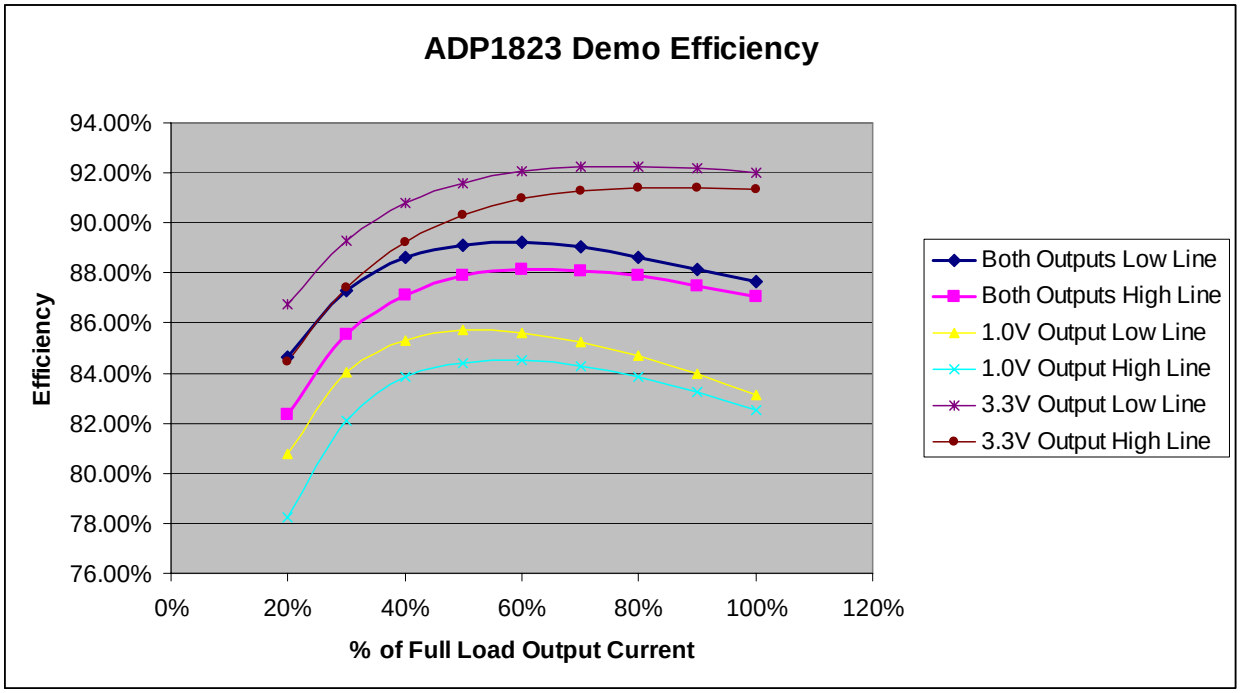

Figure 5. ADP1823 Demo board efficiency

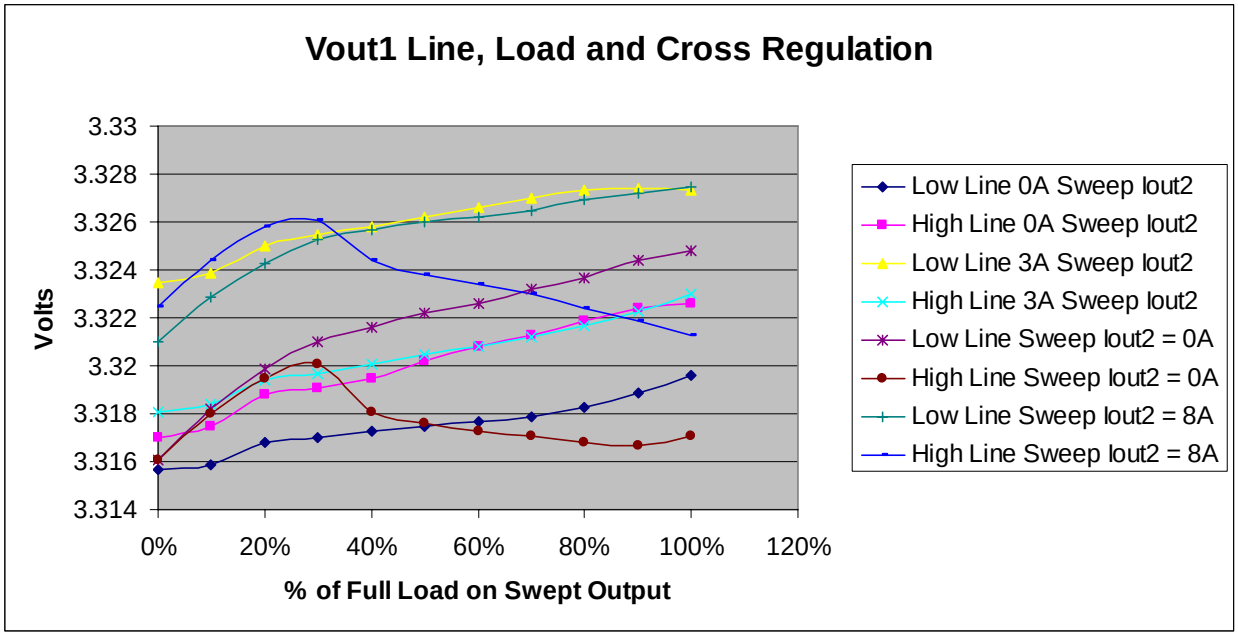

Figure 6. V_{OUT1} Load/line/cross regulation sweeping I_{OUT}

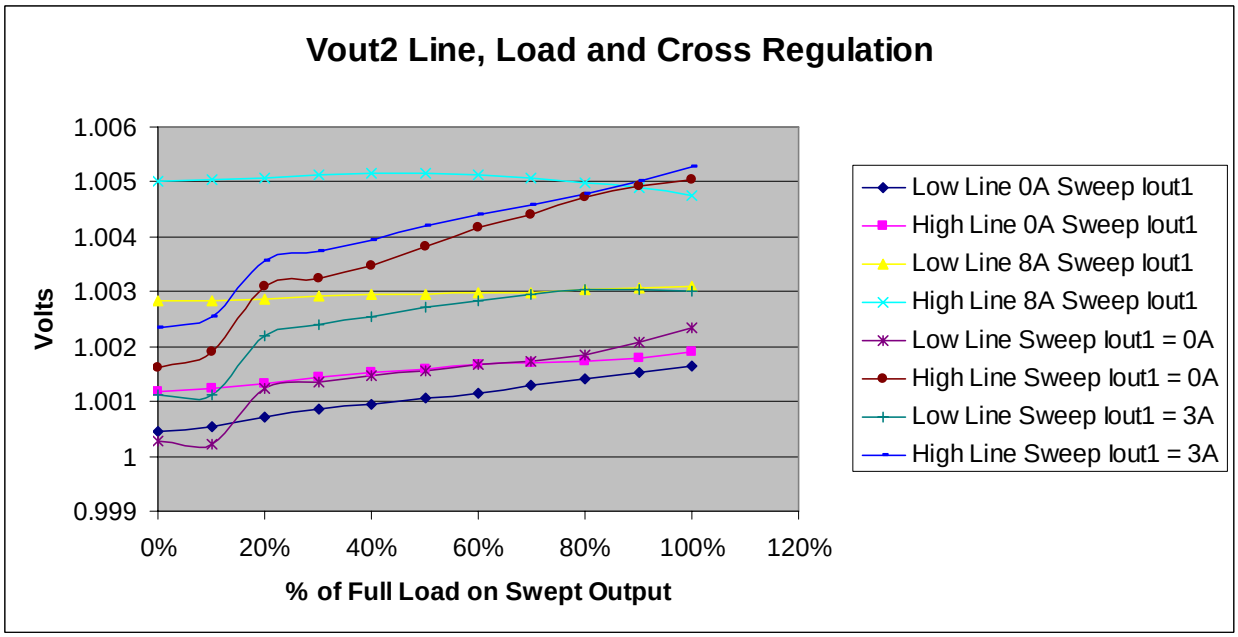

Figure 7. V_{OUT2} Load/line/cross regulation sweeping I_{OUT}

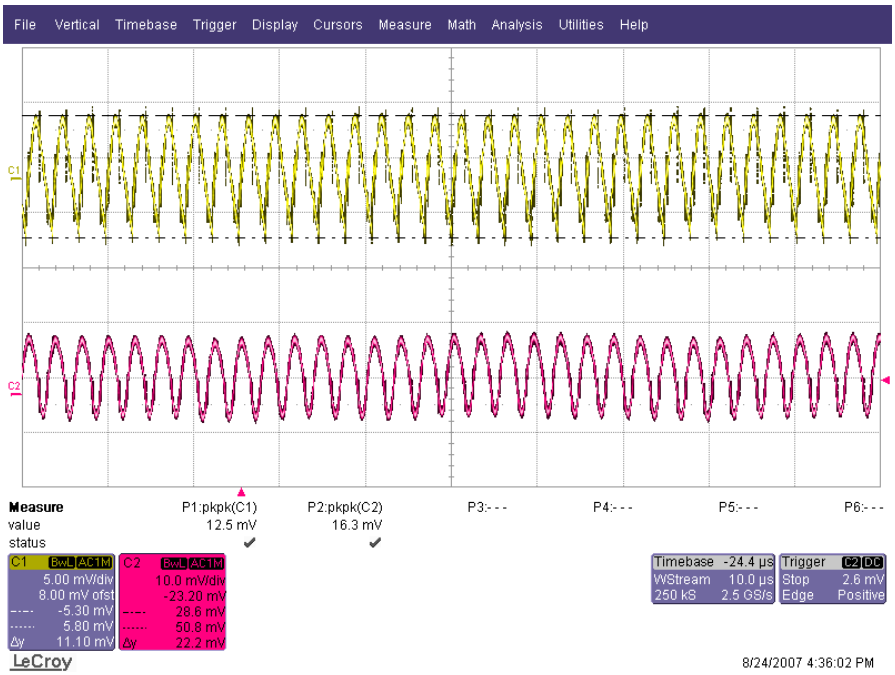

Figure 8. Voltage Ripple V_{IN} @ 10.8 V; Ch1 = 1.0 V @ 0 A, Ch2 = 3.3 V @ 0 A

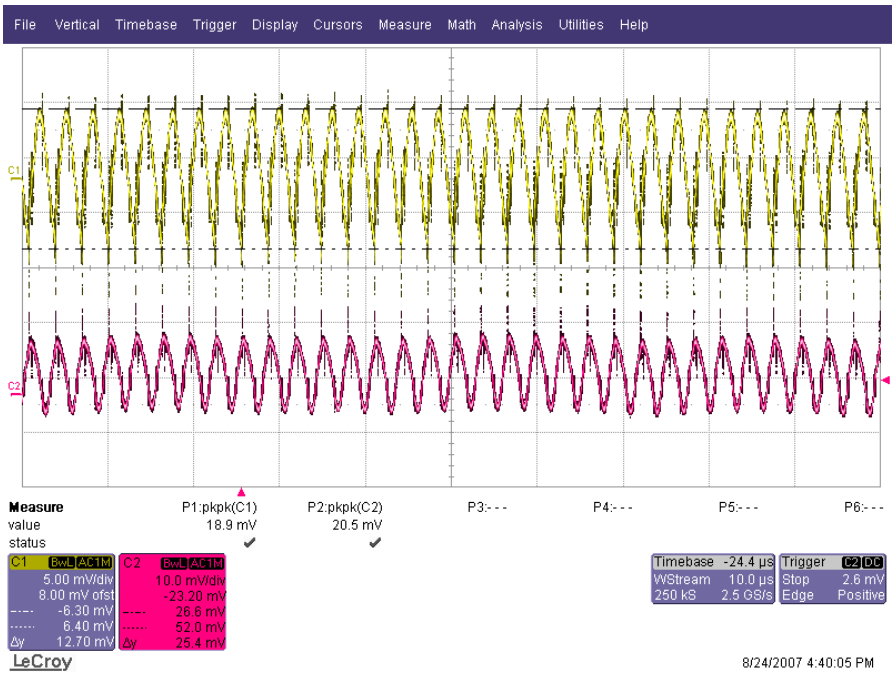

Figure 9. Voltage Ripple V_{IN} @ 10.8 V; Ch1 = 1.0 V @ 8.0 A, Ch2 = 3.3 V @ 0 A

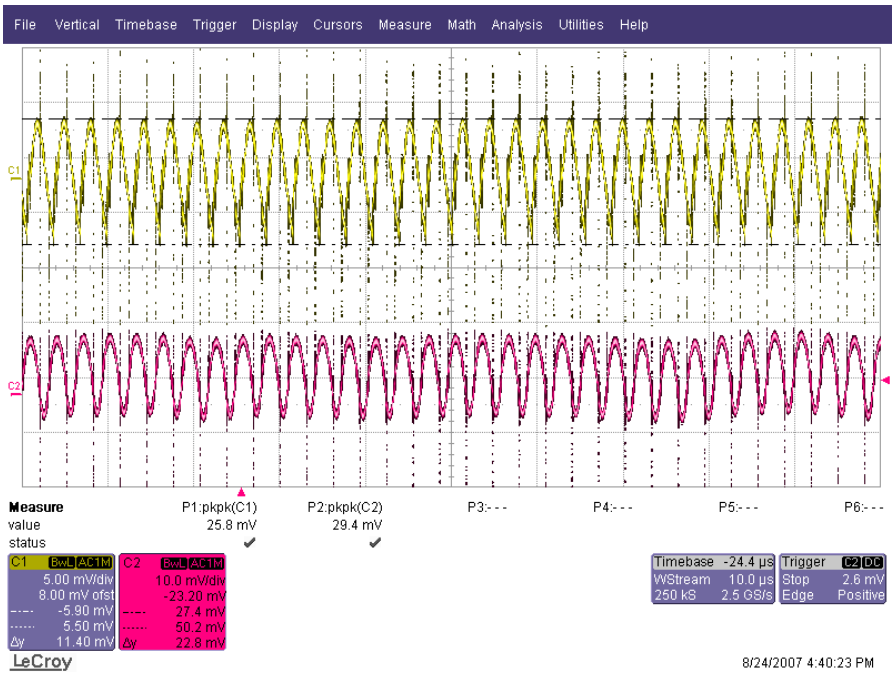

Figure 10. Voltage Ripple V_{IN} @ 10.8 V; Ch1 = 1.0 V @ 0 A, Ch2 = 3.3 V @ 3.0 A

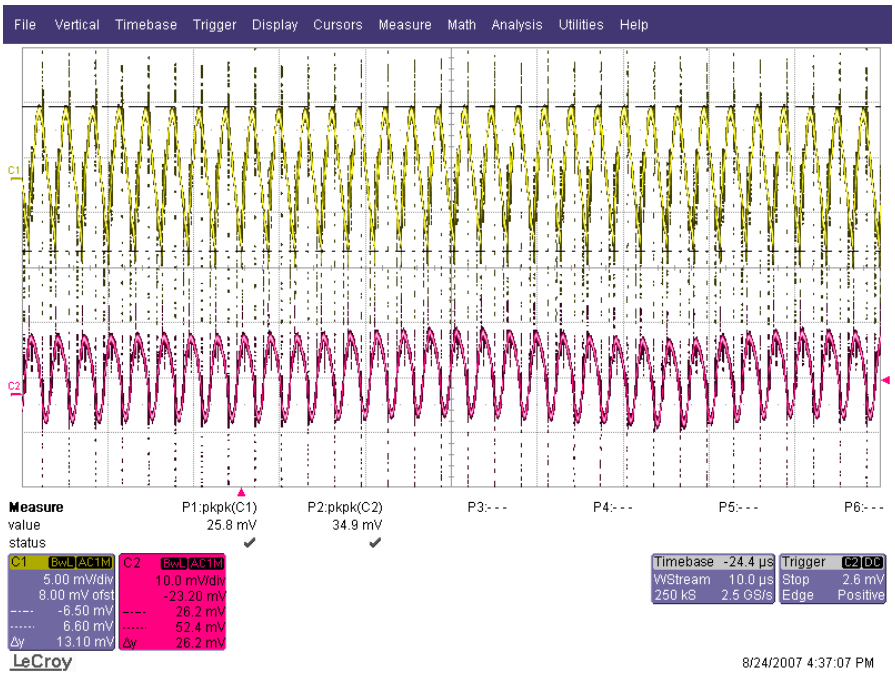

Figure 11. Voltage Ripple V_{IN} @ 10.8 V; Ch1 = 1.0 V @ 8.0 A, Ch2 = 3.3 V @ 3.0 A

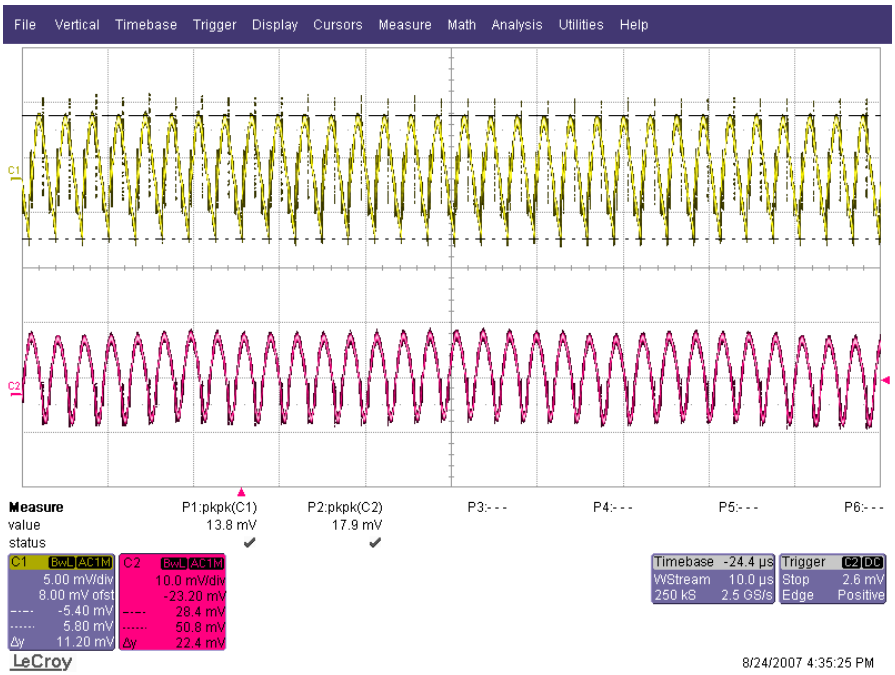

Figure 12. Voltage Ripple V_{IN} @ 13.2 V; Ch1 = 1.0 V @ 0 A, Ch2 = 3.3 V @ 0 A

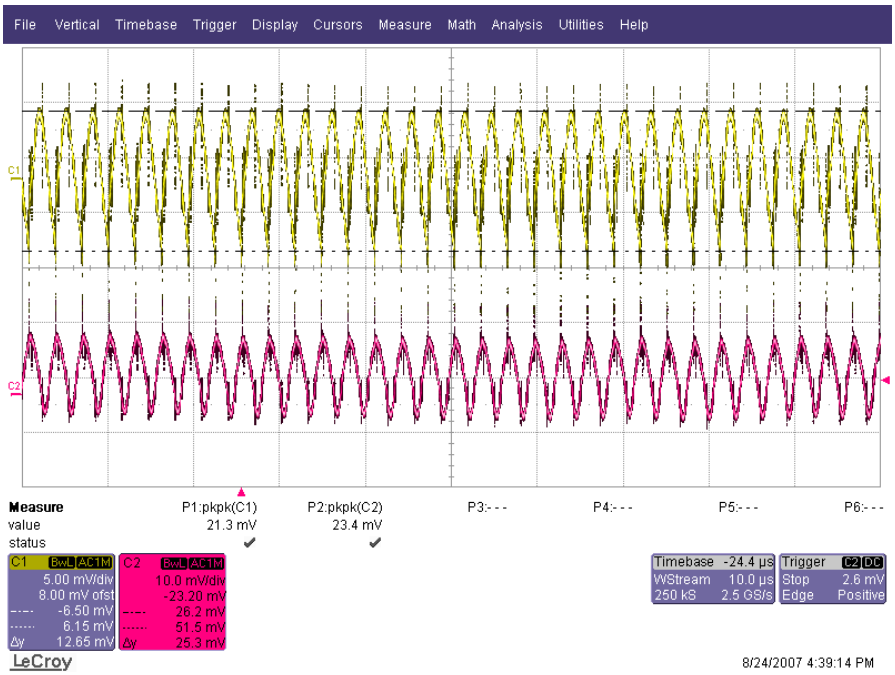

Figure 13. Voltage Ripple V_{IN} @ 13.2 V; Ch1 = 1.0 V @ 8.0 A, Ch2 = 3.3 V @ 0 A

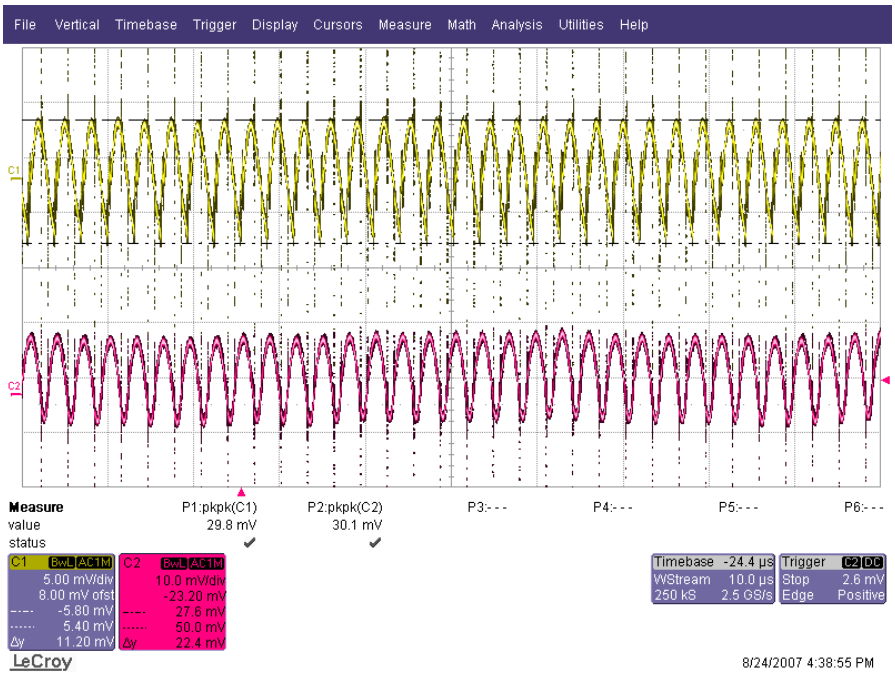

Figure 14. Voltage Ripple V_{IN} @ 13.2 V; Ch1 = 1.0 V @ 0 A, Ch2 = 3.3 V @ 3.0 A

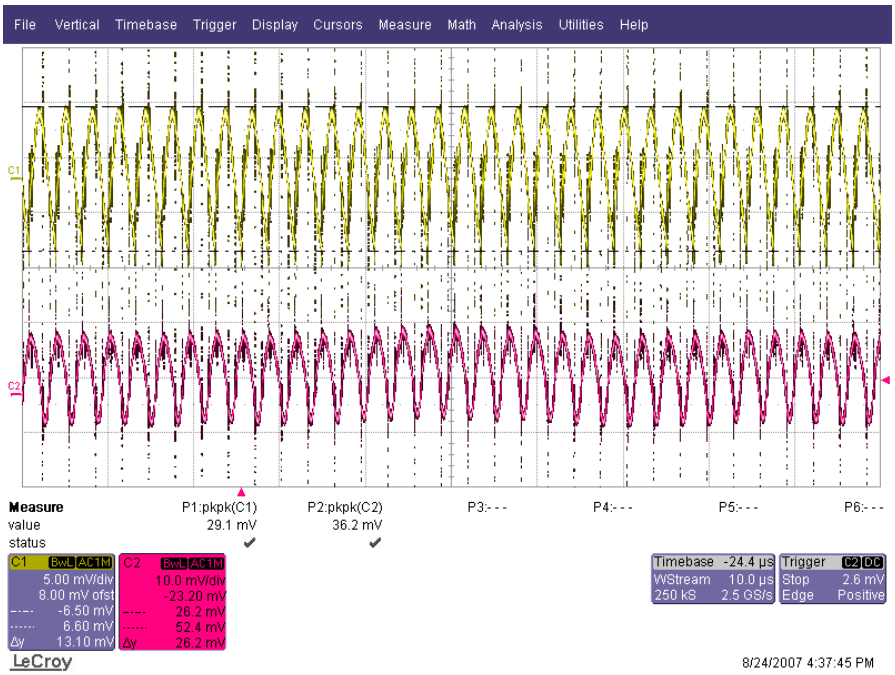

Figure 15. Voltage Ripple V_{IN} @ 13.2 V; Ch1 = 1.0 V @ 8.0 A, Ch2 = 3.3 V @ 3.0 A

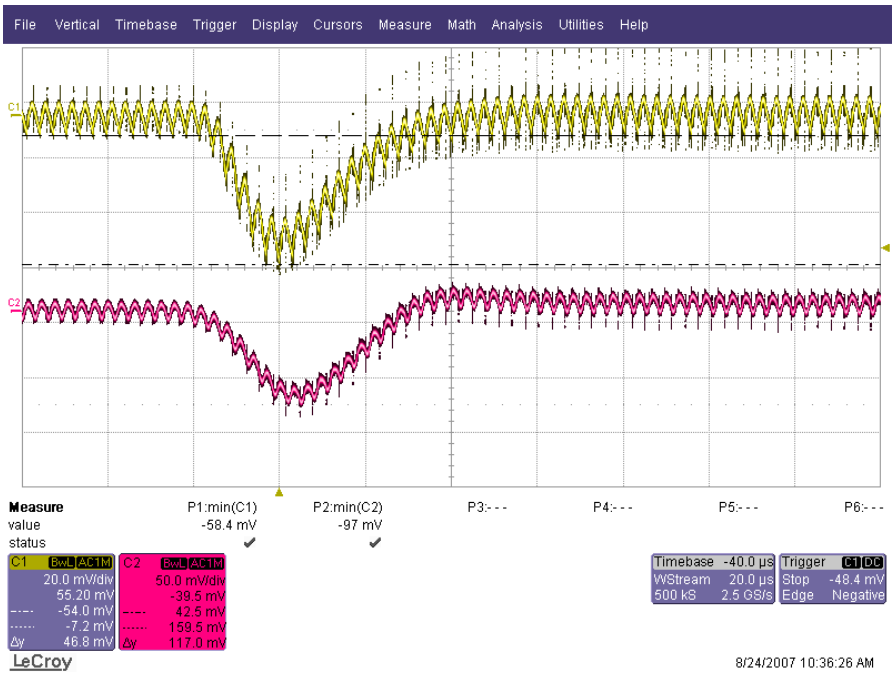

Figure 16. Load Transient V_{IN} @ 10.8 V; Ch1 = 1.0 V @ 0.8-7.2 A, Ch2 = 3.3 V @ 0.3-2.7 A

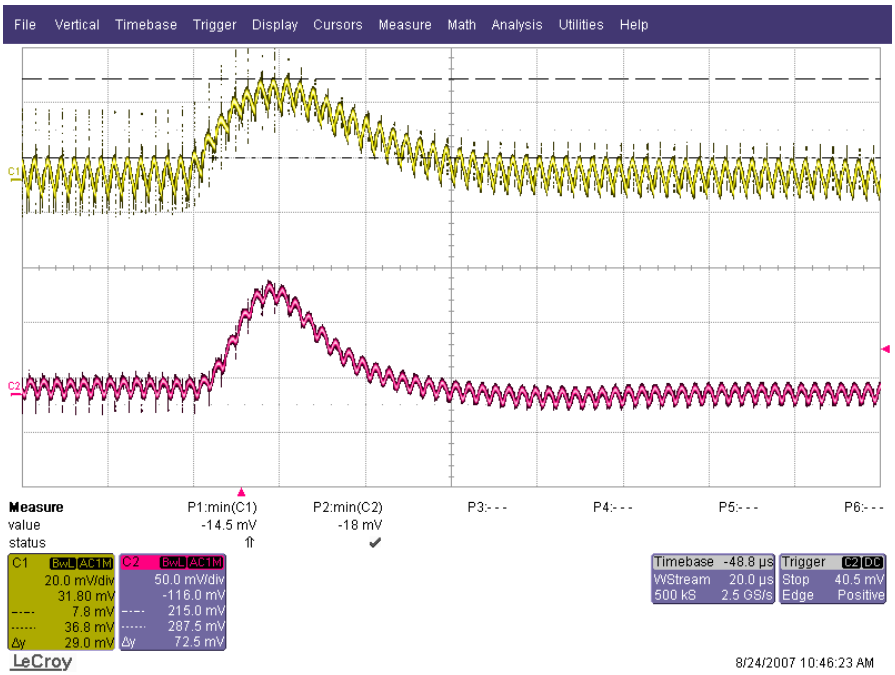

Figure 17. Load Transient V_{IN} @ 10.8 V; Ch1 = 1.0 V @ 7.2-0.8 A, Ch2 = 3.3 V @ 2.7-0.3 A

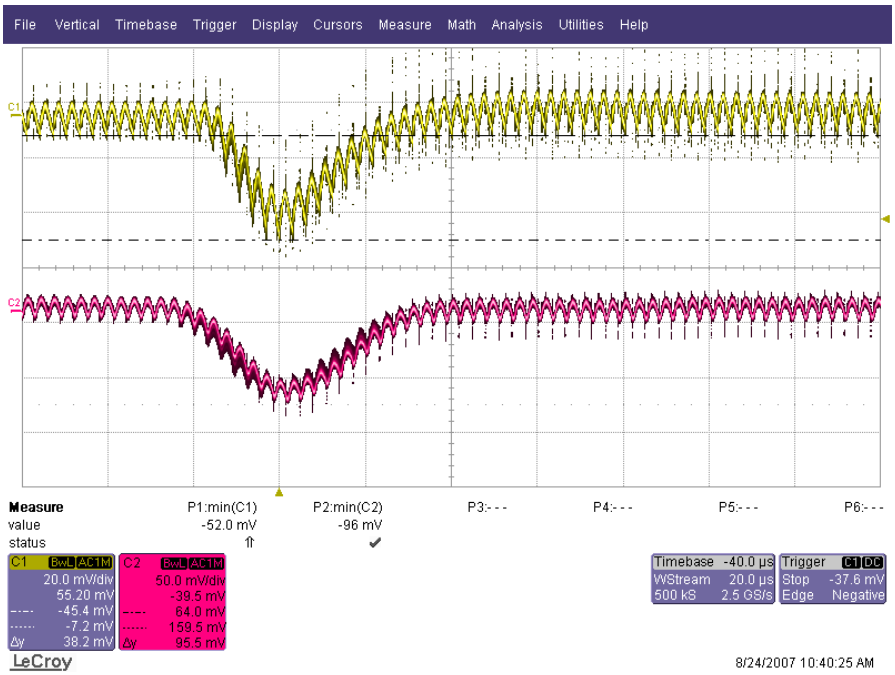

Figure 18. Load Transient V_{IN} @ 13.2 V; Ch1 = 1.0 V @ 0.8-7.2 A, Ch2 = 3.3 V @ 0.3-2.7 A

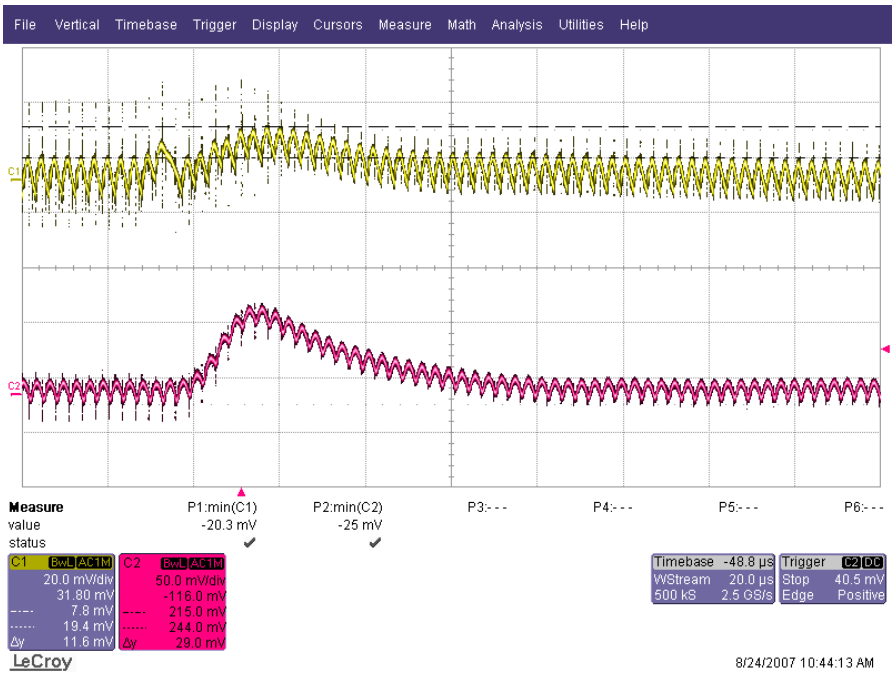

Figure 19. Load Transient V_{IN} @ 13.2 V; Ch1 = 1.0 V @ 7.2-0.8 A, Ch2 = 3.3 V @ 2.7-0.3 A

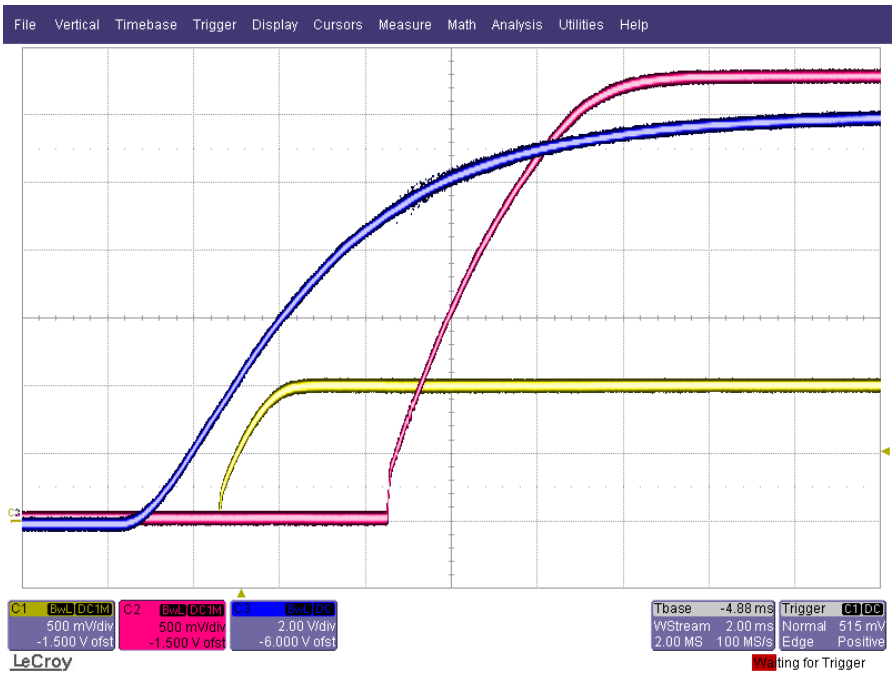

Figure 20. V_{IN} Ramped on; Ch1 = 1.0 V @ 0 A, Ch2 = 3.3 V @ 0 A, Ch3 = V_{IN}

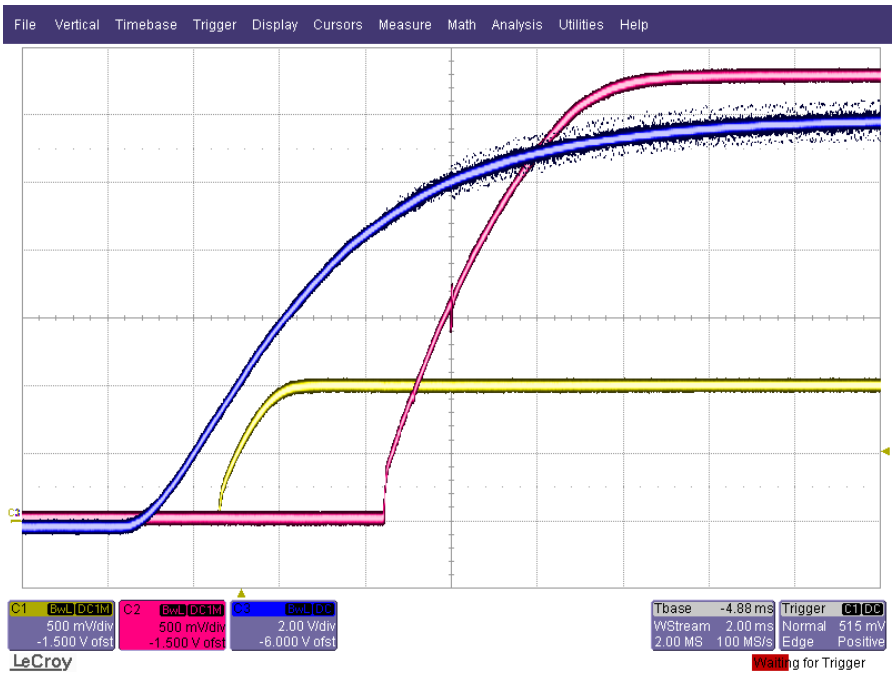

Figure 21. V_{IN} Ramped on; Ch1 = 1.0 V @ 4 A, Ch2 = 3.3 V @ 1.5 A, Ch3 = V_{IN}

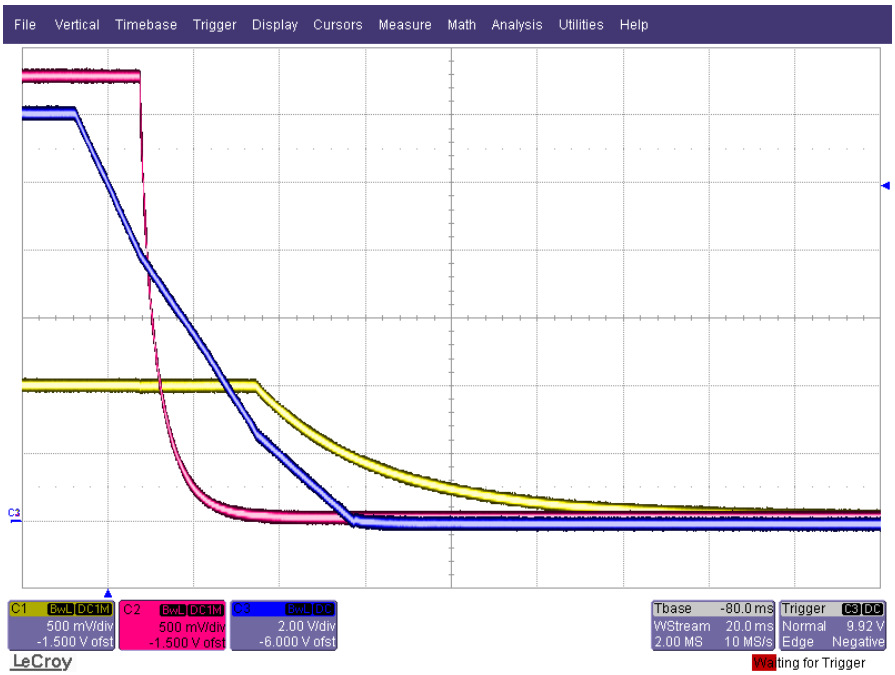

Figure 22. V_{IN} Removed; Ch1 = 1.0 V @ 50 Ohms load, Ch2 = 3.3 V @ 50 Ohms load, Ch3 = V_{IN}

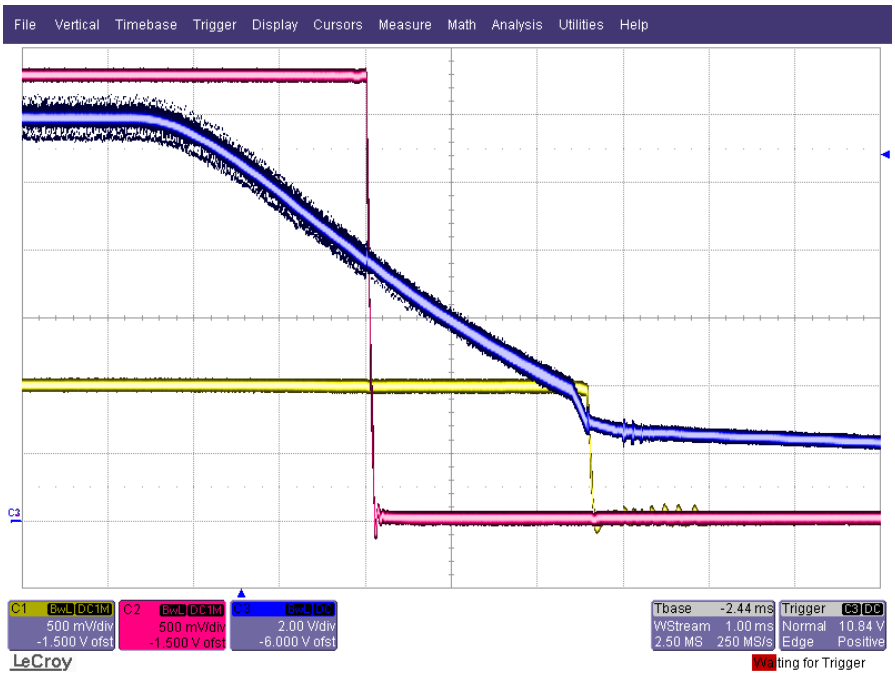

Figure 23. V_{IN} Removed; Ch1 = 1.0 V @ 8 A, Ch2 = 3.3 V @ 1.5 A, Ch3 = V_{IN}

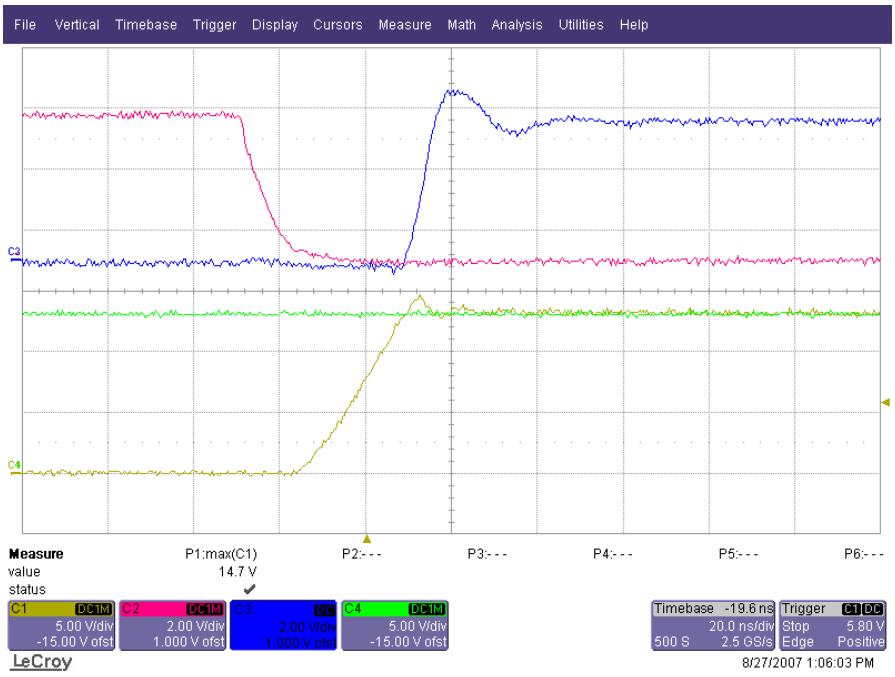

Figure 24. 1.0 V @ 0 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

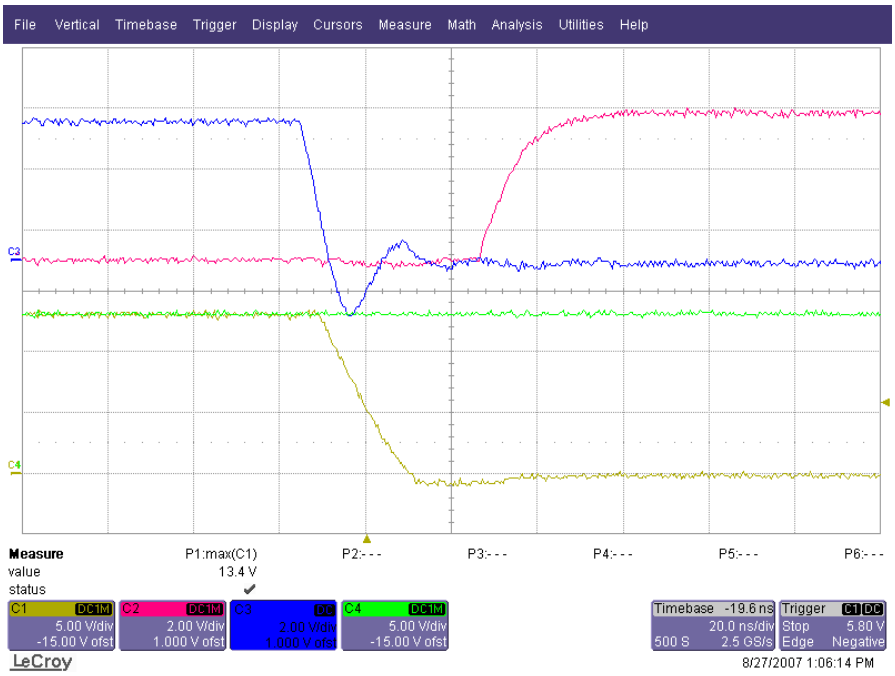

Figure 25. 1.0 V @ 0 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

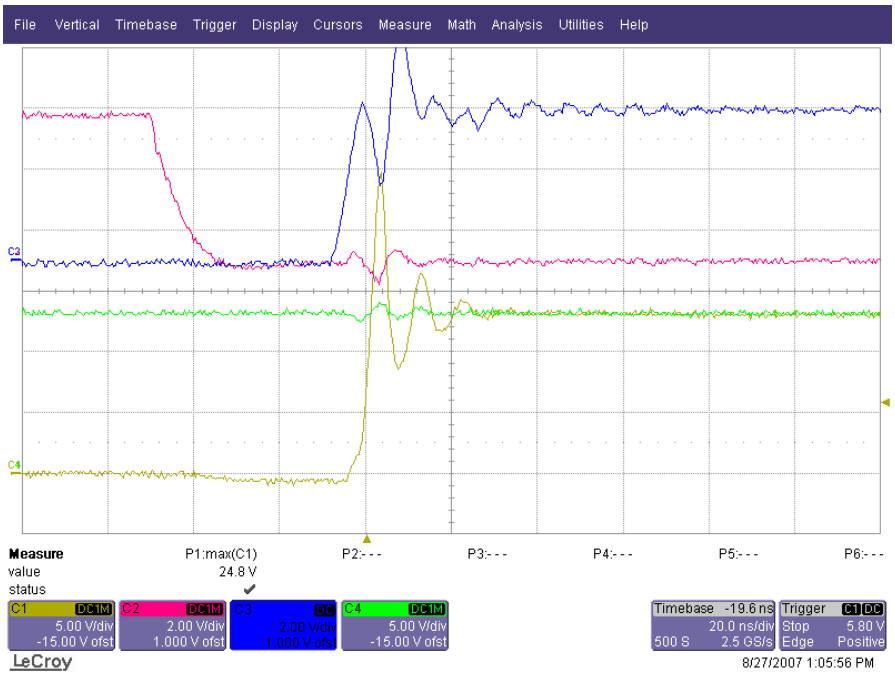

Figure 26. 1.0 V @ 8 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

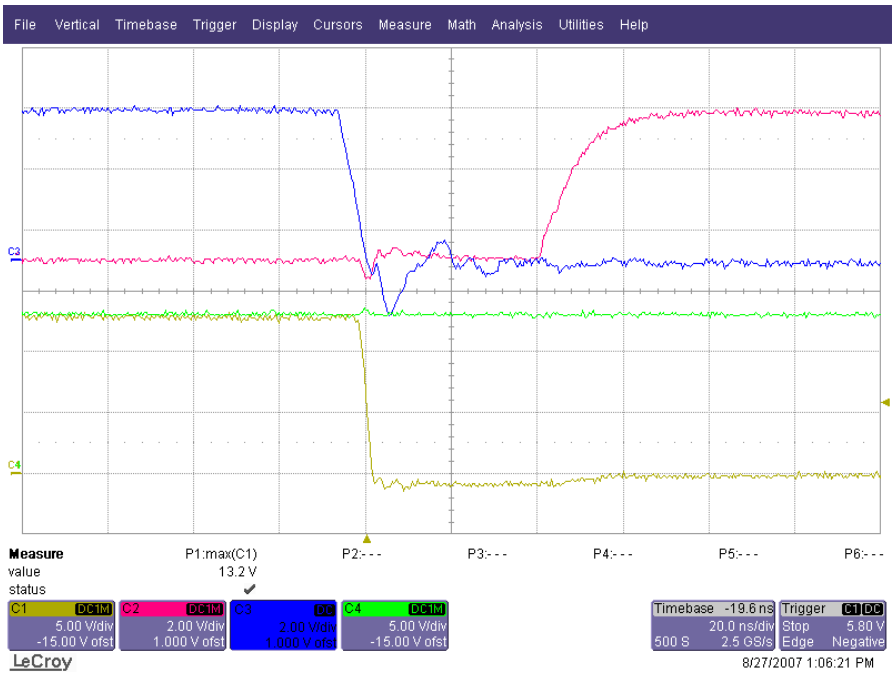

Figure 27. 1.0 V @ 8 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

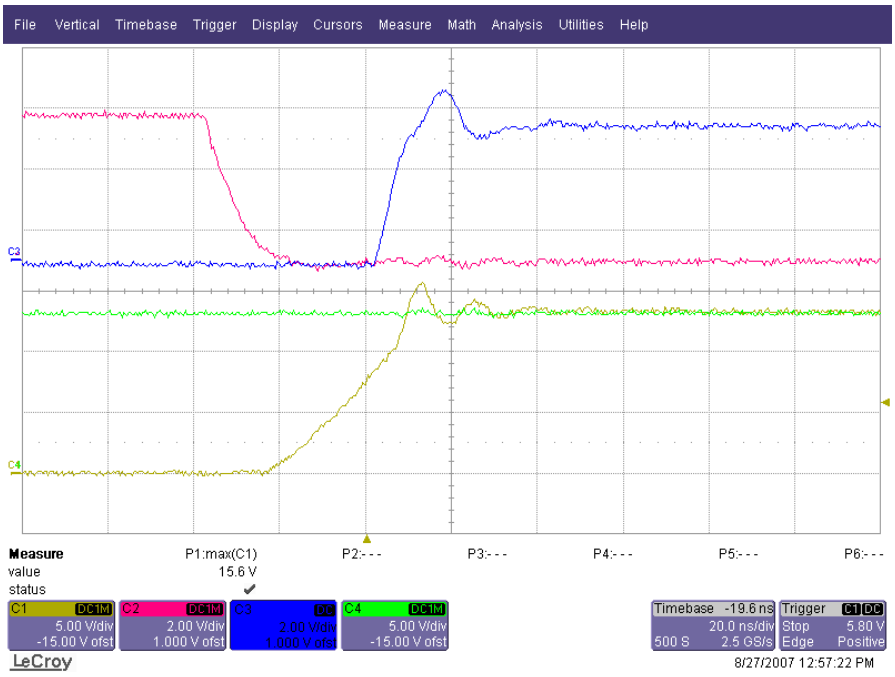

Figure 28. 3.3 V @ 0 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

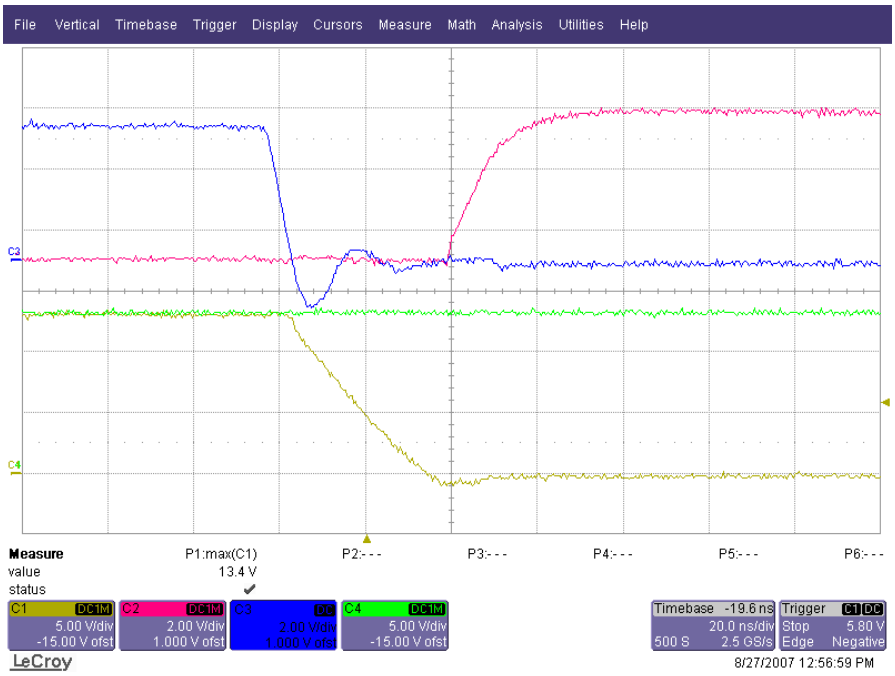

Figure 29. 3.3 V @ 0 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

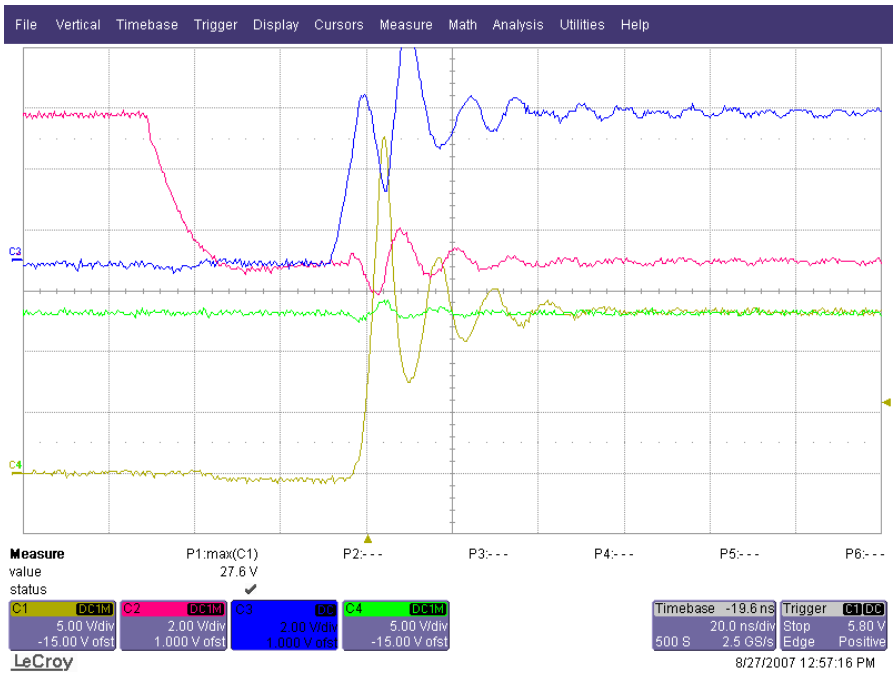

Figure 30. 3.3 V @ 3.0 A Rising Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

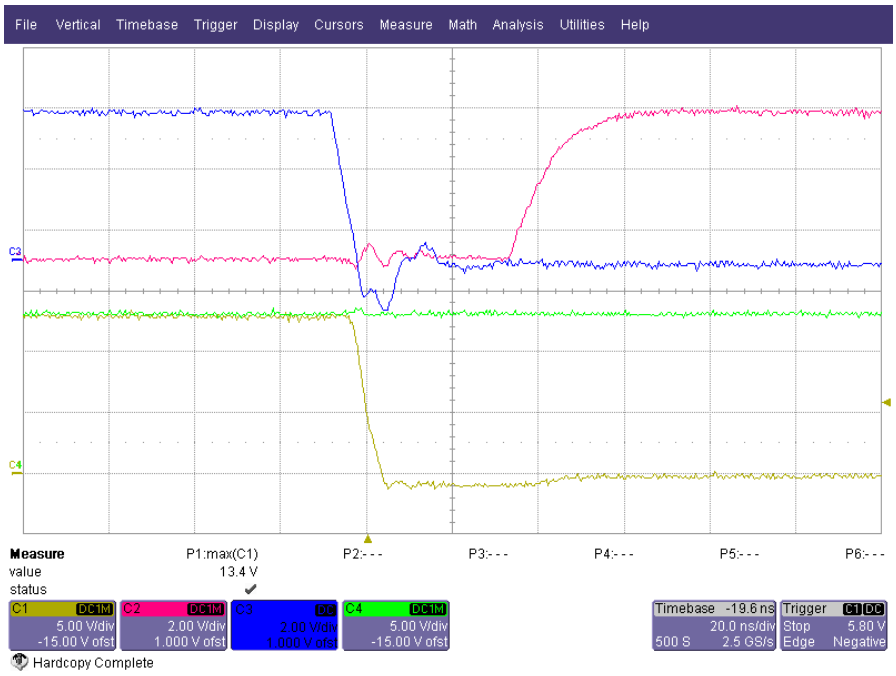

Figure 31. 3.3 V @ 3 A Falling Switchnode; Ch1 = Vds low, Ch2 = Vgs low, Ch3 = Vgs high, Ch4 = V_{IN} @ 13.2 V

NOTES

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