How to Power Your QSFP-DD Optical Transceiver

Growth in the optical transceiver market is driven by demand for higher Ethernet speed in cloud computing, the Internet of Things, and virtual data centers. Current speeds of 10Gbps, 40Gbps, and 100Gbps will soon be surpassed by 200Gbps and 400Gbps. With the increase in speed, the power consumption of the optical transceiver module must increase, while its form factor needs to stay the same. This puts tremendous pressure on the module designer to use highly integrated chips consuming the lowest possible power. How do you enable more functionality while delivering power more efficiently in a tight space? This design solution presents an innovative power management system that efficiently delivers power in a small space and enables the higher speeds anticipated for the next generation of optical transceivers.

The Optical Network Interface

In an optical network interface, communications devices like switches (Figure 1) and routers reside far away from each other (up to several kilometers) and are connected with fiber optic cables. The switch or router processes information packets, while the transceiver interfaces with the cable and translates the received optical signal into electrical impulses and vice versa.

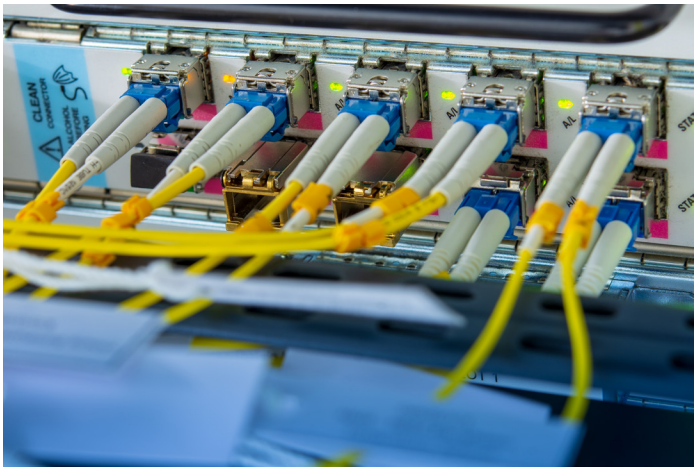

Figure 1. SFP-Transceiver Modules on Networking Switch in Data Center with Fiber Optics Cables Connected

The Optical Transceiver

Fiber optic transceivers (Figure 2) are key components of fiber optic transmission networks. They are designed in a small form-factor with integrated optical subassemblies suitable for high-density networks.

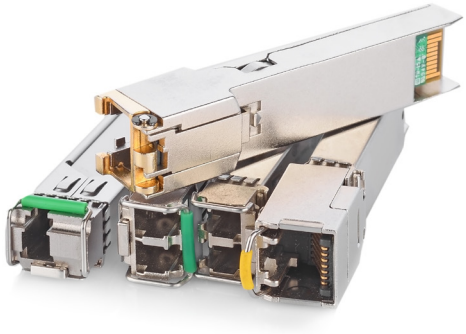

Figure 2. Optical Gigabit SFP Transceiver Module for Network Switch

The major components of a transceiver module (Figure 3) are the transmitter optical subassembly (TOSA), and the receiver optical subassembly (ROSA). The TOSA consists of a laser diode, optical interface, monitor photodiode, metal and/or plastic housing, and electrical interface. The ROSA consists of a photodiode, optical interface, metal and/or plastic housing, and electrical interface. A transimpedance amplifier (TIA) converts photodiode current into a differential voltage for further processing. An on-board DSP/PHY orchestrates the communication protocol, while a microcontroller configures the DSP/PHY, optical subassemblies, and regulators. The module's components are powered by an on-board power supply that receives the V_{CC} input (3.3V) from the host board. The 3.3V is delivered through heavy filtering to smooth out the peaks of current drawn by the transceiver components.

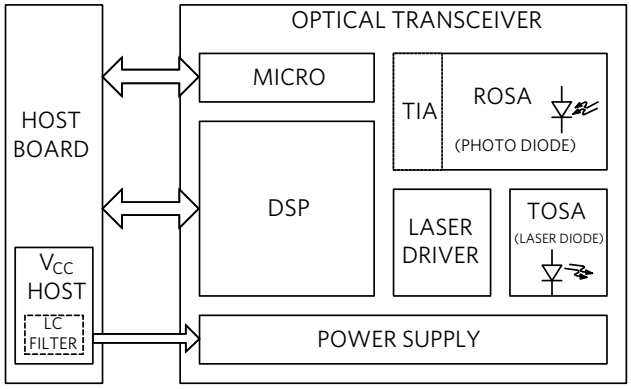

Figure 3. Optical Transceiver System

A state-of-the-art double-line density (QSFP-DD) optical transceiver with quad bandwidth, small form factor, and pluggable features has 8 power classes. Higher classes support higher data rates and longer cable reach. As an example, class 1, with 1.5W peak power and 600mA peak current can typically support a 40Gbps speed and a maximum link length of 300m. Class 7, with 14W peak power and 5.6A peak current is expected to support 400Gbps with transmission distances up to 2km. Class 8 is for highest power (>14W, 6A steady-state current).

Transceiver Power

The transceiver module power tree shown in Figure 4 reports the typical current and voltage ranges for the DSP/PHY digital, analog and PLL rails, powered by a multiple-output voltage regulator (TRIPLE BUCK). The optical interface (laser driver, TIA, ROSA, TOSA) is powered by a single regulator (BUCK). The microcontroller (MICRO) input takes 3.3V directly. The buck converters must be highly efficient to assure that the input power stays within the power envelope of the device class.

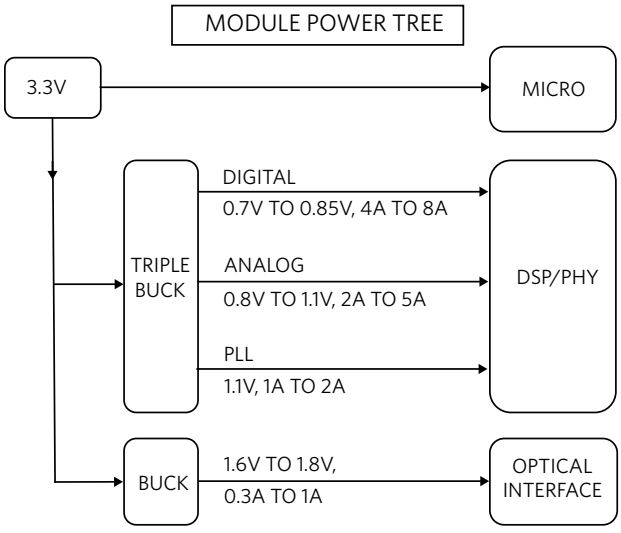

Figure 4. Transceiver Power Tree

Multiphase Architecture

For the digital rail, requiring a peak current up to 8A, a two-phase interleaved, synchronous buck converter architecture is the best solution, as shown in Figure 5.

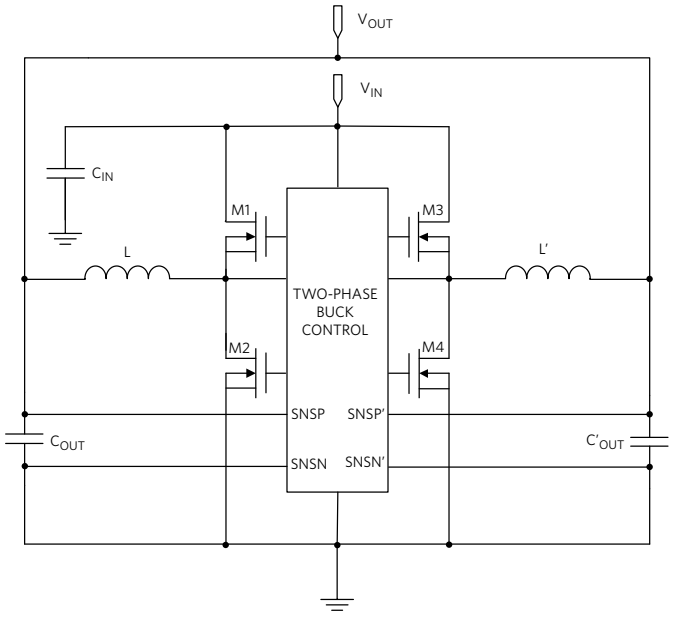

Figure 5. Two-Phase Interleaved Buck Converter

The two interleaved phases assure ripple current and hence ripple voltage reduction. Low total ripple current is obtained at a relatively low per-phase frequency of operation. As an example, Figure 6 shows that two ripple currents 180° out-of-phase at 33% duty cycle result in a total ripple current with half the amplitude of a single phase at twice the frequency. Lower output current ripple and voltage ripple at higher frequency means fewer capacitors are needed on the output, resulting in a smaller BOM.

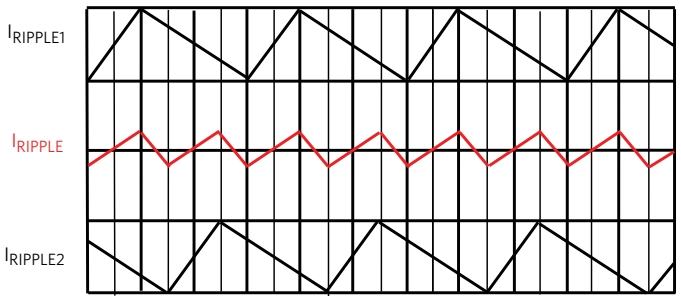

Figure 6. Two-Phase Current Ripple Reduction vs. Time

The two-phase architecture also requires fewer input capacitors. The total input current is the sum of the two out-of-phase currents (I_{IN1} and I_{IN2} in Figure 7). Here, spreading the total input current over time reduces the input current's total

RMS value, compared to a single-phase operation, allowing for a smaller input current ripple filter.

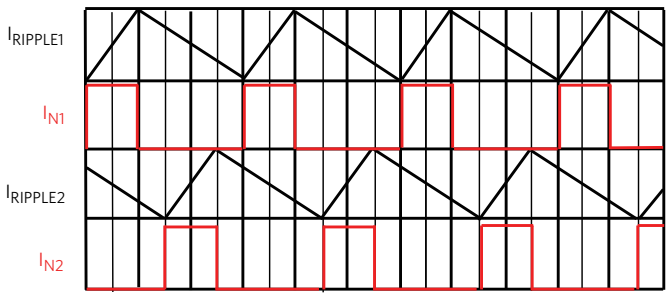

Figure 7. Two-Phase Output Ripple Currents and Input Currents vs. Time

Additionally, as shown in Figure 8, two-phase (2Φ, shown in red) is more efficient than single-phase (1Φ, shown in blue) when the two schemes run at the same output ripple frequency. Single-phase, by running at two times the switching frequency (f_{SW}) of two-phase, can also achieve high frequency and low current ripple but at higher switching losses. The two schemes have an equal number of transitions within one period, but the two-phase converter draws half the current of the single-phase converter (over twice the duration), thus reducing the switching losses.

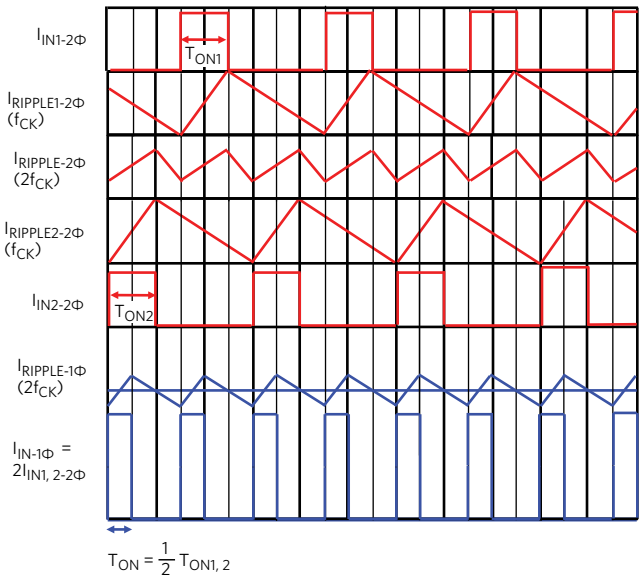

Figure 8. Two-Phase Current vs. Single-Phase Current vs. Time

Another great benefit of a two-phase converter is the fast-transient response and reduced voltage overshoot/undershoot during load steps. With half the current per phase, reduced current ripple amplitude, and double the ripple frequency, the phase switching frequency can now be pushed higher to further reduce the component size and increase the closed-loop bandwidth of the converter without running into thermal limitations.

Finally, as the total load current increases, the size of the passive components increases. For high loads, the inductor for a single-phase buck can be bulky and inefficient. Multiphase operation reduces the current in each phase, which ensures optimal sizing for passives.

Single-to-Quad-Phase, Single-to-Quad-Output, 20A Max, Configurable Buck Converter

As an example, a configurable, single-to-quad-phase, single-to-quad-output high-current, buck (step-down) converter is shown in Figure 9. High efficiency, a small PCB solution footprint, high output voltage accuracy, fast transient response, and a fast serial interface option make this device ideal for powering DSP/PHYs in optical transceiver applications. The flexible architecture allows user-selectable phase configurations such as 4 (one four-phase output), 3 + 1 (two outputs, one tri-phase and one single phase), 2 + 2 (two two-phase outputs), 2 + 1 + 1 (three outputs, one two-phase, two single-phase), and 1 + 1 + 1 + 1 (four single-phase outputs).

Single-Chip Processing System Power

By choosing the proper configuration, a single IC can power the DSP/PHY in the optical transceiver of Figure 3. In Figure 9, a 2 + 1 + 1 configuration can power the DSP/PHY digital, analog and PLL sections.

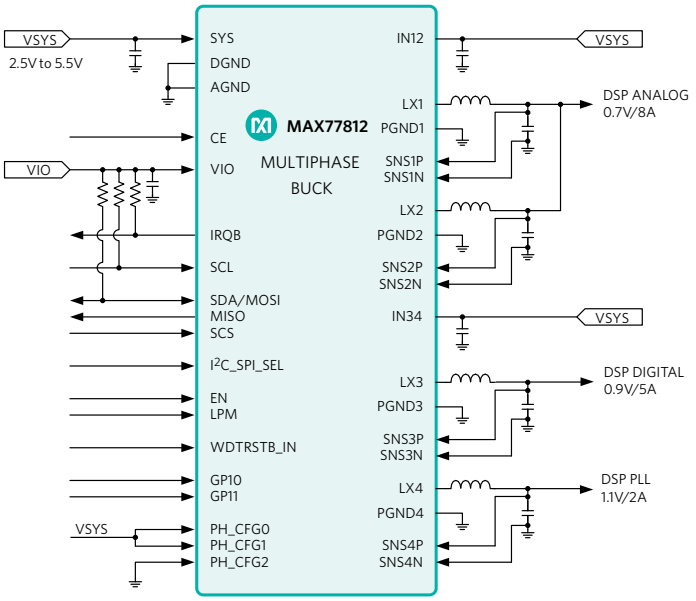

Figure 9. MAX77812 2+1+1 Application Diagram

High Efficiency

The device's two-phase efficiency curve is shown in Figure 10 (0.22µH, 2520 size inductors), covering a range of currents up to 10A.

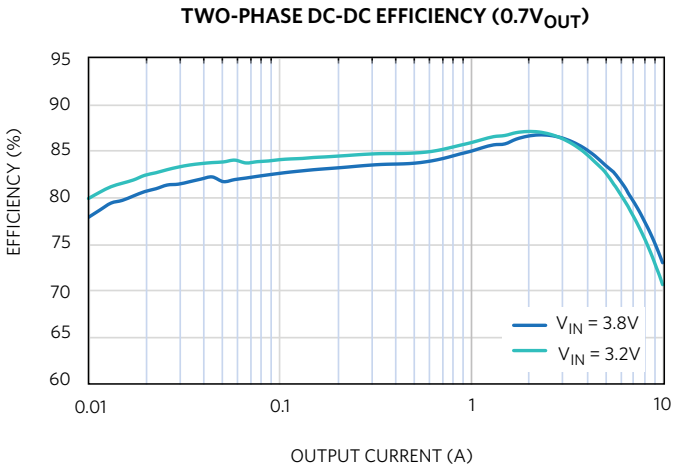

Figure 10. Two-Phase Efficiency

Thanks to the two-phase architecture, high efficiency is achieved even with a very low duty cycle (low V_{OUT}).

The device's single-phase efficiency curve is shown in Figure 11 (0.22µH, 2520 size inductors), covering a range of currents up to 5A.

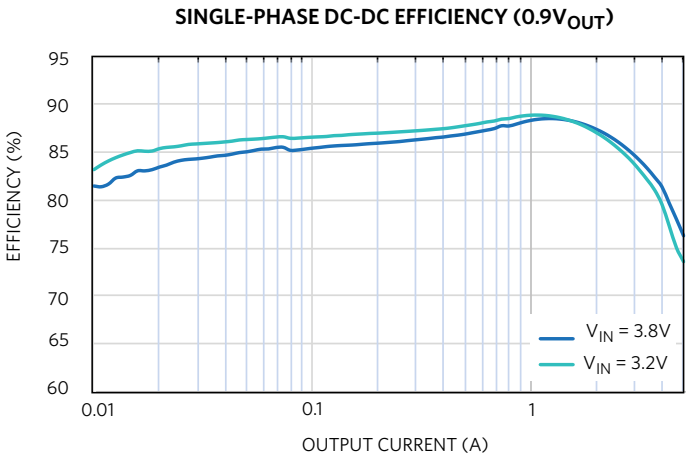

Figure 11. Single-Phase DC-DC Efficiency

Output Voltage Setting

The output voltage is programmable in 5mV steps via a serial interface. When powering the microprocessor, these fine adjustments minimize the power losses under light load operation. The default output voltages are set by OTP (one-time programmable) values at the factory and they can be overwritten by updating the new value in the output voltage setting registers even prior to enabling the outputs.

Startup and Shutdown Sequence

The MAX77812 supports programmable startup and shutdown delay times between the master phases. The startup and shutdown delay times between the master phases are programmable from 0 to 62ms (32 steps). This feature eliminates the need for an external sequencer, saving additional BOM cost and space.

Small Size

A miniature PCB footprint is achieved due to the 64-bump, 0.4mm-pitch WLP package and the use of small-size inductors and capacitors. A programmable current limit minimizes the inductor sizes based on the system's actual requirements. Figure 12 shows the PCB footprint occupying only about 79mm^2.

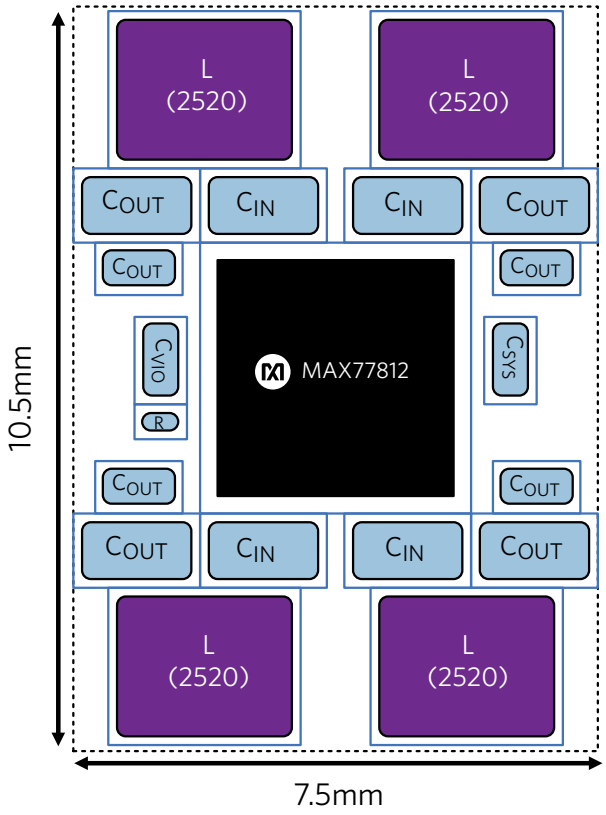

Figure 12. Small -Size PCB 2 + 1 + 1 Buck Converter (78.75mm^2)

High-Efficiency, Ultra-Small Single Buck Converter

The single-phase buck converter of Figure 4 can be implemented with the application circuit shown in Figure 13.

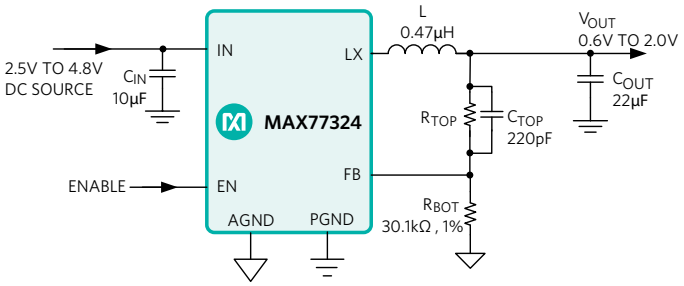

Figure 13. Advanced LED Lighting System

The efficiency curve with 1.8V output is shown in Figure 14. The solution delivers an outstanding +90% efficiency over most of the operating range.

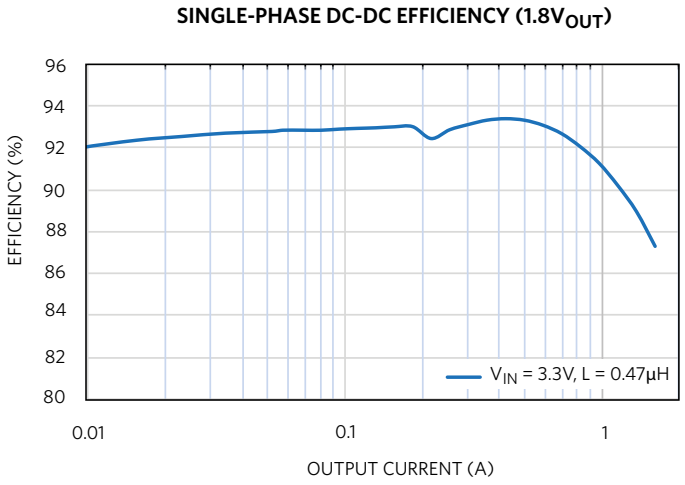

Figure 14. Single Buck Converter Efficiency

The application circuit occupies minimal space as shown in Figure 15. The WLP technology and small passives yield a PCB size of only about 7mm^2.

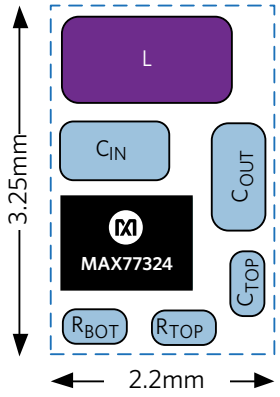

Figure 15. Single Buck Converter PCB (6.89mm^2)

Conclusion

We have discussed the optical transceiver's challenge of delivering high data rates within the constraints of the maximum power dissipation allowed for each class of QSFP-DD devices. Thanks to its high efficiency and small PCB size, the single-to-quad-phase, single-to-quad-output high-current buck regulator is an ideal choice for powering high data rate optical transceivers.

This converter's flexible architecture allows user-selectable phase configurations, making it easy to adapt to specification changes, thereby speeding up design, qualification, and time to market. A single, small-sized, high-efficiency buck converter was proposed to power the optical interface.

Glossary

DSP: Digital signal processor

PHY: Physical layer. It handles bit-level transmission between different devices and supports electrical or mechanical interfaces connecting to the physical medium for synchronized communication.

PLL: Phase-locked loop

QSFP-DD: Quad-bandwidth, small form factor, pluggable-double-line density

ROSA: Receiver optical subassembly

SFP: Small form factor, pluggable

TIA: Transimpedance amplifier

TOSA: Transmitter optical subassembly

WLP: Wafer-level package

Learn more

MAX77812 Quad-Phase, 20A Max, Configurable Buck Converter

MAX77324 4.8V$_{IN}$, 1.5A High-Efficiency, Ultra-Small Buck Converter

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