AD9510 Datasheet Comparison to ADIsimCLK
CLK INPUT = 245.76MHz

File: AD9510_245_76_LVPECL_LVDS_CMOS.clk

In this design file the ADIsimCLK predicted performance for the AD9510, 1.2GHz, 8-channel Clock Distribution IC is compared to actual measured lab results. Graphs are provided which plot both the ADIsimCLK phase noise curves and the AD9510 datasheet phase noise curves. Conditions are specified below.

245.76MHz	CLK Input	Must have excellent phase noise for testing
245.76MHz	OUT0/OUT0B	differential LVPECL
61.44MHz	OUT3/OUT3B	differential LVPECL
245.76MHz	OUT4/OUT4B	LVDS
122.88MHz	OUT5/OUT5B	LVDS
245.76MHz	OUT6	CMOS
61.44MHz	OUT7	CMOS

In this example, only the distribution section of the AD9510 chip is being tested. The PLL core is not being used.

Note that ADIsimCLK allows the user to create custom input clocks. By starting with custom oscillators specified with high-performance, the user can determine the jitter limitation of the AD9510 clock distribution section. This serves as a good baseline for seeing what performance is possible. The user can then change the phase noise performance of the input clock see the impact on output phase noise and jitter. For this comparison, the CLK source phase noise, amplitude and slew rate were set to closely match the test equipment used in bench measurements.

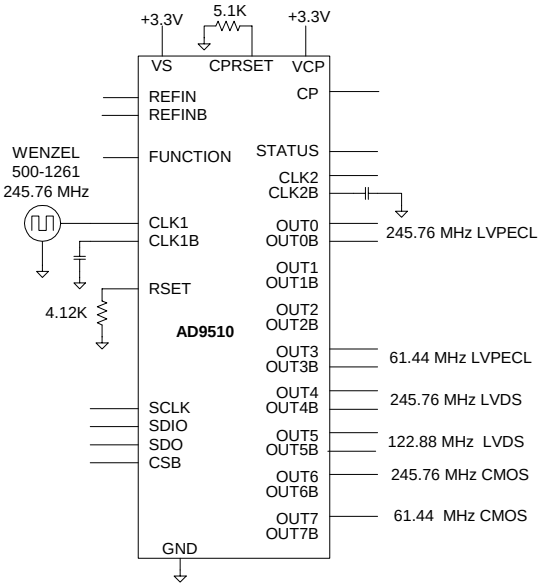
The notes and diagrams below describe how to configure the AD9510 for making datasheet comparisons at 245.76MHz. For instructions on how to navigate the ADIsimCLK page tabs and windows, please check the tutorial and help files available from the Help pulldown menu. For details on the AD9510 functionality and performance, please consult the product datasheet.

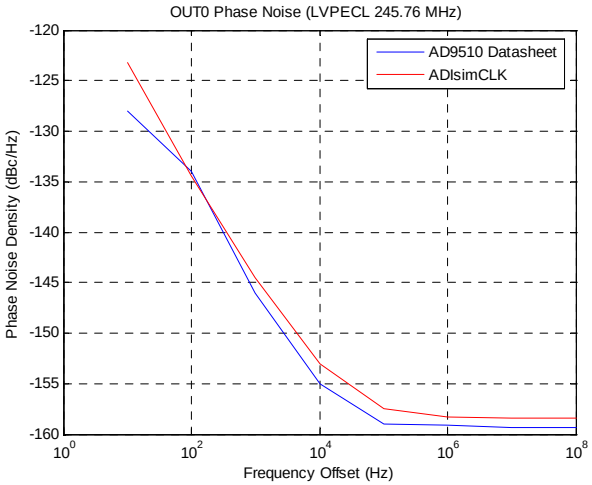
NOTES

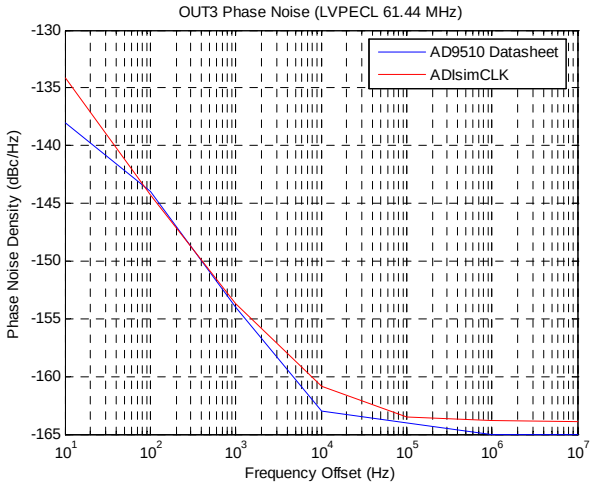
1) OUT0/OUT0B differential LVPECL clocks set to DIV=1 (divider "bypass" mode), 780mV logic swing
2) OUT1/OUT1B disabled
3) OUT2/OUT2B disabled
4) OUT3/OUT3B differential LVPECL clocks set to DIV=4, 780mV logic swing
5) OUT4/OUT4B LVDS/CMOS clock set to DIV=1 (divider “bypass” mode), LVDS mode, 3.5mA current
6) OUT5/OUT5B LVDS/CMOS clock set to DIV=2, LVDS mode, 3.5mA current; optional fine delay bypassed
7) OUT6 LVDS/CMOS clock set to DIV=1 (divider bypass mode), CMOS mode; OUT6B not connected; optional fine delay bypassed
8) OUT7 LVDS/CMOS clock set to DIV=4, CMOS mode; OUT7B not connected

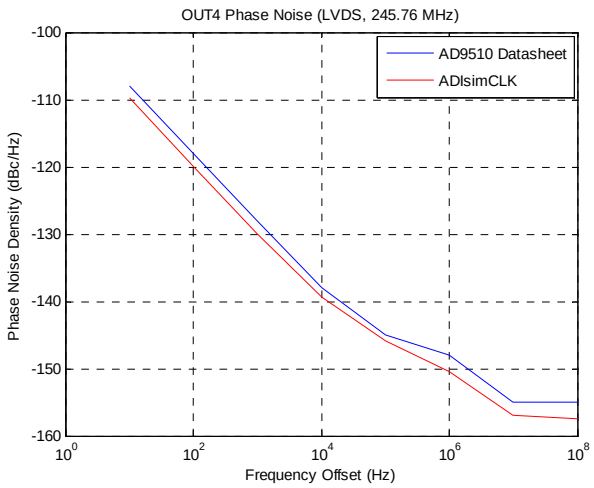
7) CLK Input source is "custom" 245.76MHz with phase noise floor (PN Floor) at -170dBc/Hz in ADIsimCLK compared to Wenzel source in lab setup.

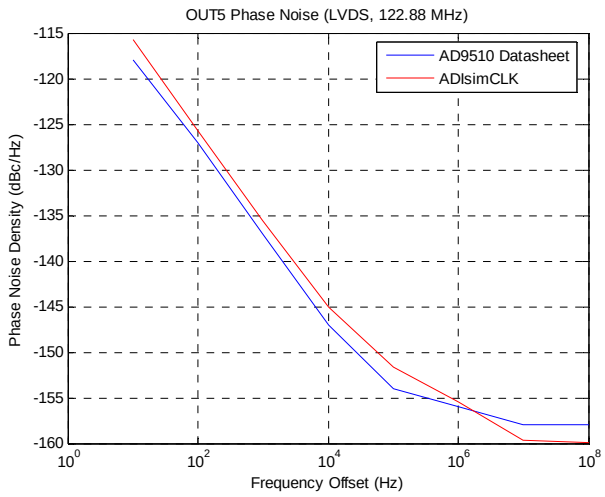
CIRCUIT

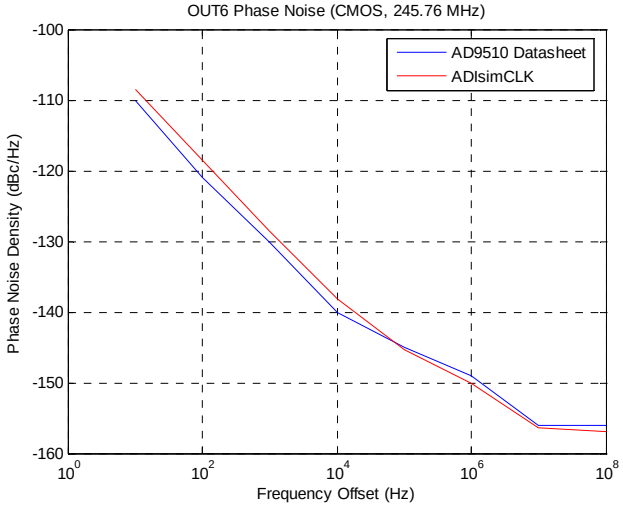


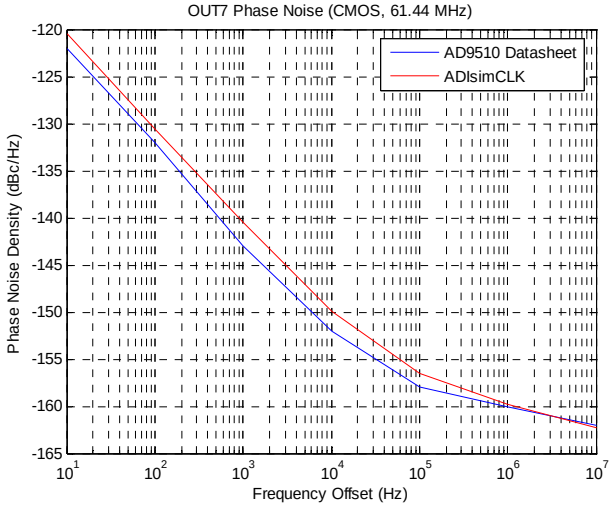





OUT4 Phase Noise (LVDS, 245.76 MHz)
AD9510 Datasheet
ADIsimCLK
Phase Noise Density (dBc/Hz)
Frequency Offset (Hz)


OUT5 Phase Noise (LVDS, 122.88 MHz)
AD9510 Datasheet
ADIsimCLK
Phase Noise Density (dBc/Hz)
Frequency Offset (Hz)


OUT6 Phase Noise (CMOS, 245.76 MHz)
AD9510 Datasheet
ADIsimCLK
Phase Noise Density (dBc/Hz)
Frequency Offset (Hz)


OUT7 Phase Noise (CMOS, 61.44 MHz)
AD9510 Datasheet
ADIsimCLK
Phase Noise Density (dBc/Hz)
Frequency Offset (Hz)