9514_quick_start.clk

Design Example Description

In this design the AD9514, 1.6 GHz, 3-Channel Clock Distribution IC is used to provide clocks to two analog-to-digital converters (ADCs) and to provide and additional reference clock.

Both ADCs require clocks with broadband jitter < 400 femtoseconds rms. Both ADCs require fast-slewing, differential LVPECL levels. ADC1 requires a 250MHz clock; ADC2 requires a 150MHz clock, while reference clock required is a CMOS 50MHz clock.
The system clock available for this example is a clean, low jitter 1.5GHz clock signal.

Because the AD9514 offers select integer divide ratios in the range of 1-32 on each clock channel, it is possible to derive the required frequencies by setting one of the dividers to DIV=6, another divider to DIV=10, and the third divider to DIV=30. Note that the AD9514 does not require a serial port for programming. By consulting the product datasheet, the user can set divide ratios, phase, delay and logic settings using the 4-level logic input pins S0-S10.

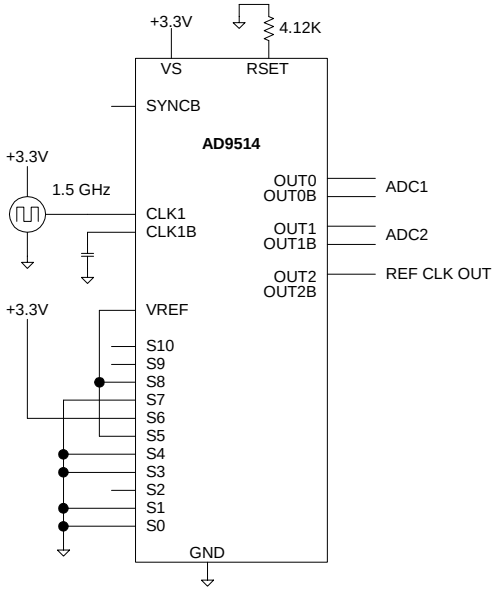
Outputs OUT0/OUT0B and OUT1/OUT1B are differential LVPECL. The third output may be programmed to either LVDS or CMOS levels. This example calls for a CMOS reference out clock. Although not used in this example, there is a complementary CMOS output available on pin OUT2B. This is available should a user need an additional CMOS clock 180 degrees out of phase with the clock on pin OUT2.

Note that ADIsimCLK allows the user to create custom input clocks. By starting with custom oscillators specified with high performance, the user can determine the jitter limitation of the AD9514 clock distribution section. This serves as a good baseline for seeing what performance is possible. The user can then change the phase noise performance of the input clock to see the impact on output clock phase noise and jitter.

The notes and diagrams below describe how to configure the AD9514 for this application. For instructions on how to navigate the ADIsimCLK page tabs and windows, please check the tutorial and help files available from the Help pulldown menu. For details on divide/phase/delay combinations available on the AD9514, please consult the product datasheet.

NOTES	
1) OUT0/OUTB Differential LVPECL clock set to DIV=6, 780mV swing 2) OUT1/OUT1B Differential LVPECL clock set to DIV=10, 780mV swing 3) OUT2 LVDS/CMOS clock set to DIV=30, CMOS mode, optional fine delay bypassed; OUT2B not connected. 4) Input Clock is custom 1.5 GHz with PN floor at -160dBc/Hz	

CIRCUIT



CIRCUITS REQUIRING CLOCKS