

## Design Example Description

In this design the AD9513, 800MHz, 3-Channel Clock Distribution IC is used to provide clocks to three analog-to-digital converters (ADCs).

All three ADCs require clocks with broadband jitter < 400 femtoseconds rms. All three ADCs require CMOS clock levels. Two of the ADCs (ADC1, ADC2) require 125MHz clocks, while ADC3 requires a 50MHz clock. The system clock available for this example is a clean, low jitter 500MHz clock oscillator.

Because the AD9513 offers select integer divide ratios in the range of 1-32 on each clock channel, it is possible to derive the required frequencies by setting two of the dividers to DIV=4 and the third divider to DIV=10. Note that the AD9513 does not require a serial port for programming. By consulting the product datasheet, the user can set divide ratios, phase, delay and logic settings using the 4-level logic input pins S0-S10.

Each output may be programmed to either LVDS or CMOS levels. This example calls for CMOS clock outputs. Although not used in this example, there is a complementary CMOS output available on pins OUT0B, OUT1B, and OUT2B. These are available should a user need additional CMOS clocks 180 degrees out of phase with clocks on pins OUT0, OUT1 and OUT2.

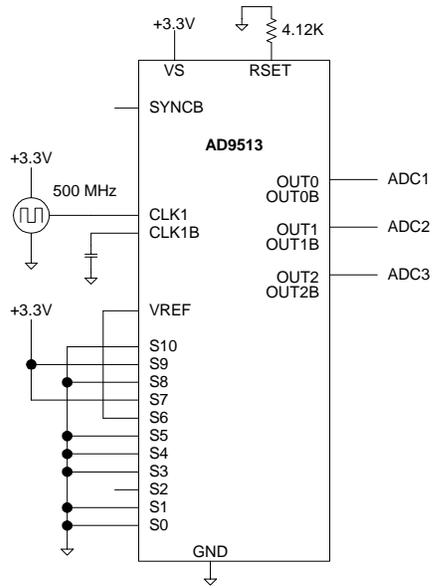
Note that ADIsimCLK allows the user to create custom input clocks. By starting with custom oscillators specified with high performance, the user can determine the jitter limitation of the AD9513 clock distribution section. This serves as a good baseline for seeing what performance is possible. The user can then change the phase noise performance of the input clock to see the impact on output clock phase noise and jitter.

The notes and diagrams below describe how to configure the AD9513 for this application. For instructions on how to navigate the ADIsimCLK page tabs and windows, please check the tutorial and help files available from the Help pulldown menu. For details on divide/phase/delay combinations available on the AD9513, please consult the product datasheet.

### NOTES

- 1) OUT0 LVDS/CMOS clock set to DIV=4, CMOS mode; OUT0B not connected
- 2) OUT1 LVDS/CMOS clock set to DIV=4, CMOS mode; OUT1B not connected
- 3) OUT2 LVDS/CMOS clock set to DIV=10, CMOS mode, optional fine delay bypassed; OUT2B not connected.
- 4) Input Clock is custom 500 MHz with PN floor at -160dBc/Hz

### CIRCUIT



### CIRCUITS REQUIRING CLOCKS

