TIMING CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UPDATED SPECIFICATION						
Data Output Transition Time DDR (CP) [1]	t_{15}	Positive clock edge to end of valid data	1.9			ns
Data Output Transition Time DDR (CP)[1]	t_{16}	Start of valid data to positive clock edge	1.7			ns
Data Output Transition Time DDR (CP)[1]	t_{17}	Negative clock edge to end of valid data	1.4			ns
Data Output Transition Time DDR (CP)[1]	t_{18}	Start of valid data to negative clock edge	1.7			ns
ORIGINAL SPECIFICATION						
Data Output Transition Time DDR (CP) [2]	t_{15}	Positive clock edge to end of valid data	−4 + TLLC/4			ns
Data Output Transition Time DDR (CP)[2]	t_{16}	Positive clock edge to start of valid data	0.25 + TLLC/4			ns
Data Output Transition Time DDR (CP)[2]	t_{17}	Negative clock edge to end of valid data	−2.95 + TLLC/4			ns
Data Output Transition Time DDR (CP)[2]	t_{18}	Negative clock edge to start of valid data	−0.5 + TLLC/4			ns

[1] Guaranteed by characterization up to 75MHz pixel clock.
[2] DDR timing specifications dependent on LLC output pixel clock; TLLC/4 = 9.25 ns at LLC = 27 MHz.