Product/Process Change Notice - PCN 11_0065 Rev. -

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Material Report). Any issues with this PCN or requirements to qualify the change (additional data or samples) must be sent to ADI within 30 days of publication date. ADI contact information is listed below.

PCN Title: AD9957 die change

Publication Date: 24-Mar-2011

Effectivity Date: 22-Jun-2011 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change

Multiple changes:

Die change 1: ESD cells improved

Die change 2: Latch up cells improved

Die change 3: Some of the digital logic was re-routed

Die change 4: REFCLK pass through altered

Spec change 1: CMOS Logic Input Max Current for both Logic 1 and Logic 0 increased to 150uA.

Spec change 2: CMOS Logic Input Typ Current for both Logic 1 and Logic 0 increased to 90uA.

Spec change 3: Full Sleep Mode Max Power increased to 40mW.

Reason For Change

Die change 1: Improve ESD sensitivity

Die change 2: Reduce likelihood of latch-up

Die change 3: Investigation in the lab and with state of the art digital design timing closure tools verified that multiple hold violations were occurring in the amplitude scale multiplier circuitry. This change fixes these problems.

Die change 4: When VCO iff off, but PLL in on, the REFCLK is passed through as an output

Spec changes: correcting errors from original release

Impact of the change (positive or negative) on fit, form, function & reliability

Die change 1: ESD damage is less likely to occur; (improvement).
Die change 2: Latch up is less likely; (improvement).
Die change 3: Prevents a configuration/state where the noise could be higher than expected or desired; (improvement).
Die change 4: Adds a function that was not present before, (improvement).

Spec change 1: CMOS Logic Input Max Current for both Logic 1 and Logic 0 increased to 150uA.

Spec change 2: CMOS Logic Input Typ Current for both Logic 1 and Logic 0 increased to 90uA.

Spec change 3: Higher power consumption in full power down mode

Product Identification *(this section will describe how to identify the changed material)*

All material dated after 1122 will be revised silicon.

There will be some early material of revised silicon available with date codes 1111 and 1112

Summary of Supporting Information

Qualification will be performed per ADI0012, Procedure for Qualification of New or Revised Processes. See attached Qualification Plan.

Supporting Documents

Attachment 1: Type: Qualification Plan Summary

ADI_PCN_11_0065_Rev_-_PCN AD9957_10_QUALIFICATION PLAN.doc

For questions on this PCN, send email to the regional contacts below or contact your local ADI sales representative					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models		
Added Parts On This Revision - Product Family / Model Number (3)		
AD9957 / AD9957/PCBZ	AD9957 / AD9957BSVZ	AD9957 / AD9957BSVZ-REEL

Appendix B - Revision History		
Rev	**Publish Date**	**Rev Description**
Rev. -	24-Mar-2011	Initial Release

Analog Devices, Inc. DocId:1491 Parent DocId:None Layout Rev:4