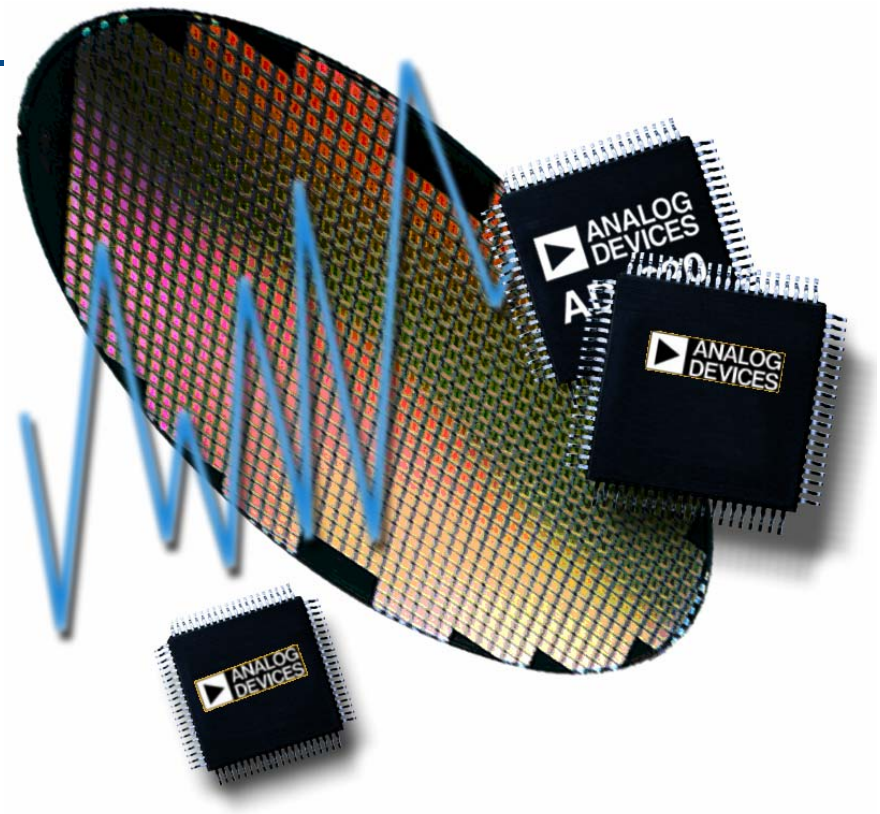

Reliability Report

Report Title: **ADLK 8” 0.6um CMOS Process Qualification**

Report Number: **4887**

Date: **18 June 2009**

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Introduction

This report details results of tests performed to qualify the ADI Limerick 8" 0.6um CMOS process. Four devices with different process variations were used for the qualification. These are the AD7344, AD7724, ADE7755A and ADG736. All four devices are previously qualified on the 6" CMOS process. There are no design changes between the 6" and 8" version. Qualification of these four devices will qualify the 8" 0.6um CMOS process.

Models covered by this qualification are:
AD5161, AD5162, AD5304, AD5305, AD5306, AD5307, AD5314, AD5315, AD5316, AD5317, AD5320, AD5324, AD5325, AD5326, AD5327, AD5338, AD5339, AD6480, AD7344, AD7476, AD7478, AD7724, AD7812, AD7814, AD7817, AD7866, AD7887, AD8551, AD8552, AD8554, AD8572, AD8574, AD9832, AD9835, ADE7751, ADE7755A, ADG3257, ADG3304, ADG701, ADG702, ADG704, ADG706, ADG711, ADG712, ADG713, ADG719, ADG721, ADG722, ADG723 ADG733, ADG734, ADG736, ADG741, ADG742, ADG749, ADG774, ADG774A, ADG779, ADG781, ADG782, ADG783, ADG784, ADG786, ADG787, ADG788, ADG822, ADG849, ADG884, ADV7123, ADV7125, ADV7127, SSM2211, and SST-6403.

Product Description

The AD7724 consists of two seventh order sigma-delta modulators. Each modulator converts its analog input signal into a high speed 1-bit data stream. The part operates from a 5 V power supply and accepts a differential input range of 0 V to +2.5 V or ±1.25 V centered about a common-mode bias.

The AD7344 is a GSM base station baseband transmit channel with auxiliary functions. The individual blocks are two 13MHz 12-bit DAC's with low pass filters on the outputs, a 13-bit timing DAC, a 10-bit power DAC, an 8-bit Ramp DAC 8 general purpose 8-bit DAC's, a 10-bit AD with an 8 channel multiplexer and 12 level shifters.

The ADE7755 is an accurate electrical energy measurement IC intended for use in two-wire distribution systems. It provides instantaneous and average real power based on line current and voltage. The part specifications surpass the accuracy requirements as quoted in the IEC1036 standard. The only analog circuitry used in the ADE7755 is in the ADC's and reference circuit. All the other signal processing (e.g., multiplication and filtering) is carried out in the digital domain.

The ADG736 is a CMOS Low Voltage 2.5Ω Dual SPDT Switch. It comprises of two independently selectable CMOS SPDT switches.

Device Characteristics

Part Number	AD7724	AD7344	ADG736	ADE7755A
Die Size (mm)	3.35 x 4.34	6.32 x 6.25	0.82 x 1.35	3.91 x 4.29
Wafer Fabrication Site	ADI- Limerick			
Wafer Fabrication Process	0.6um DPDM	0.6um DPDM CMOS	0.6um SPDM CMOS	0.6um DPTM
Transistor Count	3200	182000	108	43780
Maximum Power Dissipation (W)	0.60	0.500	0.002	0.18
Passivation Layer	Undoped-oxide/SiN			
Bond Pad Metal	AlCu			

Package/Assembly Characteristics

Available Packages	144-LQFP	48-LQFP	10-mSOIC	24-SSOP
Assembly Location	STATS	STATS	Carsem-M	Amkor-P
Package Die Attach	Ablestik 8361J	Ablestik 8361J	Ablestik 84-1LMIS R4	Ablestik 84-1LMIS R4
Leadframe Material	Copper	Copper	Copper	Copper
Package Bond Wire	Gold	Gold	Gold	Gold
Bond Wire Dia. (mils)	1.20	1.20	1.00	1.00
Package Molding Compound	Sumitomo 7372	Sumitomo 7372	Sumitomo 6600H	Sumitomo 6600H
Package Lead Finish	Tin / Lead Solder Plate	Tin / Lead Solder Plate	Tin / Lead Solder Plate	Tin / Lead Solder Plate
Package Moisture Sensitivity Level	3	3	1	1
Maximum Peak Reflow Temperature	240 +0/-5°C	260 +0/-5°C	260 +0/-5°C	260 +0/-5°C

Description/Results of Tests Performed

Table 1 provides a description of the qualification tests conducted and the associated test results. Tests and sample sizes are based on the ADI specification ADI0012, "Procedure for the Qualification of New or Revised Processes or Packages." All qualification devices were chosen from standard material manufactured through normal production processes and were electrically tested at room temperature following each endpoint. Any device that did not meet all electrical data sheet limits following stressing would be considered a failure. As Table 1 indicates no failures occurred during qualification.

Table 1. Qualification Results

Test Name	Conditions	Duration	Device	Package Type	Lot #	Sample Size	Qty. Rejects
Autoclave**	121C 100%RH 2atm	168hrs	ADG736	10-mSOIC	N29719.1	77	0
Autoclave*	121C 100%RH 2atm	168hrs	AD7344	144-LQFP	f157476.5	32	0
					f157480.5	35	0
					f157604.4	32	0
Autoclave**	121C 100%RH 2atm	168hrs	ADE7755A	24-SSOP	Q4887.1	45	0
					Q4887.7	45	0
					Q4887.13	45	0
Autoclave*	121C 100%RH 2atm	168hrs	AD7724	48-LQFP	f157478.9	50	0
					f157475.5	50	0
					f157479.9	50	0
Autoclave*	121C 100%RH 2atm	168hrs	ADMC300	80-LQFP	f123123.1	77	0
Burn-in	TJ = 125C	168hrs	ADG736	10-mSOIC	N24386.1 / .2	600	0
Burn-in	TJ = 125C	168hrs	AD7344	144-LQFP	f157476.10/12	501	0
					f157480.12	175	0
					F157480.11	195	0
					F157480.10	197	0
					F157604.9/10	206	0
					F157574.3/4/5	501	0
Burn-in	TJ = 125C	168hrs	ADE7755A	24-SSOP	Q4887.23	315	0
					Q4887.24	315	0
					Q4887.25	315	0
					Q4887.26	315	0
					Q4887.27	315	0
					Q4887.28	315	0
Burn-in	TJ = 125C	168hrs	AD7724	48-LQFP	f157478.4/5	659	0
					f157475.9/11	654	0
					f157479.5/6	660	0
High Temperature Operating Life	TJ = 150C	500hrs	ADG736	10-mSOIC	N24366.1	77	0
High	TJ = 125C	1000hrs		144-LQFP	f157476.9	31	0

Temperature Operating Life					f157480.9	32	0
					f157604.8	33	0
					f157476.13	26	0
					f157480.13	34	0
					f157573.9	32	0
					f157573.7	32	0
High Temperature Operating Life	TJ = 150C	500hrs	ADE7755A	24-SSOP	Q4887.3	82	0
					Q4887.9	82	0
					Q4887.15	82	0
High Temperature Operating Life	TJ = 135C	750hrs	AD7724	48-LQFP	f157478.6	50	0
					f157475.3	50	0
					f157479.3	50	0
High Temperature Operating Life	TJ=125C	1000hrs	ADMC300	80-LQF	f123123.1	77	0
High Temperature Storage	150C	1000hrs	ADG736	10-mSOIC	N29721.1	77	0
High Temperature Storage	150C	1000hrs	AD7344	144-LQFP	f157604.7	32	0
					f157476.8	35	0
					f157480.8	32	0
High Temperature Storage	150C	1000hrs	ADE7755A	24-SSOP	Q4887.4	45	0
					Q4887.10	45	0
					Q4887.16	45	0
High Temperature Storage	150C	1000hrs	AD7724	48-LQFP	f157478.11	45	0
					f157475.8	45	0
					f157479.11	45	0
Highly Accelerated Stress Test**	130C 85%RH 2atm, Biased	96hrs	ADG736	10-mSOIC	N29616.1	75	0
Highly Accelerated Stress Test*	130C 85%RH 2atm, Biased	96hrs	AD7344	144-LQFP	f157604.3	32	0
					f157476.4	34	0
					f157480.4	34	0
					f157573.8	35	0
					f157480.14	33	0
					f157476.14	24	0
					f157573.6	32	0
Highly Accelerated Stress Test**	130C 85%RH 2atm, Biased	96hrs	ADE7755A	24-SSOP	Q4887.2	45	0
					Q4887.8	45	0
					Q4887.14	45	0
Highly Accelerated Stress Test*	130C 85%RH 2atm, Biased	96hrs	AD7724	48-LQFP	f157479.10	45	0
					f157475.4	45	0
					f157478.10	45	0
Temperature Cycle**	-65C/+150C	500cycles	ADG736	10-mSOIC	N29720.1	77	0
Temperature Cycle*	-65C/+150C	500cycles	AD7344	144-LQFP	f157604.5	34	0
					f157476.6	33	0

					f157480.6	35	0
Temperature Cycle**	-65C/+150C	500cycles	ADE7755A	24-SSOP	Q4887.5	45	0
					Q4887.11	45	0
					Q4887.17	45	0
Temperature Cycle*	-65C/+150C	500cycles	AD7724	48-LQFP	f157475.7	45	0
					f157479.7	45	0
					f157478.7	45	0
Temperature Cycle*	-65C/+150C	500cycles	ADMC300	80-LQFP	f123123.1	77	0
Thermal Shock**	-65C/+150C	500cycles	ADG736	10-mSOIC	N29722.1	77	0
Thermal Shock*	-65C/+150C	500cycles	AD7344	144-LQFP	f157480.7	32	0
					f157604.6	35	0
					f157476.7	25	0
Thermal Shock**	-65C/+150C	500cycles	ADE7755A	24-SSOP	Q4887.6	45	0
					Q4887.12	45	0
					Q4887.18	45	0
Thermal Shock*	-65C/+150C	500cycles	AD7724	48-LQFP	f157478.8	50	0
					f157475.6	50	0
					f157479.8	50	0

Noted samples (*) were subjected to preconditioning (per J-STD-020B Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 192 hrs @ 30°C, 60%RH
- Reflow: 3 passes through a convection/IR oven with a peak temperature of 240 +0/-5°C for a minimum of 10 seconds.

Noted samples (**) were subjected to preconditioning (per J-STD-020B Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH
- Reflow: 3 passes through a convection/IR oven with a peak temperature of 240 +0/-5°C for a minimum of 10 seconds.

ESD Testing Results

The results of ESD testing are summarized in Table 2. As accept/reject criteria, all samples were electrically tested to data sheet limits before and after ESD stressing.

Human Body Model (HBM) ESD Sensitivity Classification testing was conducted using a KeyTek Verifier V3 Test System. During HBM testing of a given sample, one positive and one negative discharge was applied to each of the following pin combinations:

(1) Every individual pin to each power supply pin.
(2) Every individual pin to each Gnd. pin
(3) Every individual I/O pin to the group of all other I/O pins.

Field-Induced (Robotic) Charged Device Model (FICDM) ESD Sensitivity Classification testing was conducted using a Verifier Robotic Test System. During FICDM testing of a given sample, the device package was charged via a field plate and a discharge pin made contact with each individual device pin to discharge it through a 1Ω resistor to ground. Three positive and three negative discharges were applied to every pin.

Table 2. ESD Characterization Results*

ESD Model		Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	ADE7755A	24-SSOP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	500V	1000V	C4
FICDM	AD7724	48-LQFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	250V	500V	C3
FICDM	AD7344	144-LQFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	250V	500V	C3
FICDM	SSM2211	8-SOIC	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	2000V	C6
FICDM	AD6480	52-LQFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	250V	NA	C3
FICDM	SST6403	100-MQFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	250V	NA	C3
FICDM	AD8554	14-SOICN	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	NA	C6
FICDM	AD8551	8-SOIC-N	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1000V	1500V	C5
FICDM	AD7887	8-SOIC-N	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	500V	1000V	C4
FICDM	ADMC300	80-QFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	250V	500V	C3
FICDM	ADG786	20-LFCSP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	2000V	C6
HBM	AD7344	144-LQFP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	1500V	NA	1C
HBM	ADE7755A	24-SSOP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	1500V	2000V	1C
HBM	AD7724	48-LQFP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	4000V	NA	3A
HBM	SSM2211	8-SOIC	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	1500V	2000V	1C

HBM	AD6480	52-LQFP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	1500V	NA	1C
HBM	SST-6403	100-MQFP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	1000V	NA	1C
HBM	AD8554	14-SOICN	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	2000V	NA	2
HBM	AD8551	8-SOIC-N	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	2500V	3000V	2
HBM	AD7887	8-SOIC-N	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	4000V	NA	3A
HBM	ADMC300	80-QFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	2500V	3000V	2
HBM	ADG786	20-LFCSP	ESD Assoc. STM5.5.1-2001	1Ω, Cpkg	1000V	1500V	1C
MM	ADE7755A	24-SSOP	ESD Assoc. STM5.2-1999	0Ω, 200pF	100V	200V	M2
MM	AD8554	14-SOICN	ESD Assoc. STM5.2-1999	0Ω, 200pF	100V	NA	M2

*ADI measures ESD results using stringent test procedures based on the specifications listed in the above table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/corporate/quality/manuals/.

Latch-Up and Electrical Overstress Testing Results

The AD7724, AD7344 and ADE7755A were tested for Class I, Level A, static latch-up conditions using the test method outlined in JEDEC Standard Number 78. The result summary is shown below:

- No latch-up occurred during testing of each individual input and output pin in which both positive and negative current pulses (50µs risetime, 5ms duration) were applied up to Inorm This input and output latch-up testing was conducted initially with all input pins at Vin minimum levels, and subsequently with all input pins at Vin maximum levels.
- No latch-up occurred during testing of the supply pin groups in which voltage pulses (50µs risetime, 5ms duration) were applied up to VDD. This overvoltage latch-up testing was conducted initially with all input pins at Vin minimum levels, and subsequently with all input pins at Vin maximum levels.

Device	Inorm
AD7724	+160mA/-160mA
AD7344	+170mA/-170mA
ADE7755A	+102mA/-80mA
AD8554	+110mA/-101mA
SST6403	+125mA/-101mA

The six devices that were subjected to the latch-up test criteria all passed post-latch-up electrical testing.

Conclusion

The qualification of the ADI Limerick 8" 0.6um CMOS process has been successfully completed for production release.

Approvals

Reliability Engineer: Thomas McHugh
This report has been approved by electronic means (1.8).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page: http://www.analog.com
Sales Info: http://www.analog.com/world/corp_fin/sales_directory/distrib.html
Reliability Data: http://www.analog.com/corporate/quality/read/1stpage.html
Reliability Handbook: http://www.analog.com/corporate/quality/manuals/