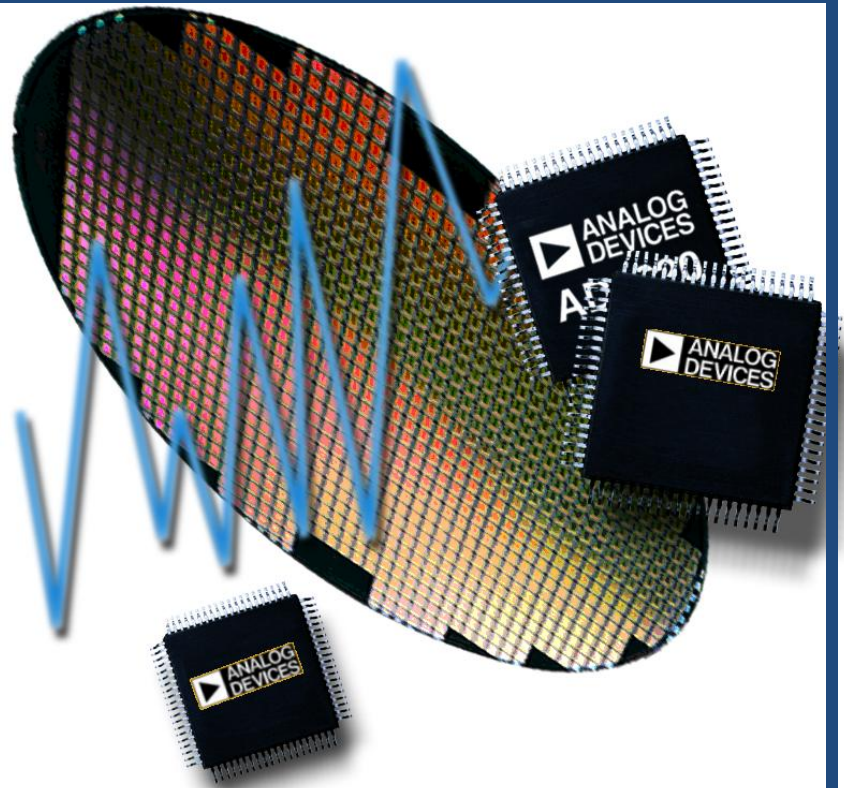

Reliability Report

Report Title: AD8542 Die Revision (Zc) and Assembly Site Change

Report Number: 8860

Revision: A

Date: 28 January 2011

Summary

This report documents the successful completion of the reliability qualification requirements for release of the AD8542 product (die revision, Zc) in an 8-MINI_SO and an 8-SOIC_N halide free package. The AD8542 is a dual rail-to-rail input and output, single-supply amplifier featuring very low supply current and 1 MHz bandwidth.

Table 1: AD8542 Product Characteristics

Die/Fab

Die ID	6416z
Die Size (mm)	0.99 x 1.03
Wafer Fabrication Site	TSMC Fab-9
Wafer Fabrication Process	0.6µm CMOS
Transistor Count	99
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Die Overcoat	Polyimide

Package/Assembly

Available Package	8-MINI_SO	8-SOIC_N
Body Size (mm)	3.00 x 3.00 x 0.85	3.90 x 4.90 x 1.55
Lead Pitch (mm)	0.65	1.27
Assembly Location	ASE-Shanghai	ASE-Shanghai
Molding Compound	Hitachi CEL9240HF10AK	Hitachi CEL9240HF10AK
Wire Type	Gold Tanaka GPG-2	Gold Tanaka GPG-2
Wire Diameter (mils)	0.80	0.80
Die Attach	Hitachi EN-4900GC	Hitachi EN-4900GC
Lead Frame Material	Copper	Copper
Lead Finish	Matte Sn	Matte Sn
Moisture Sensitivity Level	1	1
Maximum Peak Reflow Temperature (°C)	260	260

Description / Results of Tests Performed

Tables 2, 3 and 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: MINI_SO at ASE-Shanghai Package Qualification Test Results

Test Name	Spec	Conditions	Device	Lot #	Sample Size	Qty. Failures
Autoclave (AC)[1]	JESD22-A102	121°C, 100%RH, 2atm, 96 hours	AD8131	Q7514.100	77	0
				Q7514.101	77	0
				Q7514.102	77	0
			OP777	Q8520.100	77	0
				Q8520.101	77	0
				Q8520.102	77	0
Highly Accelerated Temperature and Humidity Stress (HAST)[1]	JESD22-A110	130°C, 85%RH, 2atm, Biased, 96 hours	AD8131	Q7514.200	77	0
				Q7514.201	77	0
				Q7514.202	77	0
			OP777	Q8520.200	77	0
				Q8520.201	77	0
				Q8520.202	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1000 hours	AD8131	Q7514.300	77	0
			OP777	Q8520.300	77	0
		150°C, 500 hours	AD8617	Q9114.6	77	0
Solder Heat Resistance (SHR)[1]	ADI-0049	See Footer[1]	AD8542	Q8860.SH1	30	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C, 500 cycles	AD8131	Q7514.500	77	0
				Q7514.501	77	0
				Q7514.502	77	0
			AD8617	Q9114.5	77	0
			OP777	Q8520.500	77	0
				Q8520.501	77	0
				Q8520.502	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Table 3: SOIC_N at ASE-Shanghai Package Qualification Test Results

Test Name	Spec	Conditions	Device	Lot #	Sample Size	Qty. Failures
Autoclave (AC)[1]	JESD22-A102	121°C, 100%RH, 2atm, 96 hours	AD8009	Q8964.PC1	77	0
			ADA4665-2	Q8663.100	77	0
				Q8663.101	77	0
				Q8663.102	77	0
			OP27	Q8965.PC2	77	0
				Q8965.PC3	77	0
			OP282	Q8289.100	77	0
				Q8289.101	77	0
				Q8289.102	77	0
Highly Accelerated Temperature and Humidity Stress (HAST)[1]	JESD22-A110	130°C, 85%RH, 2atm, Biased, 96 hours	AD8091	Q7512.200	77	0
				Q7512.201	77	0
				Q7512.202	77	0
			ADA4665-2	Q8663.200	77	0
				Q8663.201	77	0
				Q8663.202	77	0
			OP282	Q8289.200	77	0
				Q8289.201	77	0
				Q8289.202	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1000 hours	AD8091	Q7512.300	77	0
			ADA4665-2	Q8663.300	77	0
			OP282	Q8289.300	77	0
Solder Heat Resistance (SHR)[1]	ADI-0049	See Footer[1]	AD8542	Q8860.SH3	30	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C, 500 cycles	ADA4665-2	Q8663.500	77	0
				Q8663.501	77	0
				Q8663.502	77	0
			OP282	Q8289.500	77	0
				Q8289.501	77	0
				Q8289.502	77	0
				Q8519.200	77	0
				Q8519.201	77	0
				Q8519.202	77	0
				Q8519.203	77	0
				Q8519.204	77	0
				Q8519.205	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Table 4: 0.6µm CMOS at TSMC Fab-9 Fab Qualification Test Results

Test Name	Spec	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, Method 1015	125°C, 48 hours	AD8628	Q8479.82	240	0
				Q8479.83	240	0
				Q8479.84	240	0
				Q8479.85	240	0
				Q8479.86	240	0
				Q8479.87	240	0
				Q8479.88	240	0
				Q8479.89	240	0
				Q8479.90	90	0
Highly Accelerated Temperature and Humidity Stress (HAST)	JESD22-A110	130°C, 85%RH, 2atm, Biased, 96 hours	AD7873	Q7321.6	77	0
				Q7321.4	77	0
Highly Accelerated Temperature and Humidity Stress (HAST)[1]			AD8630	Q7954.13	77	0
				Q7954.14	77	0
				Q7954.15	77	0
			AD8648	Q7588.5	77	0
				Q7588.6	77	0
			ADA4692-2	Q7559.4	77	0
			ADA4692-2	Q7559.13	77	0
			ADA4692-2	Q7559.5	77	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C ‹ Tj ‹ 135°C, Biased, 1000 hours	AD8601	Q7454.5	77	0
				Q7454.6	77	0
				Q7454.7	77	0
			AD7873	Q7321.9	77	0
				Q7321.7	77	0
		150°C ‹ Tj ‹ 175°C, Biased, 500 hours	ADA4505-2	Q8001.1	77	0
				Q8001.6	77	0
High Temperature Operating Life (HTOL)[1]		125°C ‹ Tj ‹ 135°C, Biased, 1000 hours	AD8648	Q7588.8	77	0
				Q7588.7	77	0
		150°C ‹ Tj ‹ 175°C, Biased, 500 hours	AD8601	Q8322.5	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1000 hours	AD8506	Q8001.7	77	0
			AD8515	Q8134.7	45	0
			AD8601	Q8277.10	65	0
			AD8606	Q8042.202	77	0
			AD8629	Q7892.3	45	0
			AD8630	Q7954.8	45	0
			AD8692	Q7248.12	77	0
				Q7248.13	77	0
			AD8692	Q7248.14	77	0
			ADA4692-2	Q7559.6	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field Induced Charged Device Model (FICDM) ESD testing are summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at the Analog Devices' web site).

Table 4: AD8542 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	8-MINI_SO	JESD22-C101	1Ω, Cpkg	±1500V	NA	IV
	8-SOIC_N			±1500V	NA	IV
HBM	8-SOIC_N	ANSI/ESDA/JEDEC JS-001-2010	1.5kΩ, 100pF	±2000V	±2500V	2

Latch-Up Test Results

Six samples of the AD8542 were Latch-up tested at T_A=25°C per JEDEC Standard JESD78, Class I, Level A. All six devices passed.

Approvals

Reliability Engineer: Li Li Tay
This report has been approved by electronic means (5.0).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site.