

Report Title:	ADG467 redesign
Report Number:	7756
Revision:	В
Date:	16 December 2009



Summary

This report documents the successful completion of the reliability qualification requirements for release of the ADG467 product in a 18-SOIC_W, 20-SSOP package. The ADG467 is an octal channel protector. The channel protector will protect sensitive components from voltage transients in the signal path whether or not the power supplies are present.

Table 1: ADG467 Product Characteristics

Die/Fab	
Device / Die ID	A563A
Die Size (mm)	2.11 x 2.64
Wafer Fabrication Site	Limerick 8"
Wafer Fabrication Process	HVCMOS
Passivation Layer	undoped-oxide/OxyNitride
Bond Pad Metal Composition	AlCu

Package/Assembly

Available Package	20-SSOP
Body Size (mm)	7.50 x 5.30 x 1.80
Assembly Location	Carsem-M
Molding Compound	Sumitomo 6600HR
Wire Type	Gold Tanaka M3
Wire Diameter (mils)	1.00
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260 +0/-5C

Table 2: ADG467 Product Characteristics

Die/Fab	
Device / Die ID	A564A
Die Size (mm)	2.11 x 2.64
Wafer Fabrication Site	Limerick 8"
Wafer Fabrication Process	HVCMOS
Passivation Layer	undoped-oxide/OxyNitride
Bond Pad Metal Composition	AlCu

Package/Assembly

Available Package	18-SOIC_W



Body Size (mm)	11.55 x 7.50 x 1.50
Assembly Location	Amkor-P
Molding Compound	Sumitomo 6600H
Wire Type	Gold
Wire Diameter (mils)	1.20
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260C +0/-5C



Description / Results of Tests Performed

Tables 3 and 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Tables 1, and 2. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Test Name	Spec	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
Autoclave (AC) ²	JESD22- A102	121°C 100%RH	ADM207	Carsem-M 24-SSOP	O69361.1	45	0
		2atm 168 hours	ADM211	Carsem-M 28-SSOP	R86123.1	45	0
Autoclave (AC) ²	JESD22- A102	121°C 100%RH 2atm 96 hours	ADM691	Amkor-P 16-SOIC_W	Q7874.151 Q8060.155	45 45	0
	JESD22-	121°C	ADM211E	Carsem-M	N49605.1	45	0
(AC)	ATOZ	2atm 168		20-330F	091642 1	45 45	0
		hours	ADIVIZ 13		R86325 1	45	0
			ADM213F		040250.1	45	0
Autoclave (AC) ²	JESD22- A102	121°C 100%RH	AD7398- POLY	Amkor-P 16-SOIC W	AC47097.1	77	0
		2atm 96	ADM691	1 –	Q7498.311	45	0
		hours	DAC10	Amkor-P 18-SOIC_W	E195710.1	45	0
			ADE7751	Carsem-M	AB60919.1	45	0
			ADE7755	24-SSOP	AA89084.1	45	0
Autoclave (AC) ²	JESD22- A102	121°C 100%RH 2atm 96 hours	AD7834	Amkor-P 28-SOIC_W	Q7732.4	77	0
Autoclave (AC) ²	JESD22- A102	121°C 100%RH 2atm 96 hours	ADE7758	Amkor-P 24-SOIC_W	AC79285.1	45	0
Autoclave	JESD22-	121°C	ADE7758	Amkor-P	AB21716.1	45	0
(AC) ²	A102	100%RH 2atm 96 hours		24-SOIC_W	AB55241.1	45	0
Biased HAST (HAST) ²	JESD22- A110	130°C 85%RH 2atm, Biased 96 hours	ADE7755	Carsem-S 24-SSOP	Q4521.17	45	0
Biased	JESD22-	130°C	AD1895A	Carsem-S	Q6604.16	77	0
HAST	A110	85%RH		28-SSOP	Q6604.17	77	0
(HAST) ²		2atm,	ADM691	Amkor-P	Q8060.159	45	0
		Blased 96		16-SOIC_W	Q8276.203	45	0
		nours	ADE7753	Carsem-S 20-SSOP	Q8060.36	45	0

Table 3: Package Qualification Test Results



Test Name	Spec	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
			ADE7751	Carsem-S 24-SSOP	Q7874.9	45	0
Biased	JESD22-	110°C	AD1896A	Carsem-S	Q6605.3	77	0
HAST (HAST) ²	A110	85%RH 2atm, Biased 96 hours		28-SSOP	Q6605.4	77	0
Biased HAST (HAST) ²	JESD22- A110	130°C 85%RH 2atm, Biased 96 hours	ADM691	Amkor-P 16-SOIC_W	O91640.1	45	0
Biased HAST	JESD22- A110	130°C 85%RH	ADM691	Amkor-P 16-SOIC_W	Q7498.312	45	0
(HAST) ²		2atm, Biased 96	AD7707	Amkor-P 20-SOIC W	AB60669.1	45	0
		hours	ADE7751	Carsem-M	AB60920.1	45	0
			ADE7755	24-SSOP	AA89085.1	45	0
				Carsem-S 24-SSOP	Q7498.352	45	0
Biased	JESD22-	130°C	AD7874	Amkor-P	AA88883.1	45	0
HAST	A110	85%RH		28-SOIC_W	R86164.1	45	0
(HAST) ¹		2atm, Biased 96 hours			R86267.1	45	0
High	JESD22-	150°C	ADG467	Carsem-M	Q7756.17	77	0
Temperature	A103	1,000 hours		20-SSOP	Q7756.18	77	0
Storage Life					Q7756.19	77	0
(HTSL)			AD7398- POLY	Amkor-P 16-SOIC_W	AC47176.1	77	0
			ADE7755	Carsem-S	Q4521.19	45	0
				24-SSOP	Q4521.21	45	0
					Q4521.5	45	0
			AD1895A	Carsem-S	Q6604.11	77	0
			AD974	28-SSOP	AC76443.1	77	0
Solder Heat Resistance (SHR) ²	ADI-0049	See Footer	ADM211	Carsem-M 28-SSOP	R86126.1	10	0
Solder Heat Resistance (SHR) ²	ADI-0049	See Footer	ADM691	Amkor-P 16-SOIC_W	Q7874.154	15	0
Solder Heat Resistance (SHR) ²	ADI-0049	See Footer	ADM213	Carsem-M 28-SSOP	R86380.1	10	0
Solder Heat Resistance	ADI-0049	See Footer	AD7398- POLY	Amkor-P 16-SOIC_W	AC47178.1	11	0
(SHR) ²			DAC10	Amkor-P 18-SOIC_W	E195709.1	15	0
			ADE7751	Carsem-M	AB60922.1	15	0
			ADE7755	24-SSOP	AA89062.1	15	0
			ADM691	Amkor-P 16-SOIC W	Q7498.315	15	0
Temperature Cycling	JESD22- A104	-65°C / +150°C 500	ADM207	Carsem-M 24-SSOP	O69363.1	45	0
(TC) ²		cycles	ADM211	Carsem-M 28-SSOP	R86125.1	45	0
Temperature	JESD22-	-65°C /	ADM691	Amkor-P	Q7874.153	45	0
Cycling (TC) ²	A104	+150°C 500 cycles		16-SOIC_W	Q8060.157	45	0
Temperature	JESD22-	-65°C /	ADM211E	Carsem-M	N49607.1	45	0
Cycling	A104	+150°C 500		28-SSOP	N91507.1	45	0



Test Name	Spec	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
$(TC)^2$		cycles	ADM213		O91644.1	45	0
					R86327.1	45	0
			ADM213E		O40252.1	45	0
Temperature Cycling	JESD22- A104	-65°C / +150°C 500	ADM691	Amkor-P 16-SOIC W	Q7498.313	45	0
$(TC)^2$		cycles	DAC10	Amkor-P	E195711.1	45	0
		-		18-SOIC_W	E83002.1	45	0
			ADE7751	Carsem-M	AB60921.1	45	0
			ADE7755	24-SSOP	AA89086.1	45	0
Temperature Cycling (TC) ¹	JESD22- A104	-65°C / +150°C 500 cycles	AD7834	Amkor-P 28-SOIC_W	Q7732.8	77	0
Temperature Cycling (TC) ¹	JESD22- A104	-65°C / +150°C 500 cycles	ADE7758	Amkor-P 24-SOIC_W	AC79286.1	45	0
Temperature	JESD22-	-65°C /	ADE7758	Amkor-P	AB21717.1	45	0
Cycling (TC) ¹	A104	+150°C 500 cycles		24-SOIC_W	AB55242.1	45	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Soak: Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

2) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Soak: Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Test Name	Spec	Conditions	Device	Fab Process	Lot #	Sample Size	Qty. Failures
					Q7756.100	290	0
					Q7756.101	290	0
					Q7756.102	50	0
Early Life	IVIIL-STD-	125°C 49		Limoriak 9"	Q7756.201	290	0
Failure Rate	oos, Method	125 C 40	ADG467	BICMOS	Q7756.200	290	0
(ELFR)	1015	nours		BICIVIOS	Q7756.202	52	0
	1015				Q7756.300	290	0
					Q7756.301	290	0
					Q7756.302	40	0
	JESD22- A108	Ta=125°C, Biased 1,000 hours	ADG467	Limerick 8" BiCMOS	Q7756.2	45*	0
High					Q7756.3	45*	0
Temperature					Q7756.4	45*	0
Operating					Q7756.6	77	0
Life (HTOL) ¹					Q7756.5	77	0
					Q7756.7	77	0
High					Q7756.17	77	0
Temperature	JESD22-	150°C	406467	Limerick 8"	Q7756.18	77	0
Storage Life (HTSL)	A103	1,000 hours	ADG407	BiCMOS	Q7756.19	77	0

Table 4: Fab Qualification Test Results

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Soak: Unbiased Soak: 168 hrs @ 85°C, 85% RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

* Stressed to Fault condition. +55V, -40V on the drain of the Switch.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional gualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) ESD testing is summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at the Analog Devices Website (Analog Website).

Table 6: ESD Test Results								
ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class		
HBM	20-SSOP	ANSI/ESD STM5.1- 2007	1.5kΩ, 100pF	±300V	NA	1A		

Table C. CCD Test Desults

Latch-Up Test Results

Six samples of the ADG467 were Latch-up tested at Ta=25°C per JEDEC Standard JESD78, Class I, Level A. All six devices passed.

Approvals

This report has been approved by electronic means (4.0). Reliability Engineer: John Browne

Additional Information

Data sheets and other additional information are available on Analog Devices' web site