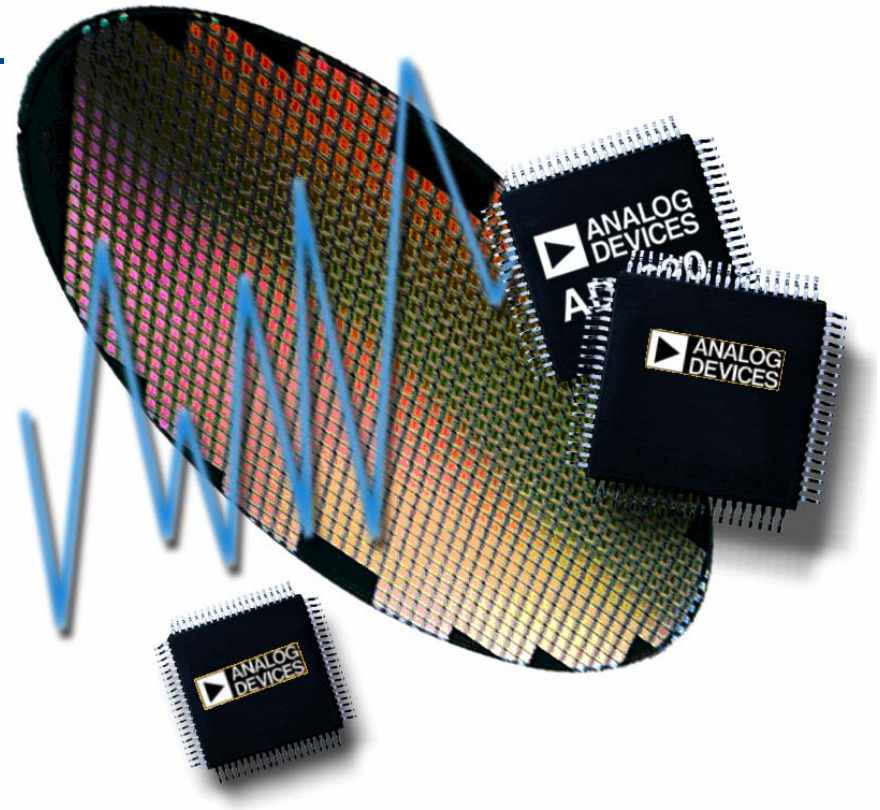

Reliability Report

Report Title: CBCMOS2 Wafer Transfer

Report Number: 5786

Date: 26 January 2007

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Summary

This CBCMOS2E Wafer Fab Process in Wilmington, Massachusetts was initially successfully qualified in July 2005 as detailed in Reliability Report 4518. This report documents the work for additional reliability qualification requirements for release of the CBCMOS2 Wafer Fab Process in Wilmington. The AD8202 and OP291 products in an 8-SOICnb package were chosen as qualification vehicles for the process qualification.

CBCMOS 2 is a 12V complementary CMOS and Bipolar process. It features double level poly and metal, as well as a Power 2E option. The basic CBCMOS 2 process has 19 masking levels. Power 2E has P+ Buried layer and P+ Sinker layers added to provide low dropout PNP transistors. Both processes use N <100> substrates and N epi. CBCMOS 2E also features trimmable 1.9 kOhms/sq. SiCr resistors.

Table 1. Product Characteristics

Device	**AD8202**	**OP291**
Maximum Power Dissipation (W)	.012	.003
Device / Die ID	AD8202	5546Y/A
Die Size (mm)	1.18 x 1.16	1.78 x 1.78
Wafer Fabrication Site	ADI-Wilmington	ADI-Wilmington
Wafer Fabrication Process	3um BiMOS DPDM	3um BiMOS DPDM
Transistor Count	53	146
Passivation Layer	doped-oxide/SiN	doped-oxide/SiN
Bond Pad Metal Composition	AlCu	AlCu
Polyimide Layer	Polyimide	Polyimide
Package/Assembly		
Available Package(s)	8-SOICnb	8-SOICnb
Body Size (mm)	4.00 x 5.00 x 1.50	4.00 x 5.00 x 1.50
Assembly Location	Amkor-P	Amkor-P
Die Attach	Ablestik 84-1LMIS R4	Ablestik 84-1LMIS R4
Lead Frame Material	Copper	Copper
Bond Wire Type	Gold	Gold
Bond Wire Dia. (mils)	1.20	1.20
Mold Compound	Sumitomo 6600H	Sumitomo 6600H
Lead Frame Finish	Tin Plate	Tin Plate
Die Overcoat	Polyimide	Polyimide
Moisture Sensitivity Level	MSL 1	MSL 1
Maximum Peak Reflow	260^{o}C	260^{o}C

Description/Results of Tests Performed

Table 2 and 3 provides a description of the qualification tests conducted and the associated test results on the AD8202 and OP291.

Table 2. Reliability Assembly Qualification Test Results

Test Name	Conditions	Specification	Part Number	Package	Lot Number	Sample Size	Qty. Rejects
Autoclave[1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	OP291	8-SOICnb	R31684.1	77	0
					R31685.1	77	0
					R31686.1	77	0
Autoclave[1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD8202	8-SOICnb	Q5481.1	77	0
					Q5481.8	77	0
					Q5481.9	77	0
High Temperature Storage	150C 1000hrs	JEDEC-STD-22, Method A103	AD8202	8-SOICnb	Q5481.2	77	0
			OP291	8-SOICnb	R31690.1	77	0
Solder Heat Resistance[1]	See Below	ADI-0049	AD8202	8-SOICnb	Q5481.3	11	0
					Q5481.14	11	0
					Q5481.15	11	0
			OP291	8-SOICnb	R31691.1	11	0
					R31692.1	11	0
					R31693.1	11	0
Temperature Cycle[1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	OP291	8-SOICnb	R31694.1	77	0
					R31695.1	77	0
					R31696.1	77	0
Temperature Cycle[1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	AD8202	8-SOICnb	Q5481.4	77	0
					Q5481.16	77	0
					Q5481.17	77	0
Thermal Shock[1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A106	OP291	8-SOICnb	R31697.1	77	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260+0/-5°C for a minimum of 10 seconds.

Table 3. Reliability Process Qualification Test Results

Test Name	Conditions	Specification	Part Number	Fab Process	Lot Number	Sample Size	Qty. Rejects
E/T Induced Gate Leakage	+/-400V @ 155C Single Duration	AEC-Q100-006	AD8202	3um BiMOS DPDM	Q5481.5	6	0
			OP291	3um BiMOS DPDM	Q5786.4	6	0
Early Life Failure	TJ = NAC 48hrs	MIL-STD-883, Method 1015	AD8202	3um BiMOS DPDM	Q5481.20	192	0
					Q5481.21	192	0
					Q5481.22	192	0
					Q5481.23	192	0
					Q5481.24	192	0
					Q5481.25	192	0
					Q5481.26	192	0
					Q5481.27	192	0
					Q5481.28	192	0
					Q5481.29	192	0
					Q5481.30	192	0
					Q5481.31	192	0
					Q5481.32	192	0
					Q5481.33	192	0
					Q5481.34	192	0
			OP291	3um BiMOS DPDM	R31746.1	400	0
					R31746.2	400	0
					R34367.1	400	0
					R34367.2	400	0
					R42761.1	400	0
					R42761.2	400	0
High Temperature Operating Life	TJ = NAC 1000hrs	JESD22-A108	AD8202	3um BiMOS DPDM	Q5481.6	77	0
					Q5481.10	77	0
					Q5481.11	77	0
			OP291	3um BiMOS DPDM	R45465.1	77	0
					R45466.1	77	0
					R45467.1	77	0
Highly Accelerated Stress Test	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	OP291	3um BiMOS DPDM	R31687.1	77	0
					R31688.1	77	0
					R31689.1	77	0
Temperature Humidity Bias[1]	85C 85%RH, Biased 1000hrs	JEDEC-STD-22, Method A101	AD8202	3um BiMOS DPDM	Q5481.7	77	0
					Q5481.18	77	0
					Q5481.19	77	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH

- Reflow: 3 passes through an oven with a peak temperature of 260+0/-5°C for a minimum of 10 seconds.

ESD Testing

The results of Human Body Model (HBM), Machine Model (MM), and Field Induced Charge Device Model (FICDM) ESD testing are summarized in Table 4.
ADI measures ESD results using stringent test procedures based on the specifications listed in the above table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/corporate/quality/manuals/.

Table 4. AD8202 and OP291 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Part	Highest Pass Level	First Fail Level	Class
FICDM	8-SOICnb	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	AD8202	1000V	1500V	C4
				OP291	1500V	NA	C6
HBM	8-SOICnb	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	AD8202	2000V	2500V	Class 2
				OP291	3000V	3500V	Class 2
MM	8-SOICnb	ESD Assoc. STM5.2-1999	0Ω, 200pF	AD8202	200V	400V	M3
				OP291	200V	400V	M3

Latch-up Testing

Six samples of the AD8202 and OP291 passed Latch-up testing at Ta=105°C per JEDEC Standard JESD78, Class I, Level A.

Approvals

Reliability Engineer: Denis Belisle
This report has been approved by electronic means (3.0).