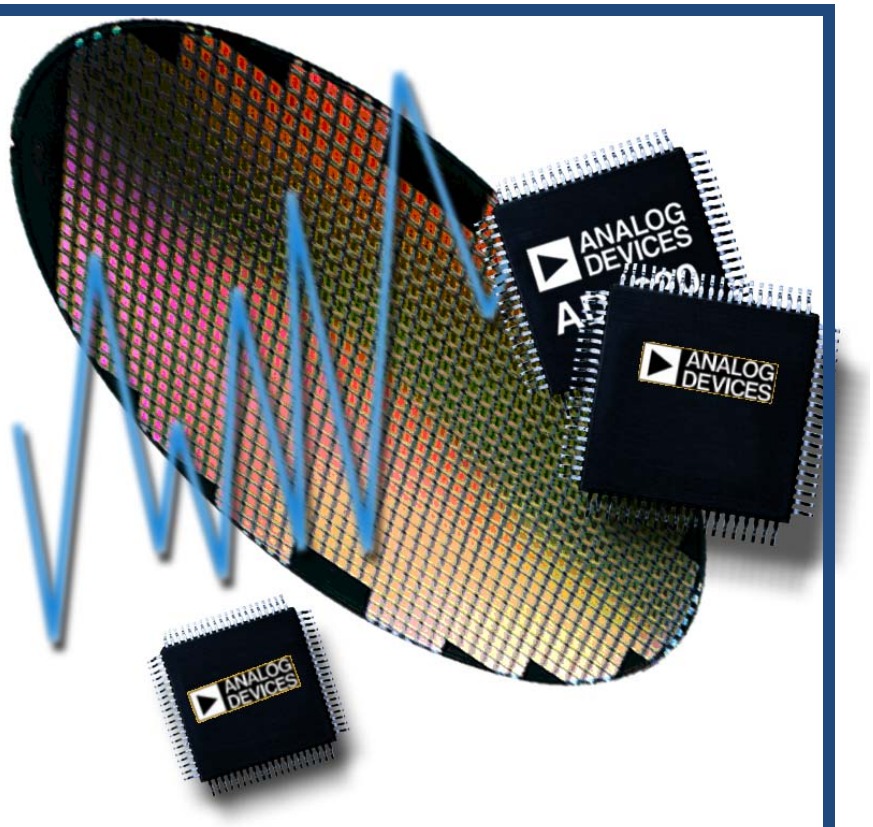

Reliability Report

Report Title: AD7810/11/12/23 Transfer to TSMC

Report Number: 7976

Revision: B

Date: 21 December 2009

Summary

This report documents the successful completion of the reliability qualification requirements for release of the AD7810, AD7823, AD7811 and AD7812 product in a 8-miniSOIC, 16-SOIC_N, 8-SOIC_N and 20-SOIC_W package. The AD7810, AD7823, AD7811 and AD7812 are high speed, low power, 10-bit A/D converter, high speed, low power, converters.

Table 1: AD7812 Product Characteristics

Die/Fab

Device / Die ID	G042B
Die Size (mm)	2.04 x 2.19
Wafer Fabrication Site	TSMC 2A 6"
Wafer Fabrication Process	0.60um DPDM CMOS
Transistor Count	5 thousand
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Maximum Current Density (mA/µm)	0.12

Package/Assembly

Available Package	20-SOIC_W
Body Size (mm)	13.00 x 7.60 x 2.35
Assembly Location	Amkor-P
Molding Compound	Sumitomo 6600H
Wire Type	Gold
Wire Diameter (mils)	1.20
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Table 2: AD7811 Product Characteristics

Die/Fab

Device / Die ID	G0412B
Die Size (mm)	2.04 x 2.19
Wafer Fabrication Site	TSMC 2A 6"
Wafer Fabrication Process	0.60um DPDM CMOS
Transistor Count	5 thousand
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Maximum Current Density (mA/µm)	0.12

Package/Assembly

Available Package	16-SOIC_N
Body Size (mm)	10.00 x 4.00 x 1.75
Assembly Location	Carsem-M
Molding Compound	Sumitomo 6600H
Wire Type	Gold Tanaka M3
Wire Diameter (mils)	1.20
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Table 3: AD7810 Product Characteristics

Die/Fab

Device / Die ID	G05B
Die Size (mm)	1.42 x 2.06
Wafer Fabrication Site	TSMC 2A 6"
Wafer Fabrication Process	0.60um DPDM CMOS
Transistor Count	2889
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Maximum Current Density (mA/µm)	0.13

Package/Assembly

Available Package	8-MINI_SOIC
Body Size (mm)	3.00 x 3.00 x 1.00
Assembly Location	Carsem-M
Molding Compound	Sumitomo 6600
Wire Type	Gold Tanaka M3
Wire Diameter (mils)	1.00
Die Attach	Ablestik 84-1LMI
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Table 4: AD7823 Product Characteristics

Die/Fab

Device / Die ID	G051B
Die Size (mm)	1.42 x 2.06
Wafer Fabrication Site	TSMC 2A 6"
Wafer Fabrication Process	0.60um DPDM CMOS
Transistor Count	2889
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Maximum Current Density (mA/µm)	0.13

Package/Assembly

Available Package	8-SOIC_N
Body Size (mm)	5.00 x 4.00 x 1.75
Assembly Location	Carsem-M
Molding Compound	Sumitomo 6600H
Wire Type	Gold Tanaka M3
Wire Diameter (mils)	1.30
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 5 and 6 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Tables 1, 2, 3 and 4. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 5: Package Qualification Test Results

Test Name	Spec	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
Autoclave (AC)	JESD22-A102	121°C 100%RH 2atm 168 hours	ADM202E	Carsem-M 16-SOIC_N	R86152.1	45	0
Autoclave (AC)[1]	JESD22-A102	121°C 100%RH 2atm 96 hours	ADM3202	Carsem-M 16-SOIC_N	Q7498.82	50	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	ADM202E	Carsem-M 16-SOIC_N	R86153.1	45	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	AD7707	Amkor-P 20-SOIC_W	AB60669.1	50	0
Solder Heat Resistance (SHR)[1]	ADI-0049	See Footer	ADM202E	Carsem-M 16-SOIC_N	R86176.1	10	0
Solder Heat Resistance (SHR)[1]	ADI-0049	See Footer	ADM3202	Carsem-M 16-SOIC_N	Q7498.305	15	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C 500 cycles	ADM202E	Carsem-M 16-SOIC_N	R86154.1	45	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C 500 cycles	ADM3202	Carsem-M 16-SOIC_N	Q7498.303	50	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Table 6: Fab Qualification Test Results

Test Name	Spec	Conditions	Device	Fab Process	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, Method 1015	125°C 48 hours	AD7314	TSMC 2A 6" 0.6µm CMOS	AA88950.1	400	0
					AA88950.2	400	0
					AA88950.3	210	0
			ADM1029		n91512.7	110	0
					N91512.4	150	0
					N91512.5	150	0
					N91512.6	150	0
					O91631.1	255	0
					O91631.2	255	0
Biased HAST (HAST)	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	ADV7175	TSMC 2A 6" 0.6µm CMOS	F124480.4	45	0
					F124481.4	45	0
					F124482.4	45	0
			AD73322		F117464.5	45	0
					F125657.9	45	0
					F117966.7	45	0
Biased HAST (HAST) [1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	AD9281	TSMC 2A 6" 0.6µm CMOS	J31360.1	77	0
					J31358.1	77	0
					J31359.1	77	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C ‹ Tj ‹ 135°C, Biased 1,000 hours	AD7015	TSMC 2A 6" 0.6µm CMOS	OF45308.4	45	0
					OF46725.4	45	0
					OF46726.4	45	0
			ADM1025		F102031.4	76	0
					F102041.4	77	0
					F102042.4	77	0
			AD7314		AA88981.1	50	0
		150°C ‹ Tj ‹ 175°C, Biased 1,000 hours			R86144.1	45	0
					R86343.1	45	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C 1,000 hours	AD6421	TSMC 2A 6" 0.6µm CMOS	F108185.22	45	0
					F108185.28	45	0
					F108185.34	45	0
			AD73322		F117464.7	45	0
					F117966.4	45	0
					F121100.11	45	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field Induced Charge Device Model (FICDM) ESD testing are summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at the Analog Devices Website (Analog Website).

Table 7: ESD Test Results

ESD Model	Device	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	AD7812	20-SOIC_W	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±1500V	NA	C6
	AD7811	16-SOIC_N			±1000V	±1500V	C5
	AD7810	8-PDIP			±1500V	NA	C6
HBM	AD7812	20-SOIC_W	ANSI/ESD STM5.1-2007	1.5kΩ, 100pF	±2500V	±3000V	2
	AD7810	8-PDIP			±3000V	±3500V	2

Latch-Up Test Results

Six AD7812 devices were subjected to latch-up testing per JEDEC Standard JESD78, Class II, Level A, at T_A=25°C. All parts were electrically tested at room temperatures pre- and post stress. All six devices passed.

Approvals

This report has been approved by electronic means (4.0). Reliability Engineer: Fergus Downey

Additional Information

Data sheets and other additional information are available on Analog Devices' web site: Analog Website