A 4 Tx/Rx, 0.1-18GHz 3UVPX Tuner + Digitizer + Processor System on Module

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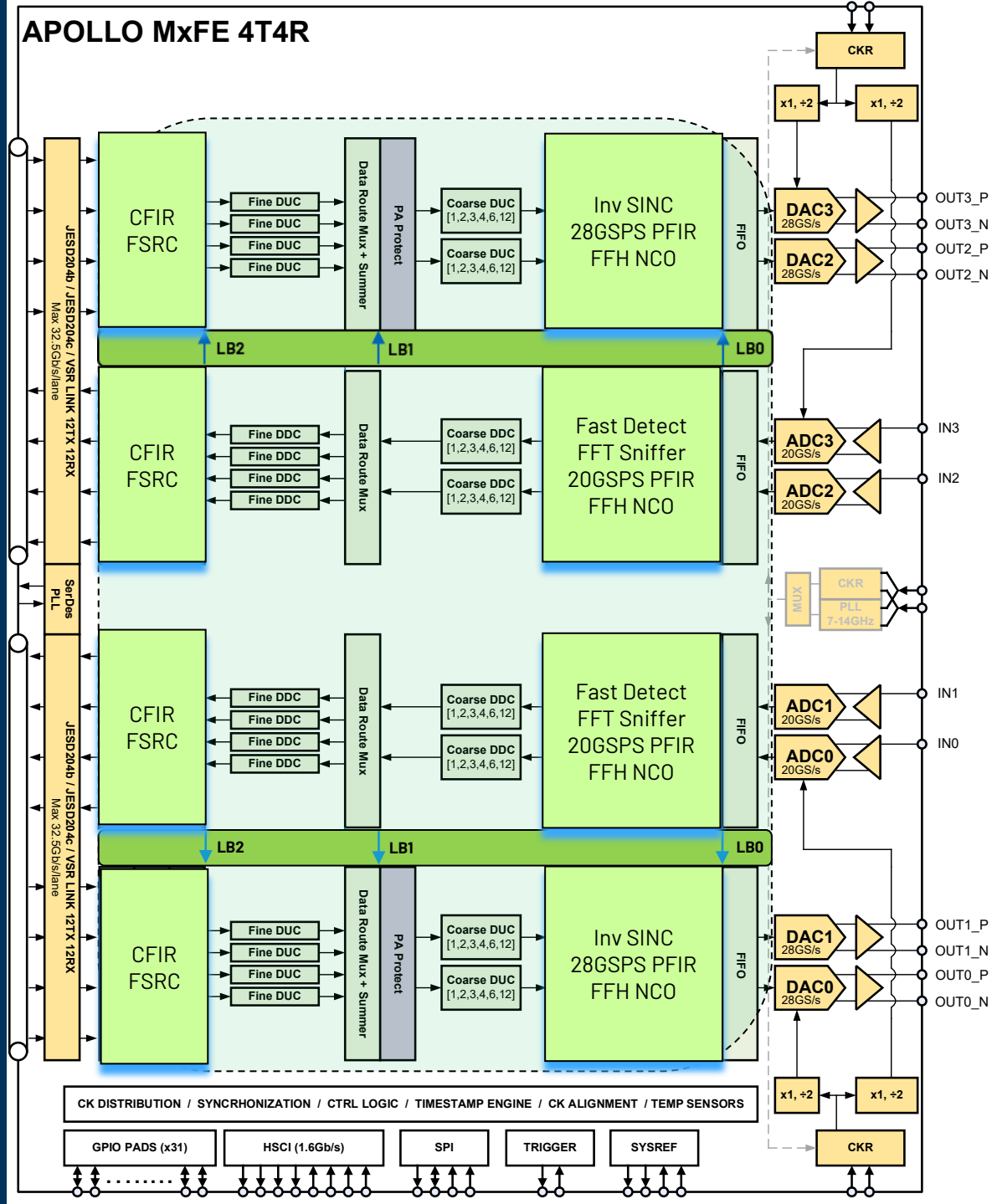
Product Line Manager, COTS Digitizers

analog.com

SCAN ME

New Apollo MxFE™ – 4T4R AD9084

- **4 Channel 20GSPS Rx, 28GSPS Tx**
- **RF Bandwidth: DC to 18GHz**
- **Frequency Agile across L,S,C, X, Ku-Band**
  - iBW: 10GHz/channel in Full Bandwidth Mode (2T2R)
  - iBW: 4GHz/channel with DSP enabled (4T4R)
- **Programmable & Dynamically Reconfigurable DSP**
  - Coarse & Fine Decimation / Interpolation 1x-1536x
  - Coarse & Fine Independent FFH NCOs
- **Offload FPGA Compute from Fabric to ASIC**
  - FFT Sniffer, PFILT, CFIR, FSRC
- **Differential & Single Ended Input Variants**



Apollo MxFE™ Microwave Digitizer IC Ecosystem

Codesigned Integrated Circuits With Apollo MxFE™ In-Mind

- Clocking PLLs / Synthesizers
  - 22GHz PLL VCO
- Power Distribution Network
  - Switching Regulators
  - Linear Drop-Out Regulators
- RF/Microwave Front-End Circuitry
  - Multifunction Up-/Down-Converters
  - RF Amplifiers
  - Digital Step Attenuators
  - Tunable Filters
  - Analog Beamforming ICs

Microwave Digitizer SOMs – Existing & Future

Software Defined Radio Modules

ADALM-PLUTO

Available

#Chan: 1T1R

IC: AD9363

RF Tuning: 0.33-3.8GHz

IBW: 20MHz

Processor: Xilinx Zynq Z-7010

AD-JUPITER-EBZ

Available

#Chan: 2T2R

IC: ADRV9002

RF Tuning: 0.03-6GHz

IBW: 40MHz

Processor: Xilinx Zynq UltraScale+ MPSoCs XCZU3EG

System on Module (SOM) Cards

ADRV9364-Z7020

Available

#Chan: 1T1R

IC: AD9364

RF Tuning: 0.07-6GHz

IBW: <0.2-56MHz

Processor: Xilinx Zynq XC7Z020-1CLG400I

ADRV9361-Z7035

Available

#Chan: 2T2R

IC: AD9361

RF Tuning: 0.07-6GHz

IBW: <0.2-56MHz

Processor: Xilinx Zynq XC7Z035-L2FBG676I

ADRV9009-ZU11EG + FMCOMMS8

Available

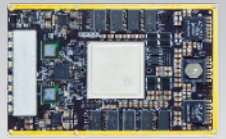
#Chan: 8T8R8O

IC: ADRV9009

RF Tuning: 0.08-6GHz

IBW: 200MHz

Processor: Xilinx UltraScale+ ZU11EG (8GB DDR4)



3UVPX Ruggedized Apollo FFSOMs

ADSY1100 3UVPX

2Q CY25

#Chan: 4T4R

IC: AD9084 (Apollo)

RF Tuning: 0.1-20GHz

IBW:

<8GHz (2T2R)

<4GHz (4T4R)

Processor: Xilinx Virtex UltraScale+ VU11P + Zynq ZU4EG

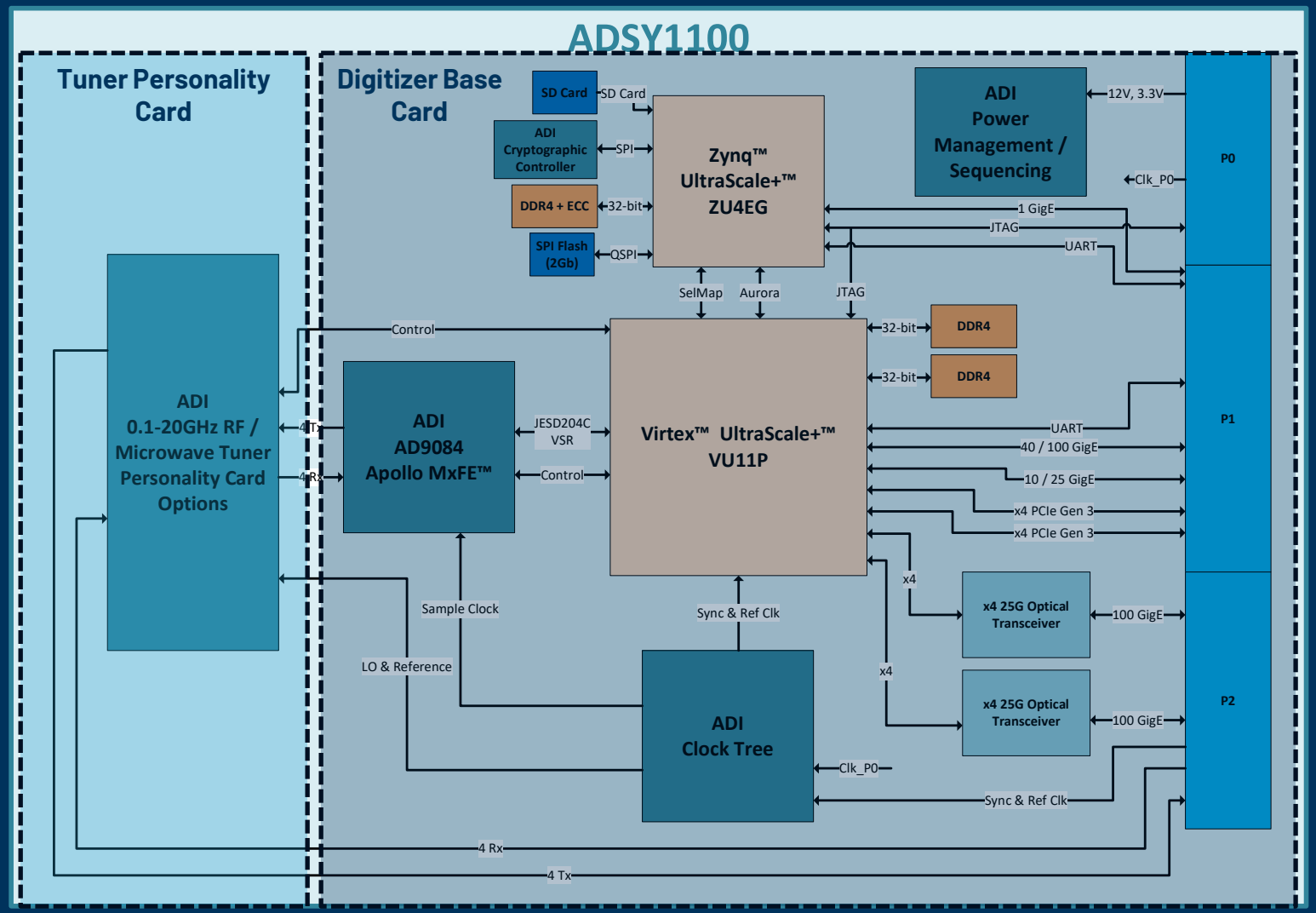
Housing: Ruggedized Environmental Enclosure

AD-SYNCHRONA14-EBZ

Available

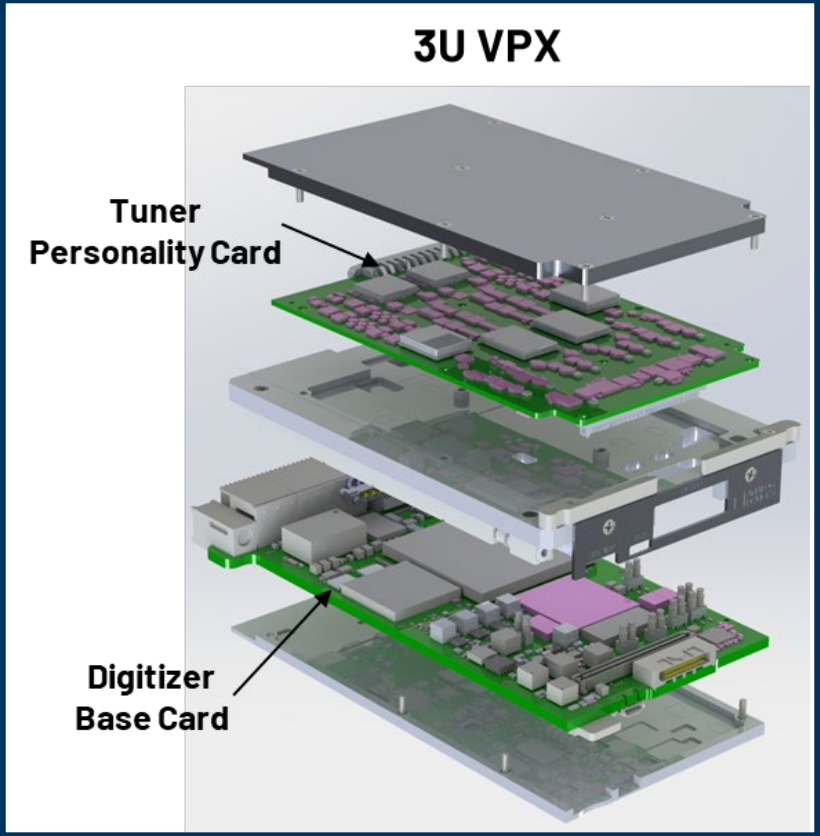
Multichannel System Clocking
Provides high-accuracy reference clock distribution
Synchronize up to 7× ADRV9009-ZU11EG RF SOMs and FMCOMMS8 for coherent operation of 56 RF channels
Price: $3k

ADSY1100: 4T/4R, 0.1-20GHz, 1" Pitch 3UVPX RF SOM

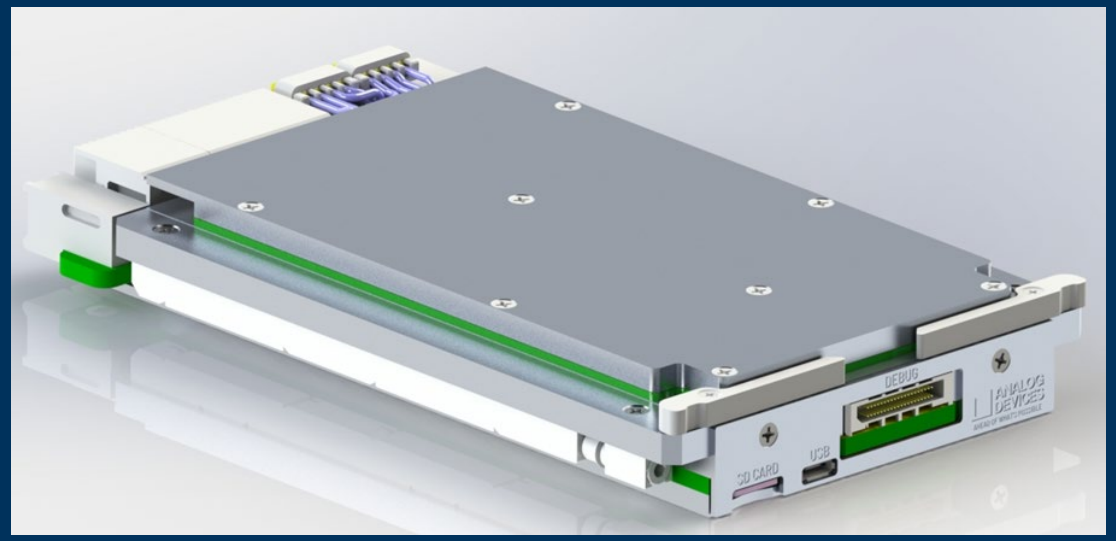


Key Digitizer Base Card Features

- 4x 20GSPS ADCs
- 4x 28GSPS DACs
- Hardened DSP FFT Sniffer
- Fast-Frequency Hopping
- AD9084 Low-Latency Loopback



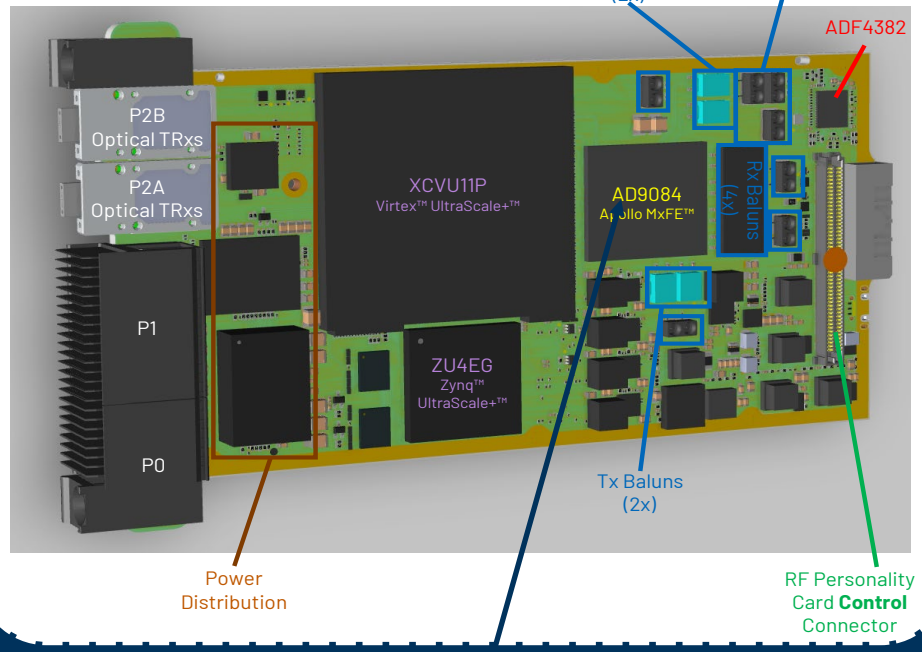
ADSY1100 Microwave SOM Initial Specifications



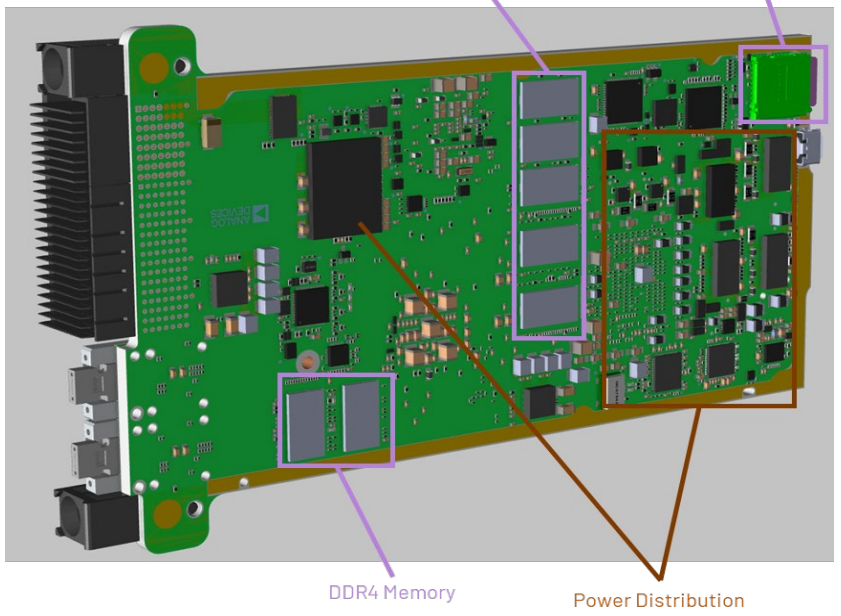
SCAN ME

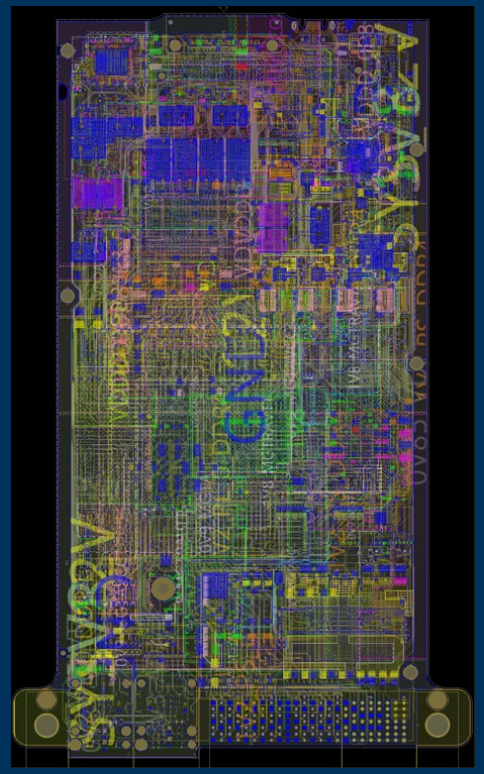
ADSY1100: Apollo MxFE™-Based Digitizer Base Card

Digitizer Base Card Top

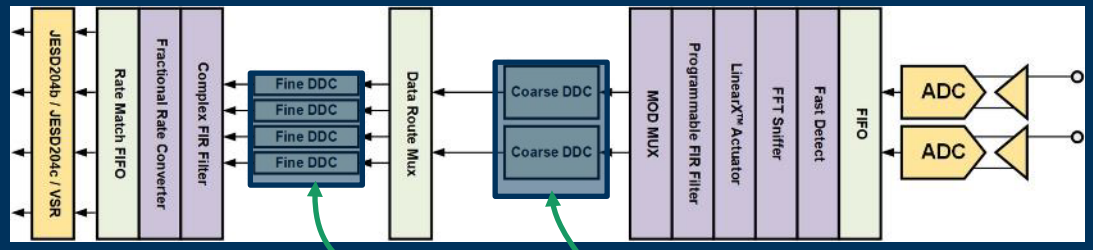


Digitizer Base Card Bottom

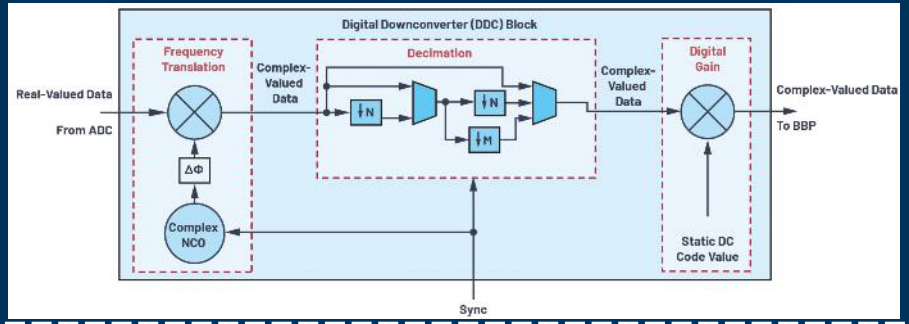


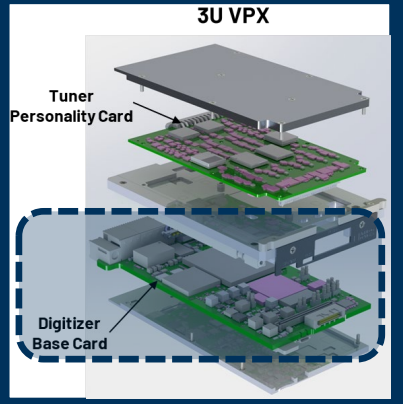


AD9084 Hardened Digital Signal Processing Blocks

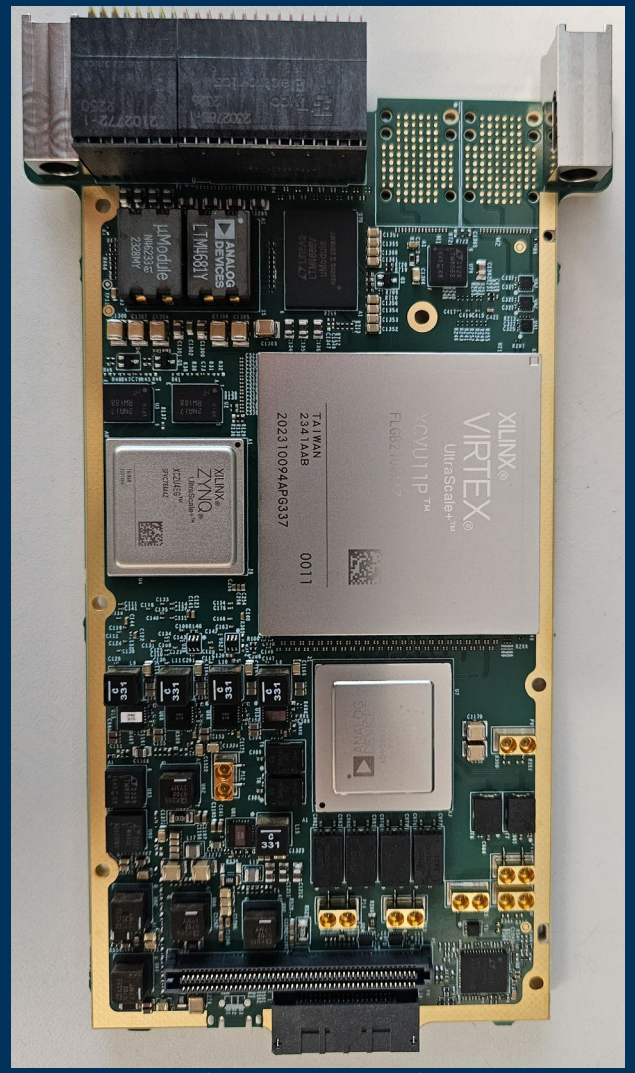


AD9084 Hardened DDCs Offload FPGA Resources

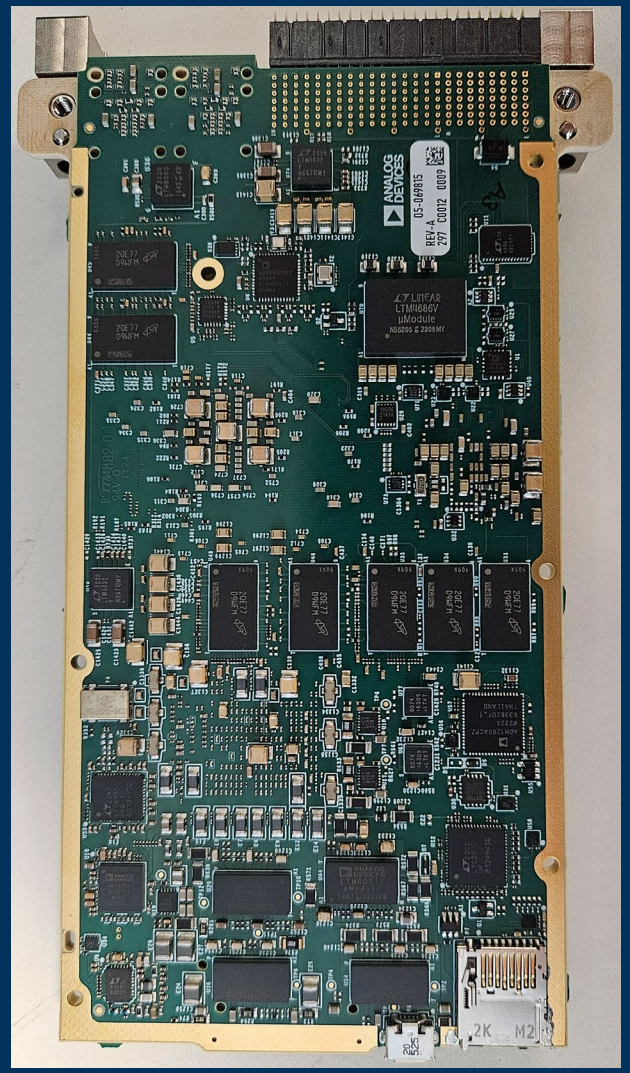




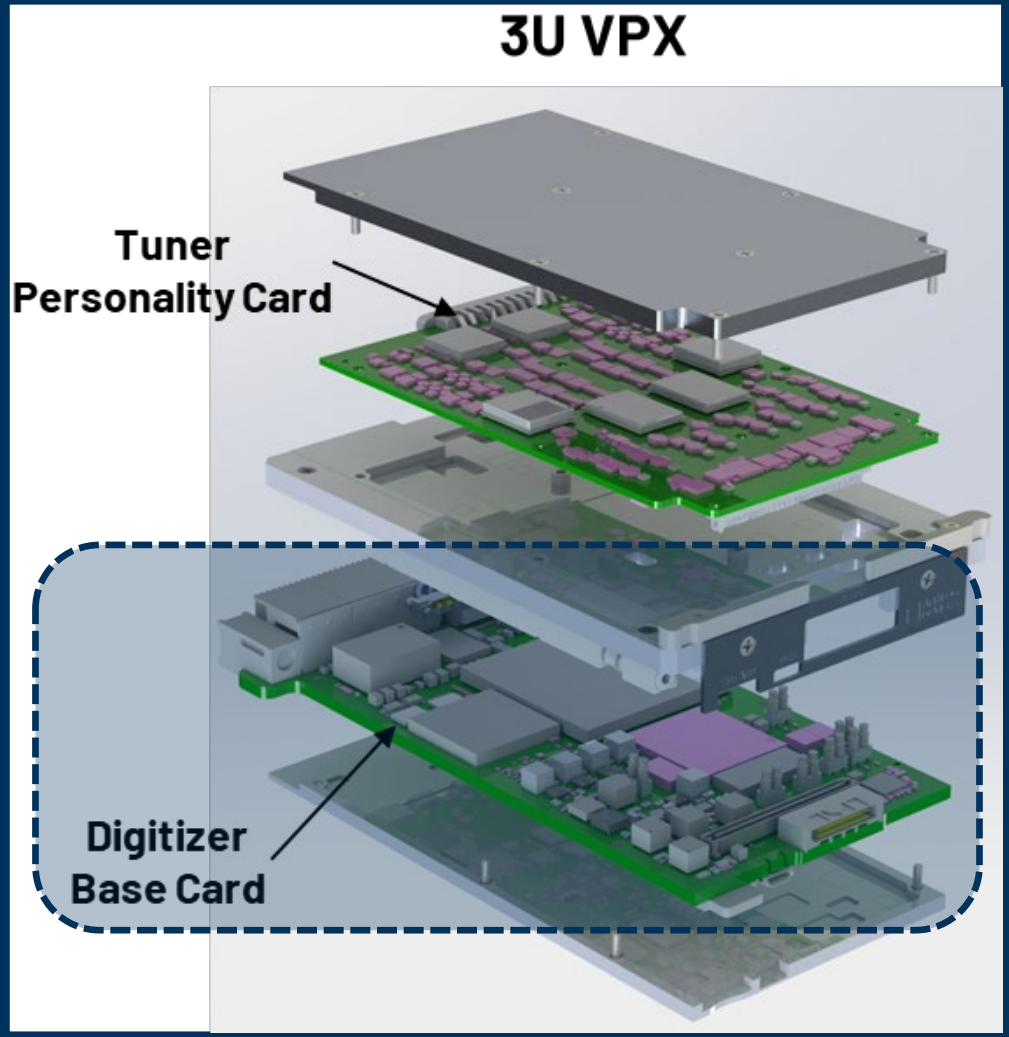
Prototype Microwave Digitizer Base Cards



Primary Side



Secondary Side

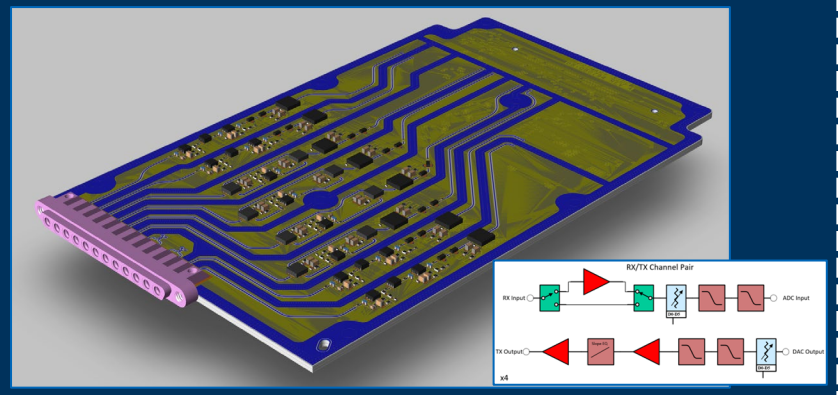


ADSY1100: Swappable Microwave Tuner Personality Cards

Passthru RFPC

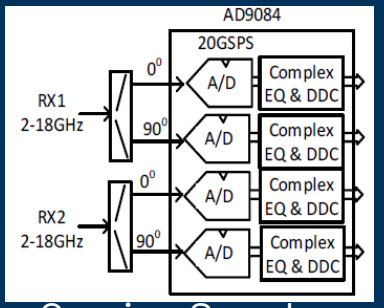
4T/4R Through Traces

Simple, 1st Nyquist RFPC



4T/4R RF Chain: 10MHz – 8.5GHz

40GSPS Apollo MxFE™ Interleaving RFPC

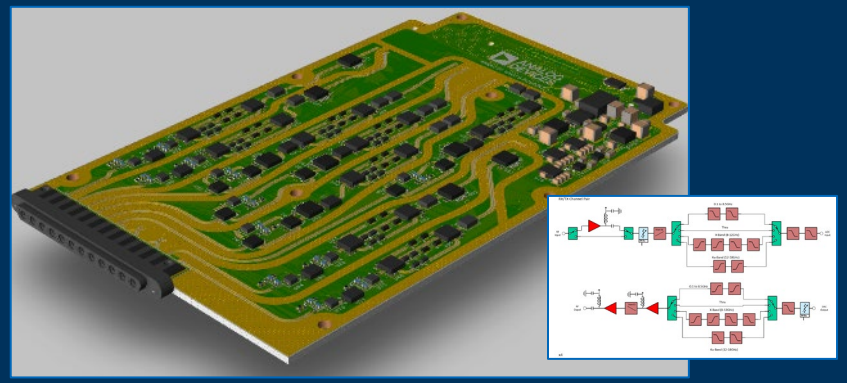


Coming Soon!

P Delos, B Reggiannini, "Doubling ADC Sampling Bandwidth with Direct Quadrature Sampling," Government Microcircuit Applications and Critical Technology Conference, 2024.

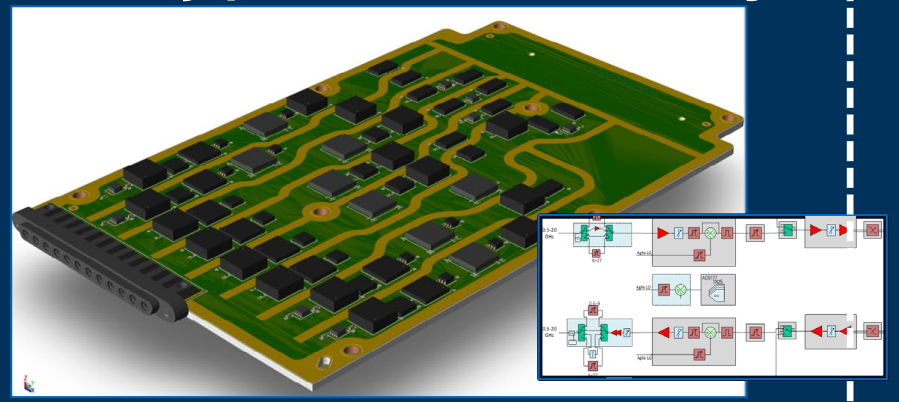
2T/2R: 20GHz Nyquist

1st & 2nd Nyquist RFPC (No Mixing)

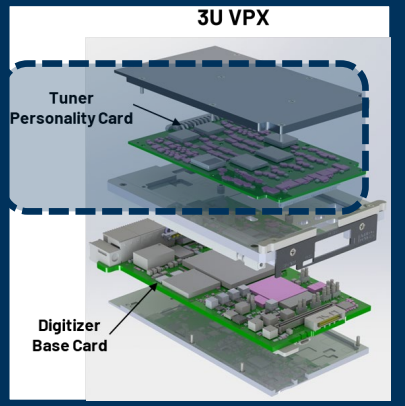


4T/4R Switched RF Chain: 100MHz – 18GHz

1st Nyquist RFPC (With Mixing)

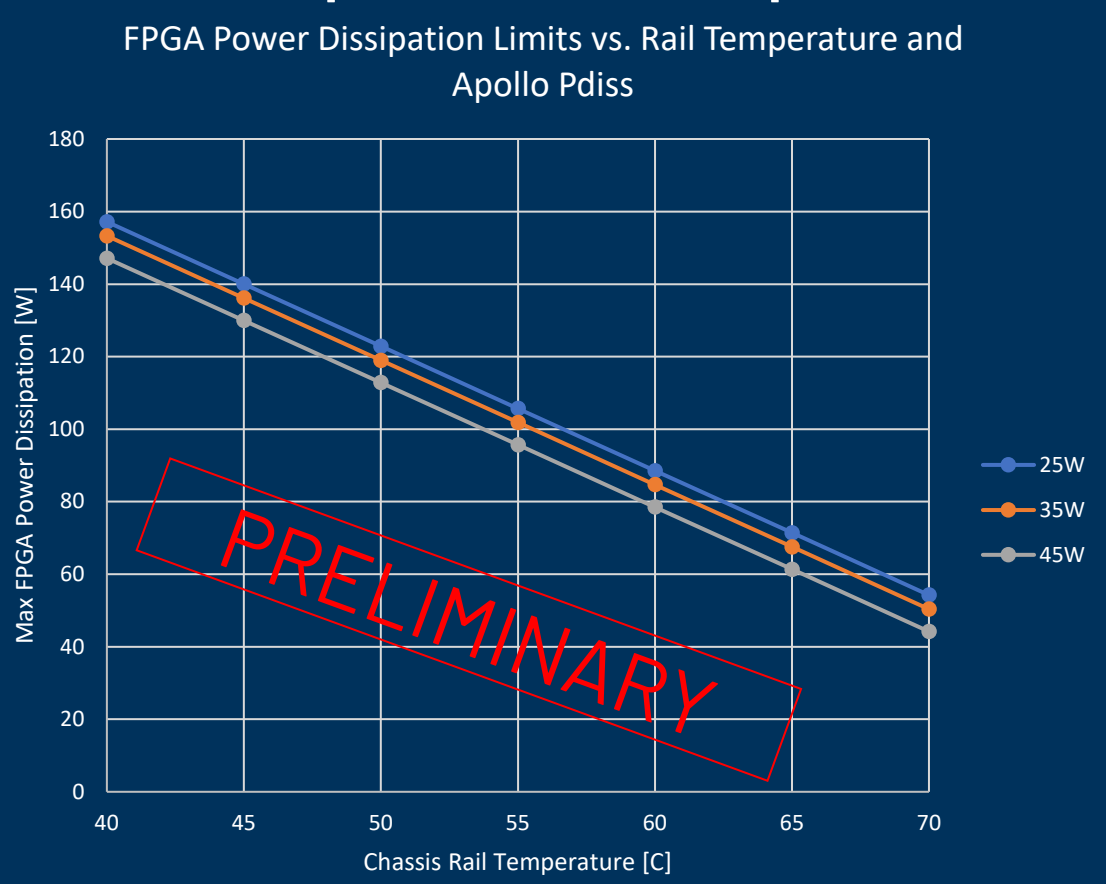


4T/4R Wideband RF Chain: 100MHz – 20GHz



ADSY1100 Mechanical / Thermals

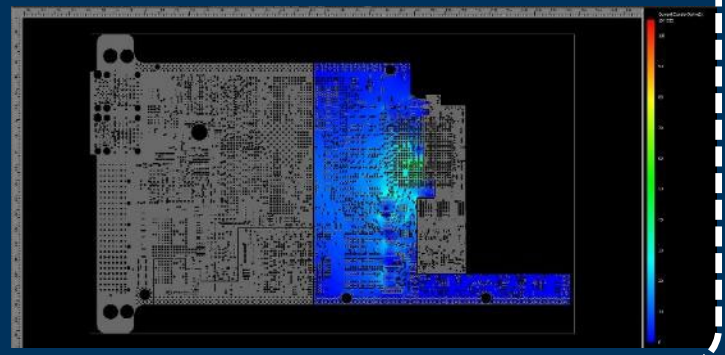
Power Dissipation vs. Rail Temperature:

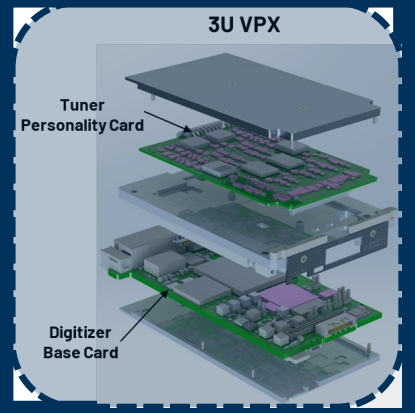


Rail Temperature vs. Power Dissipation:

Max Rail Temp		FPGA Pdiss						
		30	40	50	60	70	80	90
Apollo Pdiss	25	76	75	72	69	66	62	59
	35	75	73	70	67	64	61	58
	45	72	71	69	66	63	60	57

IR Drop → Thermals





Thermal Simulations Performed for Various Thermal Loads

ADSY1100 HDL / Software

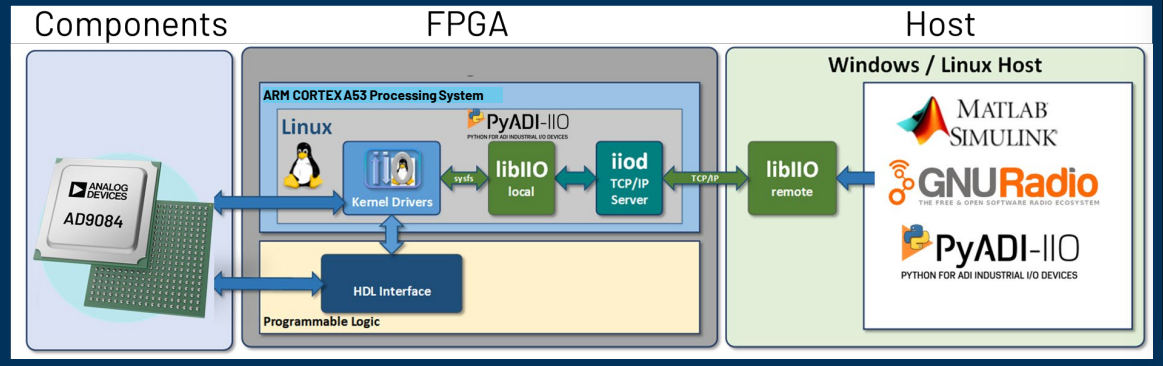
Consistent ecosystem across ADI converter, clock chip

System team provides

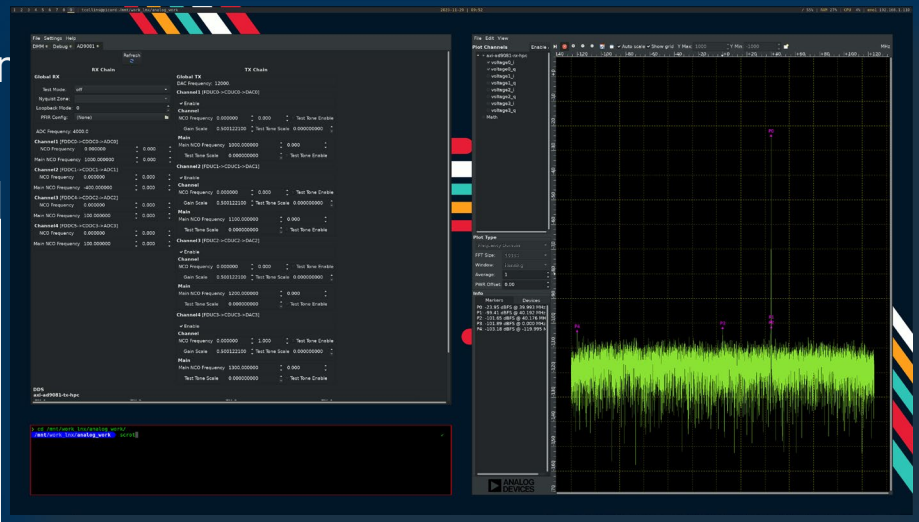
- ✓ **“Golden” HDL reference designs**
- ✓ **In-kernel software drivers**
- ✓ **Kuiper Linux and PetaLinux userspaces**
- ✓ **Bare-metal software drivers (No-OS) / projects**
- ✓ **Bindings & interfaces to 3rd party tools**
- ✓ **Configuration and debug tooling**

All drivers, software, & HDL are supported, updated, & r

“Take what you need” for your system




```python
import adi
import matplotlib.pyplot as plt
from scipy import signal

dev = adi.ad9084("ip:10.44.3.185")

print("CHIP Version:", dev.chip_version)
print("API  Version:", dev.api_version)

print("TX SYNC START AVAILABLE:", dev.tx_sync_start_available)
print("RX SYNC START AVAILABLE:", dev.rx_sync_start_available)

# Configure properties
print("--Setting up chip")

# Set NCOs
dev.rx_channel_nco_frequencies = [0] * 4
dev.tx_channel_nco_frequencies = [0] * 4

dev.rx_main_nco_frequencies = [-2800000000] * 4
dev.tx_main_nco_frequencies = [10000000000] * 4

dev.rx_enabled_channels = [0]
dev.tx_enabled_channels = [0]
dev.rx_nyquist_zone = ["odd"] * 4
```

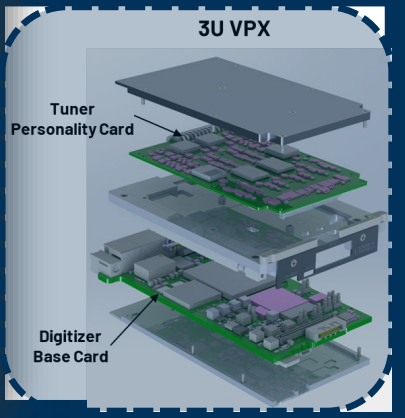


ADSY1100 includes:

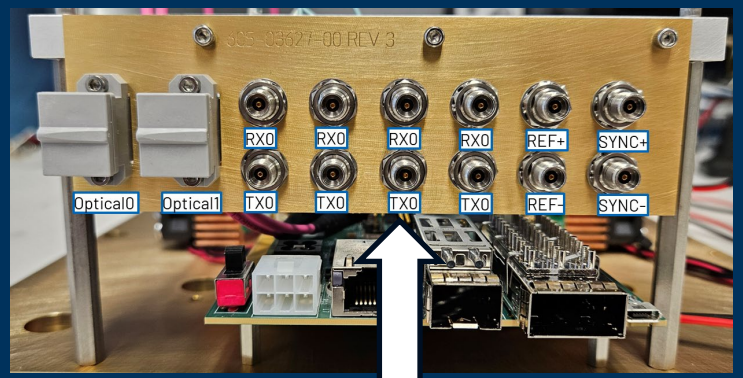
- ✓ ADI JESD204 cores (PHY, Link, TPL)
- ✓ DMA
- ✓ PCIe/Ethernet offload
- ✓ SelMap & Aurora
- ✓ HSCI
- ✓ System-level drivers in IIO kernel
- ✓ Bare-metal project in Xilinx SDK

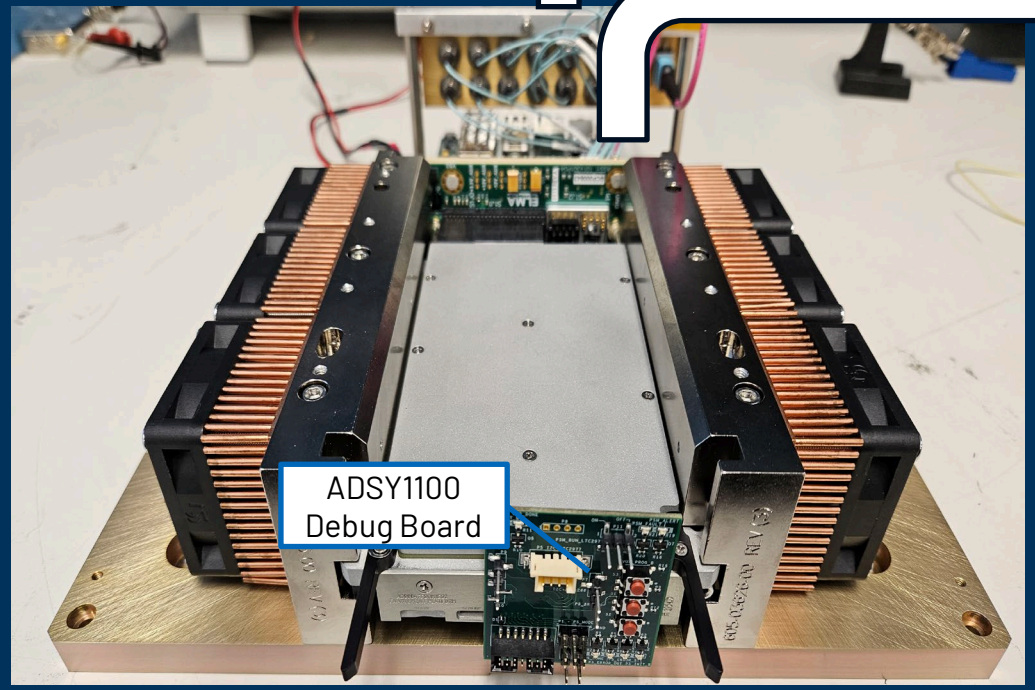
Application-level support for:

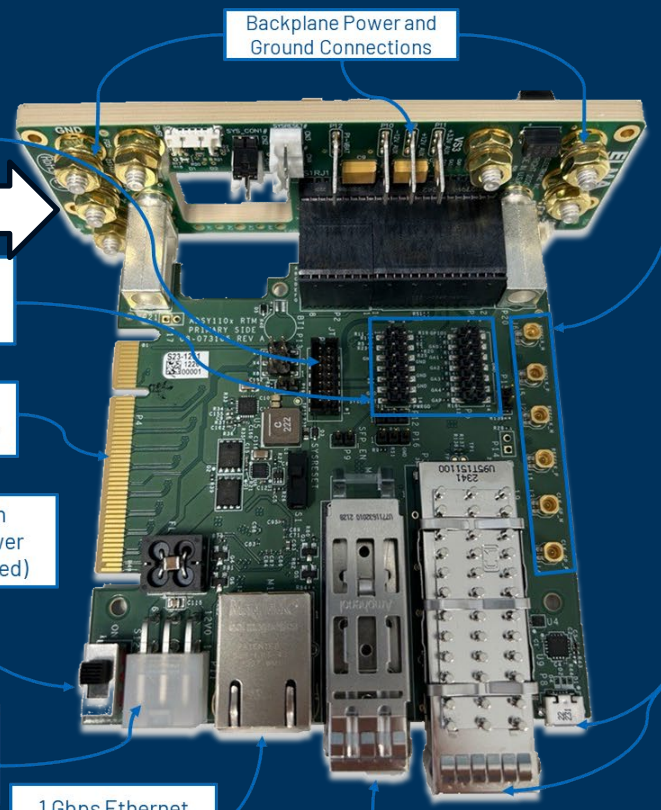
- ✓ libIIO
- ✓ MATLAB (Streaming & targeting)
- ✓ Python (pyadi-iio)
- ✓ Others



ADSY1100 RF/Microwave Digitizer Test Setup







Backplane Power and Ground Connections

RF Connections for clocking

JTAG

Digital IO

PCIE Gen 3 x8 Edge Connector

Power Switch (If the RTM Power connector is used)

UART Terminal Connection (MicroUSB Connector)

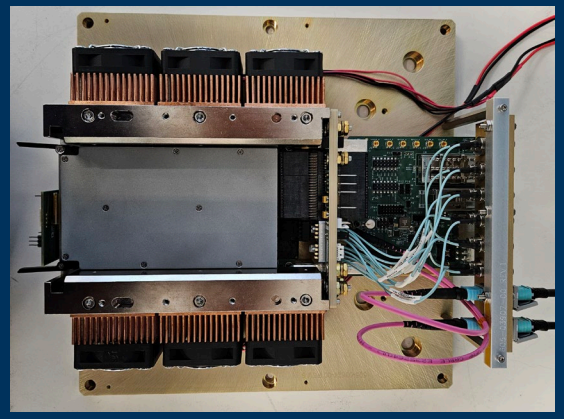
40/100 Gbps Ethernet (QSFP+ Connector)

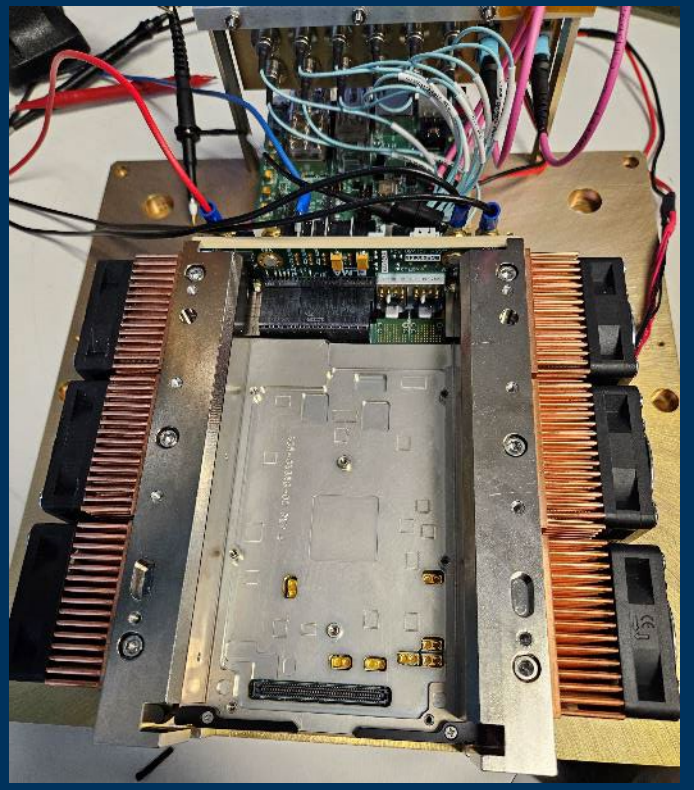
10/25 Gbps Ethernet (SFP+ Connector)

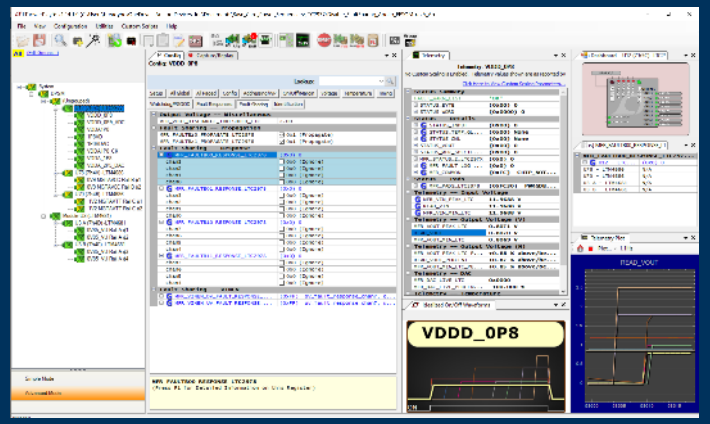
RTM Power Connector - This may be used instead of the backplane power

1 Gbps Ethernet (RJ45 Connector)

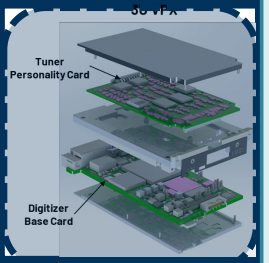
ADSY1100 Microwave Digitizer Prototype Testing

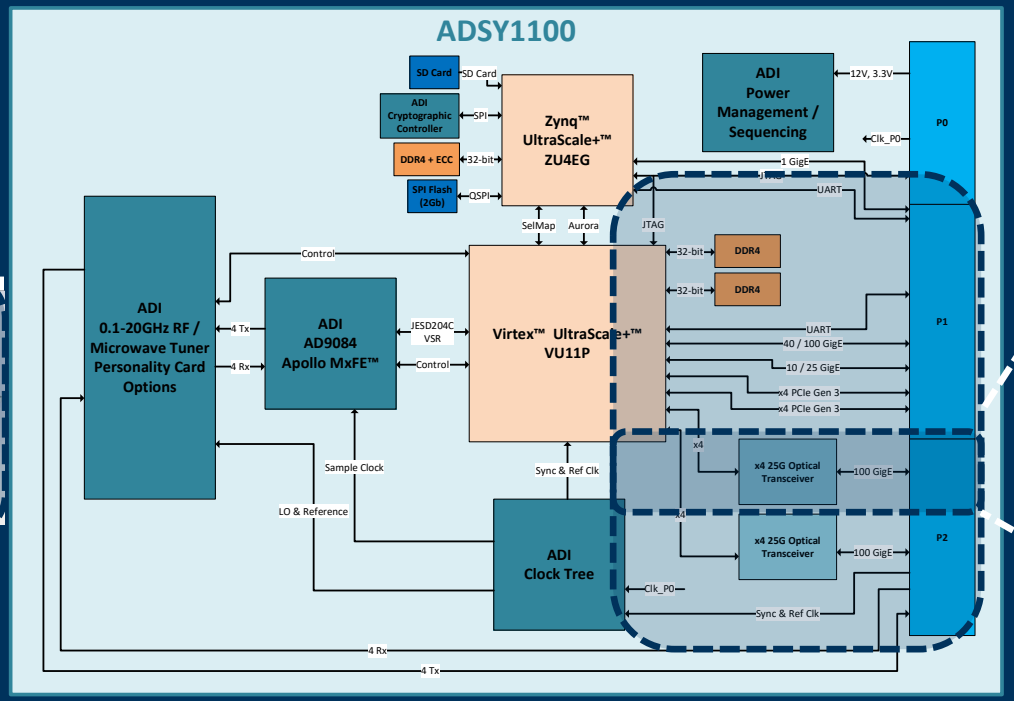




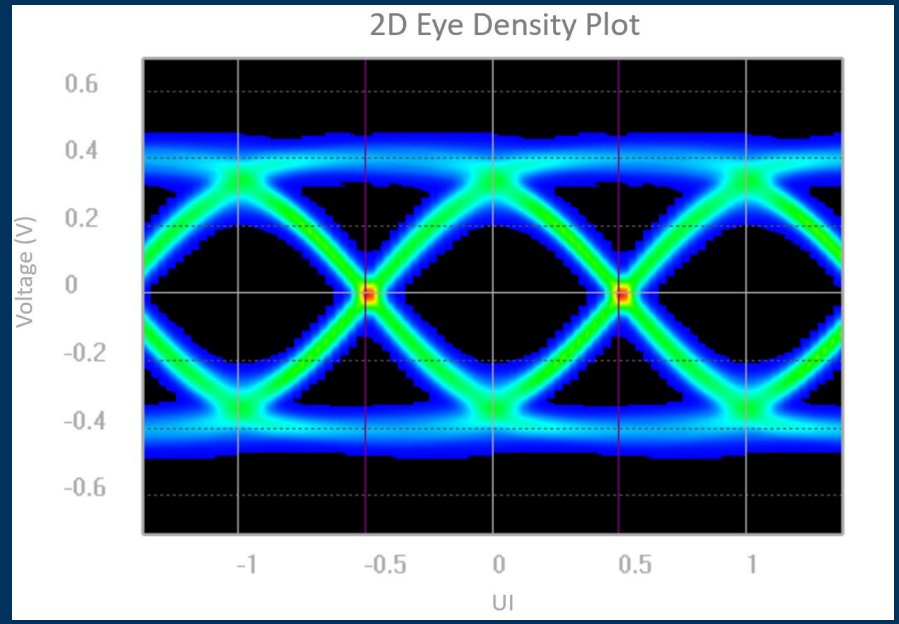


ADSY1100: Processor Offload Options





Optical Ethernet Eye Diagram



Backplane Offload Method	Scaled Throughput [Gbps]	Allowed Sample Rate for All 4 RF Channels [GSPS][a]	Allowed Sample Rate for 1 RF Channel [GSPS][a]
DDR4 Memory Via 1Gbps Ethernet	0.940	0.267[b]	1.068[b]
10Gbps Ethernet	9.40	0.073	0.293
40Gbps Ethernet	37.6	0.293	1.175
PCIe Gen 3	63.0	0.492	1.968
200Gbps Ethernet (Optical)	188	1.468	5.000

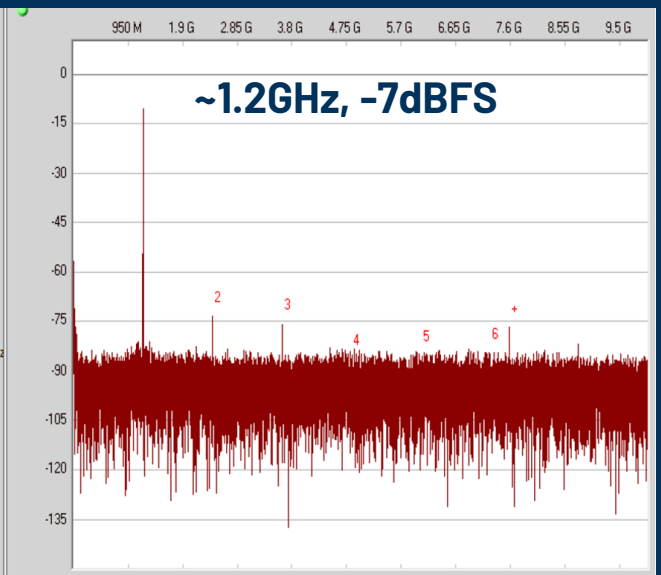
[a] Assumes 16-bit I/Q
[b] Using DDR4 as capture buffer

AD9084: 20GSPS ADC/DAC Test Results

Pre-Release ADC Results

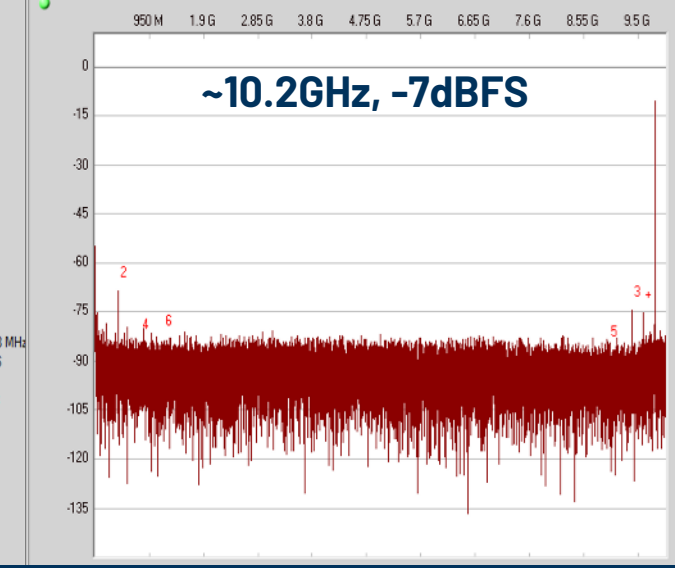
Date = 11/8/2023
Time = 10:32:19 AM
Sample Frequency = 20000 MHz
Samples = 65536
SNR = 40.084 dB
SNRFS = 46.987 dB
SINAD = 40.05 dBc
DC Frequency = 0 MHz
DC Power = -52.49 dBFS
Fund Frequency = 1209.021 MHz
Fund Power = -6.903 dBFS
Fund Bins = 21
Harm 2 Power = -63.183 dBc
Harm 3 Power = -65.793 dBc
Harm 4 Power = -83.922 dBc
Harm 5 Power = -80.026 dBc
Harm 6 Power = -77.663 dBc
Worst Other Frequency = 7582.041 MHz
Worst Other Power = -73.712 dBFS
Noise / Hz = -146.987 dBFS / Hz
Average Bin Noise = -92.142 dBFS
THD = -61.107 dBc
SFDR = 63.183 dBc

SFDR: 70.1dBFS

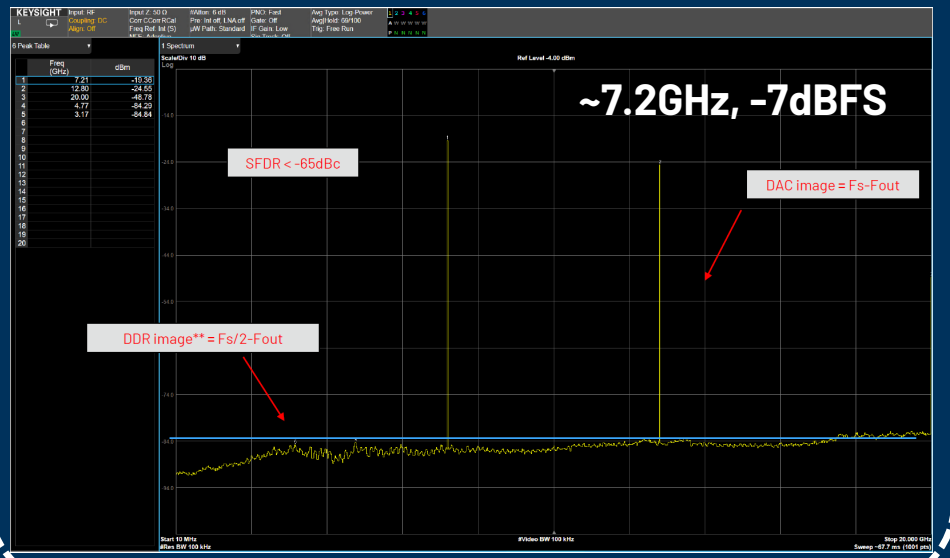


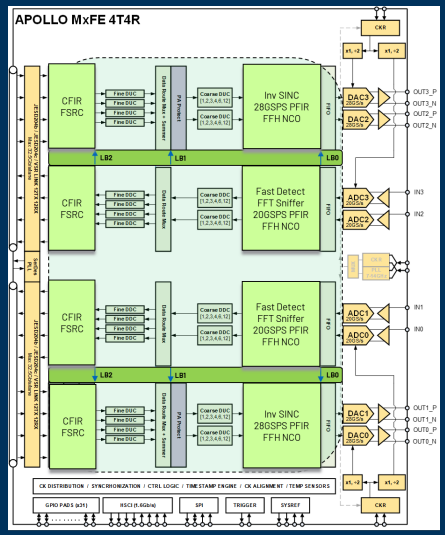
Date = 11/8/2023
Time = 11:26:31 AM
Sample Frequency = 20000 MHz
Samples = 65536
SNR = 38.623 dB
SNRFS = 45.563 dB
SINAD = 38.566 dBc
DC Frequency = 0 MHz
DC Power = -51.97 dBFS
Fund Frequency = 9800.02 MHz
Fund Power = -6.941 dBFS
Fund Bins = 21
Harm 2 Power = -58.428 dBc
Harm 3 Power = -64.717 dBc
Harm 4 Power = -80.837 dBc
Harm 5 Power = -86.205 dBc
Harm 6 Power = -76.533 dBc
Worst Other Frequency = 9599.968 MHz
Worst Other Power = -72.063 dBFS
Noise / Hz = -145.563 dBFS / Hz
Average Bin Noise = -90.718 dBFS
THD = -57.432 dBc
SFDR = 58.428 dBc

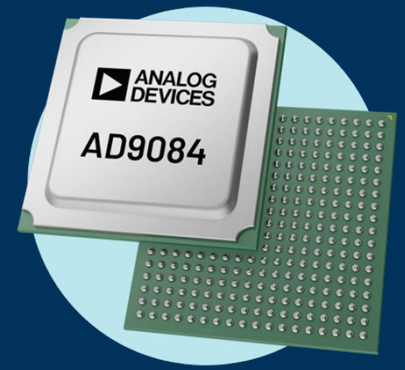
SFDR: 65.4 dBFS



Pre-Release DAC Results







AHEAD OF WHAT'S POSSIBLE

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ANALOG DEVICES

SCAN ME