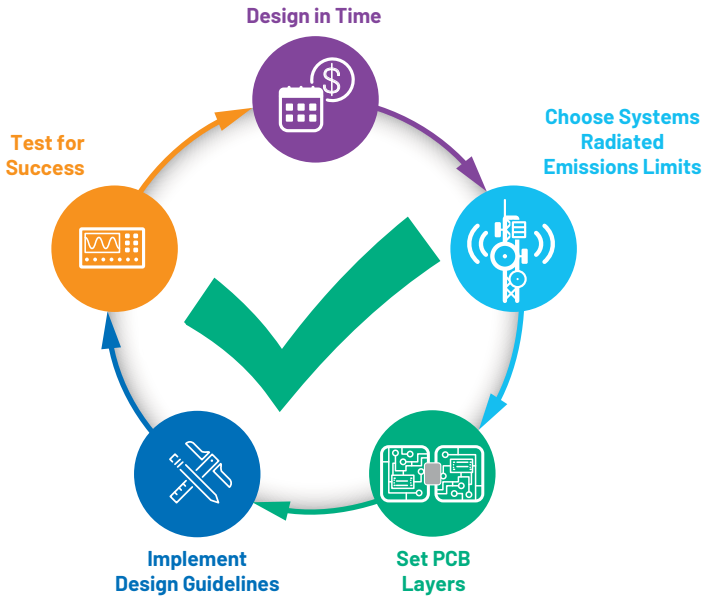
Simple Steps to EMI Compliance

ADM2582E and ADM2587E Signal and Power Isolated RS-485

Passing Your EMC Certification Is a Time-to-Revenue Differentiator



Design for EMI Compliance

- Easily reduce emissions
- Verified component choices
- Proven PCB layout

Emissions Increase	USA	EU+
Class A	Nonresidential	Industrial
Class B	Residential	Residential, Commercial, Light Industrial

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ADI iCoupler®

1. Choose a 2- or 4-Layer PCB

Emissions Limits: Class A vs. Class B

- Depending on your radiated emissions requirements (Class A or Class B), it is important to select the correct number of layers for your PCB. Typically with the ADM2582E and ADM2587E, Class A can be met with a margin on a 2-layer PCB.
- For the more stringent Class B requirements, a stitching capacitance is required in order to meet the required limits. On a 2-layer PCB, this requires the use of a discrete high voltage capacitor. On a 4-layer PCB, use of an embedded interplane capacitor provides better radiated emissions performance.
- Please see Table 1 for more detail on the device setup, load, and measured margin on the required emissions class. Select the number of layers for your design and continue with the layout guide.

Table 1. Trade-Offs to Meet the Required Radiated Emission Level

	Layer Count	CISPR 32	Pass Margin (dB)	Supply (V)	Data Rate	Stitching Capacitor Technique	Load (Ω)
ADM2587E	4	B	5.5	3.3	500 kbps	Embedded	54
	4	B	8.5	5	500 kbps	Embedded	54
	2	A	3.9	3.3	500 kbps	None	54
	2	A	4	5	500 kbps	None	54
ADM2582E	4	B	4.7	3.3	16 Mbps	Embedded	54
	4	B	6.5	5	16 kbps	Embedded	54
	2	A	1.2	3.3	16 Mbps	None	54
	2	A	4.7	5	16 Mbps	None	54
	2	B	3.7	3.3	16 Mbps	Discrete	54
	2	A	7.5	5	16 Mbps	Discrete	54

2. Follow Recommended Decoupling

2-Layer PCB | 4-Layer PCB

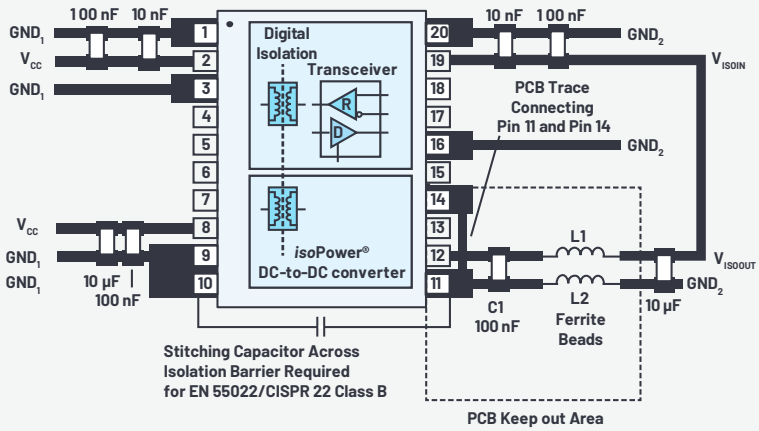


Figure 1. PCB decoupling for 2-layer and 4-layer PCB.

- Figure 1 shows the components and connections required to meet the desired radiated emissions limits.
- Device decoupling requirements are as follows:
  - 100 nF and 10 nF ceramic caps from V_{CC} to GND1 (C4/C3) and V_{ISOIN} to GND2 (C5/60).
  - 100 nF and 10 µF from V_{CC} to GND1 (C9/C7) and V_{ISOOUT} to GND2 (C1/C8).
- Placement of ceramic caps as shown in Figure 2 and Figure 3 for 2- and 4-layer boards, respectively. Ensure the lower value cap is nearest the DUT.
- Capacitor form factors are as follows:
  - C4, C6, C8, and C9 are 0805 footprint.
  - C1, C3, C5, and C7 are 0603 footprint.

2. Follow Recommended Decoupling (Continued)

2-Layer PCB	4-Layer PCB

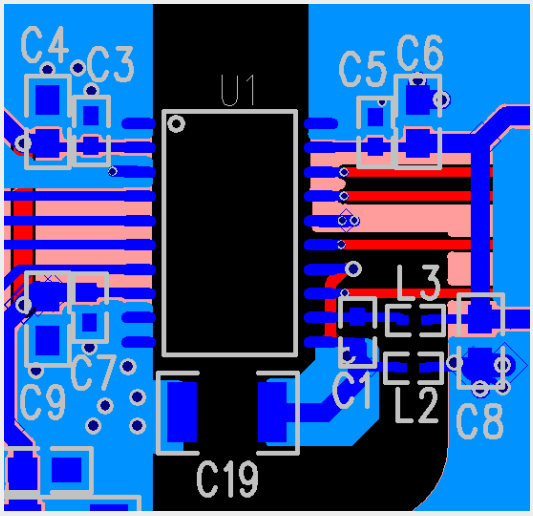


Figure 2. 2-layer PCB.

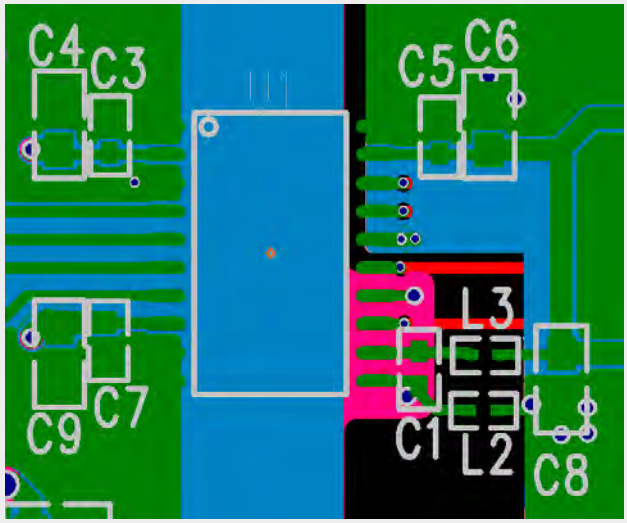


Figure 3. 4-layer PCB.

3. V_{ISO} and GND2 Connections

2-Layer PCB	4-Layer PCB

- The selection of the ferrite bead for L3 and L2 is critical in order to meet the required emissions limits. This ferrite bead is required to be high impedance over a broad frequency range and it is recommended to use the BLM15HD182SN1 ferrite bead. Figure 4 shows the impedance curve for the ferrite bead.
- To reduce the capacitive coupling of high frequency noise, ensure there is a minimum 4 mm separation between the isolated ground copper pour at Pin 11 and the GND2 plane, as shown in Figure 2 and Figure 3. Provide cutouts around and below L2 and L3 on all layers.
- Do not connect the V_{ISOOUT} pin to a power plane. Ensure that the V_{ISOIN} (Pin 19) is connected through the L3 ferrite bead to the V_{ISOOUT} (Pin 12) connect between V_{ISOOUT} and V_{ISOIN} using a PCB trace, as shown in Figure 2 and Figure 3.
- Similarly do not connect the GND2 (Pin 11 and Pin 14) directly to the GND2 plane. Connect Pin 14 and Pin 11 using a PCB trace. Ensure that the these pins are connected through the L2 ferrite bead to the GND2 plane.

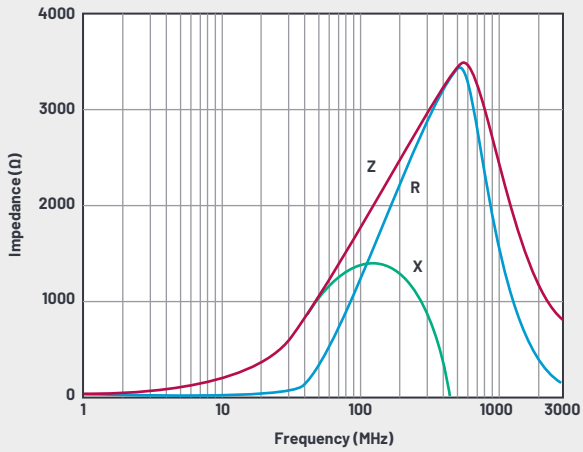


Figure 4. BLM15HD182SN1 impedance curve.

4. Provide a Return Path for High Frequency (Common-Mode) Noise

2-Layer PCB

Follow the implementation of the stitching capacitor depending on your PCB layer requirements.

- For a 2-layer PCB, place a high voltage decoupling capacitor as shown.
- Suggested capacitor:
  - Value: 100 pF
  - Case: 1812
  - Manufacturer: TDK
  - Manu. No: C4532C0G3F101K160KA

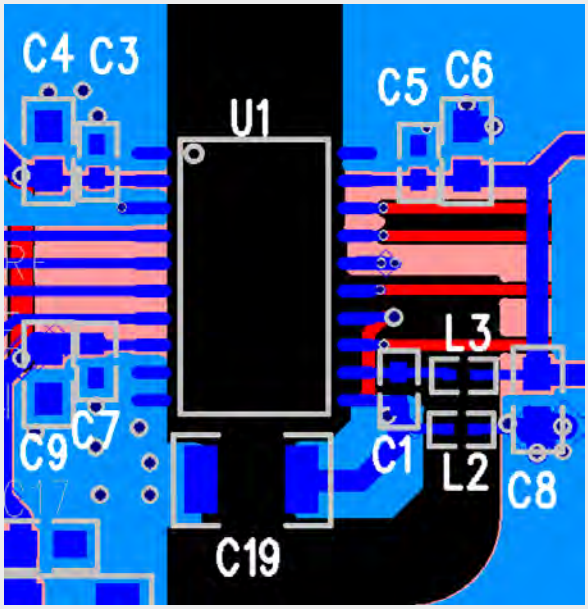


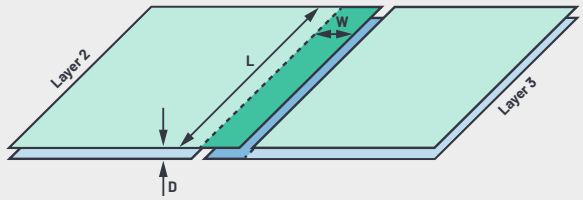
Figure 5. Placement of high voltage stitching capacitor.

4-Layer PCB

- Class B can be achieved by placing an embedded stitching capacitor between GND_{ISO} and GND1 on layers 2 and 3. The capacitance required to meet Class B is 35 pF.
- Adjust W, L, and D of overlapping planes to required capacitance. On Layer 3, connect the floating overlapping plane to GND_{ISO} (Pin 11 and Pin 14) only.
- Note: IEC 61010 third edition requires D to be a minimum of 0.4 mm. Therefore, adjust W and L accordingly.

Table 2. PCB Stack-up

Layer	Primary Side	Secondary Side
1	GND1	GND2
2	GND1	GND2
3	V_{CC1}	GND2 and stitching cap
4	GND1	GND2



$$Capacitance = \frac{\varepsilon o \times \varepsilon r \times W \times L}{D}$$

Figure 6. PCB stitching capacitance.

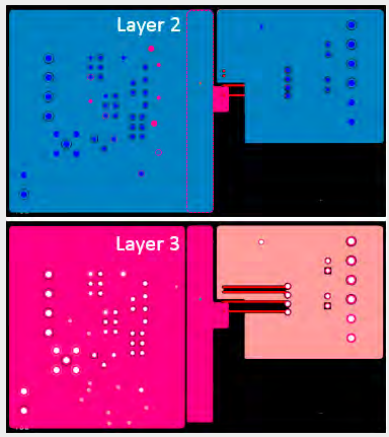


Figure 7. Embedded stitching capacitor.

- For further information on the 2-layer ADM2582E/ADM2587E, please visit analog.com/UG-916.
- For further information on the 4-layer ADM2582E/ADM2587E, please visit analog.com/UG-044.

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