

MAX5992A Evaluation Kit# (NQ84)
Initial Objective Specification Summary

Hardware IOS	<input checked="" type="checkbox"/> YES	<input type="checkbox"/> NO
Software IOS	<input type="checkbox"/> YES	<input checked="" type="checkbox"/> NO
Firmware IOS	<input type="checkbox"/> YES	<input checked="" type="checkbox"/> NO

Products: MAX5992A

Product Description: High Power PD Controller for 2x2 PD, Multiple-PD Redundancy and FTTB

Target Market: IEEE802.3af/at PoE Compliant Powered Devices, Fiber To The Building(FTTB), Outdoor Units

Personnel:

Business Unit	SPM	
Business Manager	Joe Chong	Sunnyvale 408-530-6258
Corp. App. Engineer	Gaoling Zou	Sunnyvale 408-530-6463
Design Engineer	Andrea Vigna	Italy 390382497140
EV Kit Engineer	Robert Brewer	Sunnyvale 408-530-6187
EV Kit Manager	Phill Leyva	Sunnyvale 408-530-6573

IC Status and EVKIT Quantity:

Estimated IC tape-out/PG date :	WW39	FY12
Estimated IC PP/BB parts date:	WW47	FY12
Estimated IC Intro date :	WW52	FY12
Hand Carry	N/A	N/A
First build EVKIT prototype Qty.	25 boards	RoHS Compliant
Additional prototype Qty.	0 boards	RoHS Compliant
EVKIT Production Qty.	25 boards	RoHS Compliant

EVKIT Description:

Name (silk screen)	MAX5992A EVALUATION KIT
Part Number	MAX5992AEVKIT#
Evaluates	MAX5992A
Number of Registers	0
Number of GPIO	0
Interface	N/A
Interface Platform	N/A

IC Information:

Product	MAX5992AETG+
Die Type	NQ84
Package Type	24-TQFN-EP(T2444+4)
Exposed Paddle	Yes

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Initial Objective Specification Summary

EVKIT Specifications:**Power Supply:**

Input Voltage Range	36V to 57V
Output Voltage/Output Current	12V/8A
PD Classification	Class 5 (~100W)
Converter Operating Frequency	300kHz

PCB Information:

Number of Layers	4
Copper Thickness	2 oz
Dielectric Type	FR4-08 or similar
Board Thickness	Standard (0.062")
IC Placement	Top-side/Bottom side
Controlled Impedance	Yes. 90 Ohm

PCB Layout Notes:

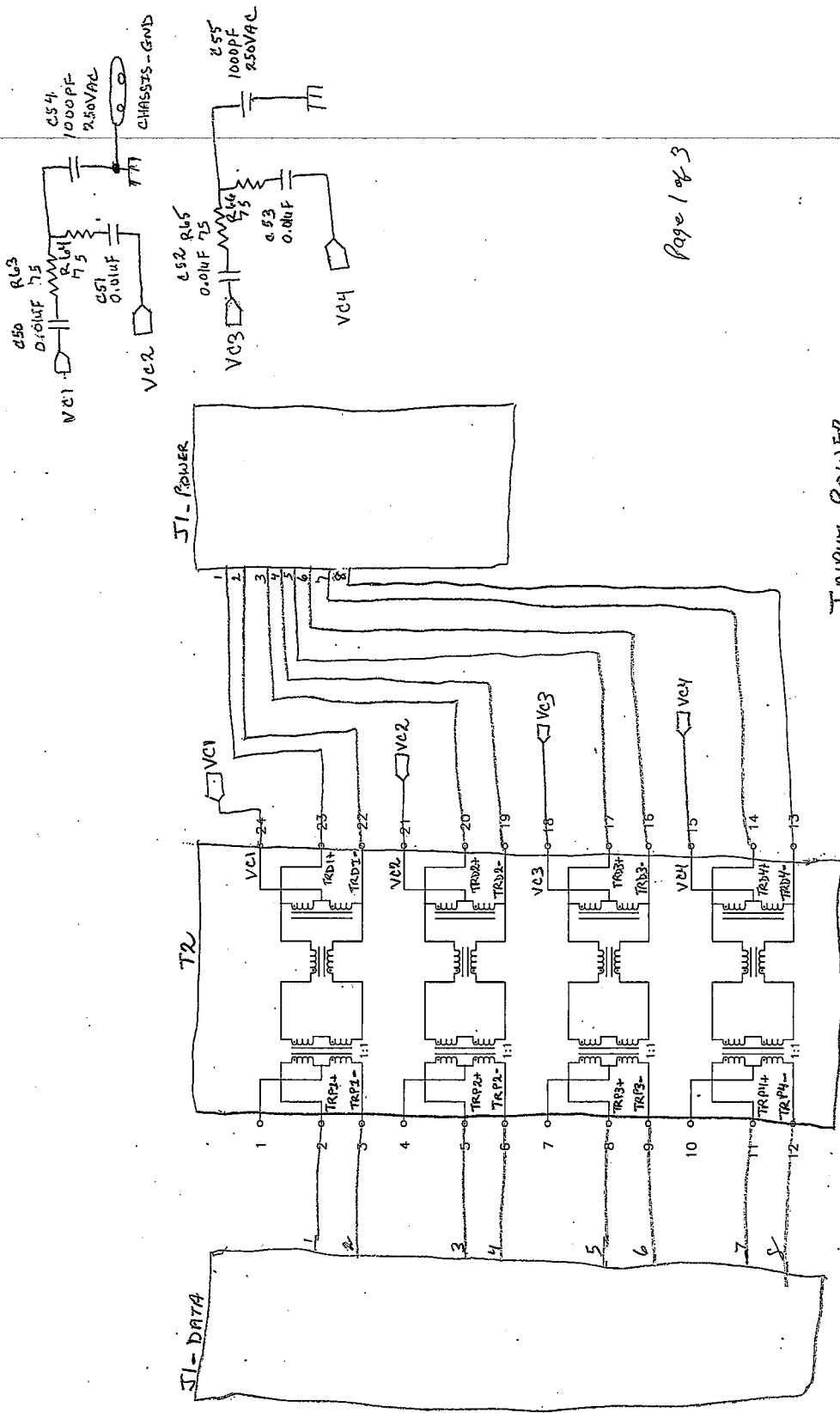
1. Layer 1 will be used for power, ground and signal routing.
2. Layer 2 will be used for the ground plane.
3. Layer 3 will be used for the power planes.
4. Layer 4 will be used for signal routing and additional copper required for thermal enhancement of the FETs, transformer, etc.

IOS Notes:

1. Ten (10) prototype boards will be built initially. After verification by the BU and EVKE, the remaining 15 prototype boards will be built.

Checklist:

BOM	Included Excel BOM
Schematics	Included
Software related documentation (timing diagrams, registers map, mock GUI...)	N/A
Firmware Description or Flow Chart	N/A
Approved IC Pin Out, Package and Code	Included
Pin Description	Included
Components data sheet (for new parts)	Included



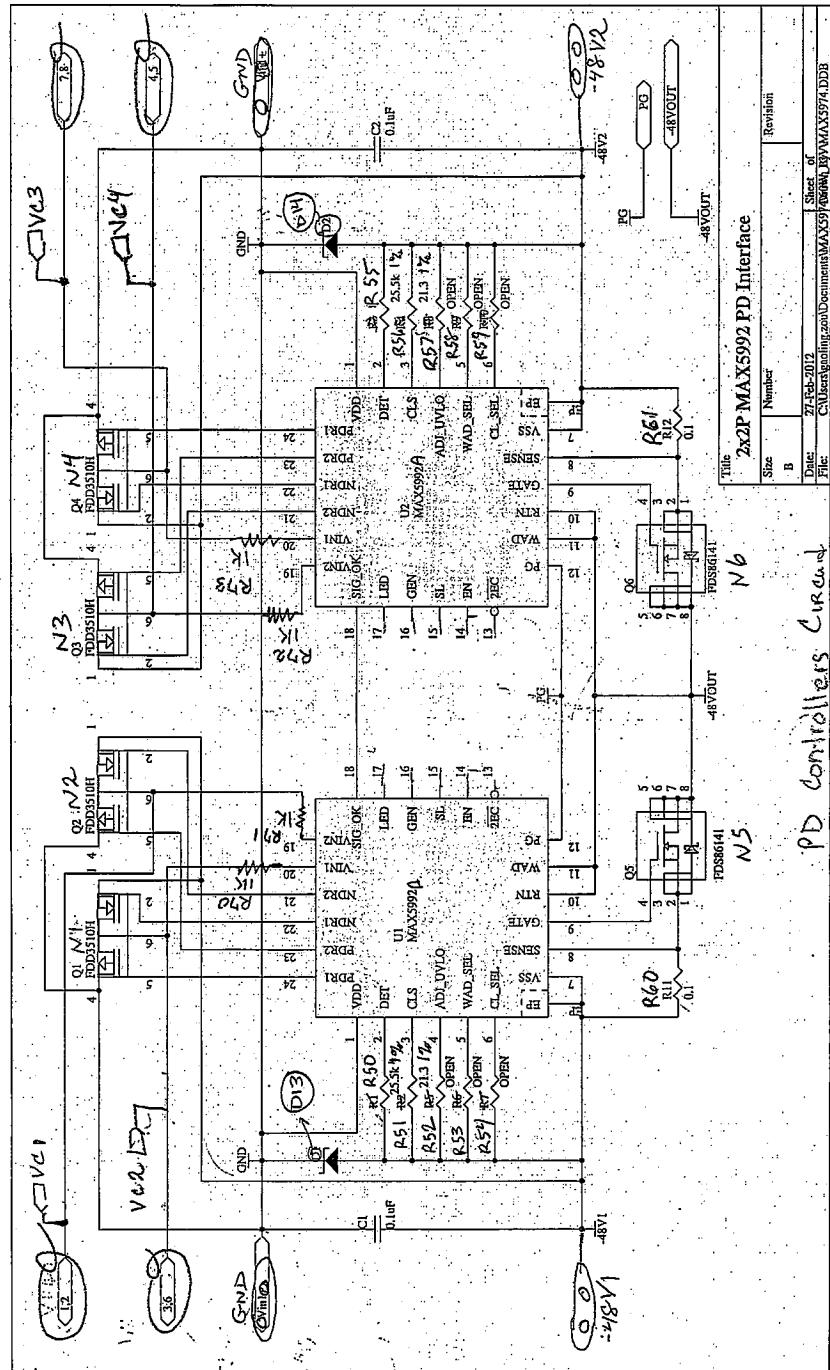
Page 1 of 3

INPUT POWER

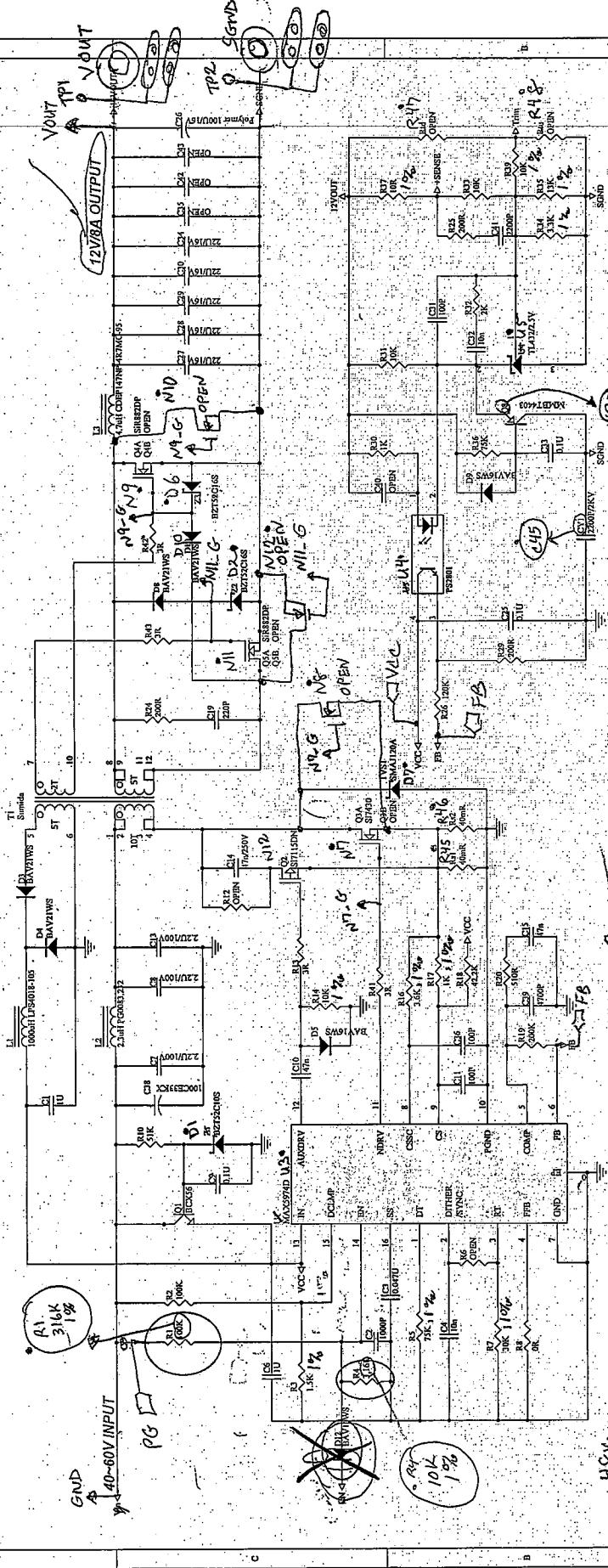
① Remove
part
numbers
from
schematics

Draw Dis/Div

Draw D13



- ① Remove all part numbers
 ② Change D1, D2, D3 to zener symbol



1. Push EN low to disable the output
2. Trim margin +/- 10% Vout
3. Adjust R1d to trim down the output
 $R1d = 10 * (Vadj - 2.5) / (2 * Vadj) * 10$
4. Adjust R1u to trim up the output
 $R1u = 25 * (Vadj - 1.2) / 10$

page 3 of 3

DC-DC Converter Circuit

MAX5992AEVKIT# : Rev P1, Omega sign translates to ? Mark when uploaded		35 characters		60 characters	
Parent Number	Item Component Description	QTY Per	Remarks	Manufacturer Part Number	
(Reference Designators)					
MAX5992AEVKIT#	0001 1uF 10% 16V X7R ceramic capacitor (0805)	1 C1	Murata GRM21BRZ71C105K		
	0001 1uF 10% 16V X7R ceramic capacitor (0805)	1 C1	TDK C2012X7R1C105K		
	0002 100pF 5% 50V C0G ceramic capacitor (0603)	4 C2, C11, C31, C36	Murata GRM1885C1H01J		
	0003 0.047uF 50V X7R ceramic capacitor (0603)	3 C3, C10, C15	Murata GRM188R71H473K		
	0004 0.01uF 50V X7R ceramic capacitor (0603)	2 C4, C32	Murata GRM188R71H03K		
	0005 1uF 10% 16V X7R ceramic capacitor (0603)	1 C6	Murata GRM188R71C105K		
	0005 1uF 10% 16V X7R ceramic capacitor (0603)	1 C6	TDK C1608X7R1C105K		
	0006 2.2uF 10% 100V ceramic capacitors (1210)	3 C7, C8, C13	TDK C3225X7R2A225K		
	0006 2.2uF 10% 100V ceramic capacitors (1210)	3 C7, C8, C13	Murata GRM32ER72A225K		
	0007 0.1uF 10% 50V X7R ceramic capacitors (0603)	3 C9, C25, C23	Murata GRM188R71H04K		
	0009 0.047uF 10% 250V X7R ceramic capacitor (1206)	1 C14	Murata GRM31CRZ72E473K		
	0009 0.047uF 10% 250V X7R ceramic capacitor (1206)	1 C14	TDK C316X7R2E473K		
	0010 220pF 10% 250V X7R ceramic capacitor (0603)	1 C19	Murata GRM188R72E221K		
	0011 100uF 16V Polymer tantalum capacitor	1 C26	SANYO 16TQCL001M		
	0011 100uF 16V Polymer tantalum capacitor	1 C26	KEMET T521D107M016ATE050		
	0012 22uF 10% 16V X5R ceramic capacitor (1206)	5 C27-C30, C34	Murata GRM31CRB1C226K		
	0013 33uF 100V aluminium electrolytic capacitor, (8.3mmx8.3mm)	1 C38	Panasonic EEE-FK2A330P		
	0014 4700pF 10% 50V X7R ceramic capacitor (0603)	1 C39	Murata GRM188R71H472K		
	0015 2200pF 10% 50V X7R ceramic cap 0603	1 C41	Murata GRM188R71H222K		
	0016 2200pF 2000V X7R ceramic cap 1808.	1 C45	JOHANSON 202R9W222KV4		
	0017 0.01uF 100V X7R ceramic capacitor (0805)	2 C50-C53	Murata GRM21BRZ72A103K		
	0018 1000pF 10% 250V X7R ceramic capacitor (1808)	2 C54, C55	Murata GA352QR71GF102K		
	0019 10V zener diode (SOD323)	1 D1	DIODES INC BZT52C10S-7-F		
	0020 16V zener diodes (SOD323)	2 D2, D6	DIODES INC BZT52C16S-7-F		
	0021 250V 200mA diode (SOD323)	4 D3, D4, D8, D10	DIODES INC BAV21WS-7-F		
	0022 75V 200mA diode (SOD323)	2 D5 D9	DIODES INC BAV16WS-7-F		
	0023 120V 400W TVS Diode	1 D7	DIODES INC SMAJ120A-13-F		
	0024 Transient Voltage Suppressor (SMB)	2 D13, D14	Tyco Electronics 5520252-4		
	0025 Modular Jack Assembly, Side Entry, 8 Position	2 J1_Data, J1_Power			
	0026 1000uH 100mA Inductor (4mm X 4mm)	1 L1	Coilcraft LPS4018-105ML_		
	0027 2.3uH 7A, Inductor (6.8mm X 6.8mm)	1 L2	Pulse PG0083-232		
	0028 4.7uH 15A, Inductor(4.9mm X 14.9mm)	1 L3	CDEP147NP-4R7MC-95		
	0029 80V 4.3A/2.8A N/P Channel MOSFETs (DPAK-4L)	4 N1-N4	Fairchild FDD3510H		
	0030 100V 7A N-channel MOSFET(SO-8)	2 N5, N6	Fairchild FDS8614J		
	0031 150V 7.2A N-channel MOSFET (Power Pak)	1 N7	VISHAY Si7430DP		
	0032 150V 7.2A N-channel MOSFET (Power Pak)	1 N7	Fairchild FDMS2572		
	0033 100V 17.6A N-channel MOSFET (PowerPak)	2 N9, N11	Vishay SIR882DP		
	0034 150V -1.9A P-channel MOSFET (PowerPak 1212-8)	1 N12	Vishay Si7115DN		
	0035 80V, 1A NPN transistor	1 Q1	Diodes Inc BCX56		
	0036 40V 600mA PNP transistor	1 Q2	DIODES INC MMBT4403-7-F		
	0037 316k Ohm +/-1% resistor (0805)	1 R1			
	0038 100k Ohm +/-1% resistor (0805)	1 R2			
	0039 1.5k Ohm +/-1% resistor (0603)	1 R3			

	0040	10k Ohm +/-1% resistor (0603)	1 R39
0041	75k Ohm +/-1% resistor (0603)	2 R5, R36	
0042	30k Ohm +/-1% resistor (0603)	1 R7	
0043	0 Ohm +/-5% resistor (0603)	1 R8	
0044	51K +/-1% resistor (0805)	1 R10	
0045	3 Ohm +/-1% resistor (0603)	4 R13, R41, R42, R43	
0047	3.6k Ohm +/-1% resistor (0603)	1 R16	
0048	1k Ohm +/-1% resistors (0603)	2 R17, R30	
0049	42.2K +/-1% resistor (0603)	1 R18	
0050	200K +/-1% resistor (0603)	1 R19	
0051	510 Ohm +/-1% resistor (0603)	1 R20	
0052	200 Ohm +/-1% resistor (1206)	1 R24	
0053	200 Ohm +/-1% resistors (0603)	2 R25, R29	
0054	120k Ohm +/-1% resistor (0603)	1 R26	
0055	2k Ohm +/-1% resistor (0603)	1 R32	
0056	3.3k Ohm +/-1% resistor (0603)	1 R34	
0057	13k Ohm +/-1% resistor (0603)	1 R35	
0058	10 Ohm +/-1% resistor (0603)	1 R37	
0059	40m Ohm +/-1% resistors (1206)	2 R45, R46	
0060	25.5k Ohm 1% resistors (0603)	2 R50, R55	
0061	21.3 Ohm +/-1% resistor (0805)	2 R51, R56	
0062	0.1 Ohm 1% 1/4W (1206)	2 R60, R61	
0063	75 Ohm 5% resistor (0805)	4 R63, R66	
0064	1k Ohm 5% resistors (0603)	4 R70-R73	
0065	Non-Insulated banana jack	2 SGND, VOUT	
0066	Transformer 10:5:5:2 (EFD25)	1 T1	
0067	LAN Transformer	1 T2	
0068	Red Test Point	1 TP1	
0069	Black test Point	1 TP2	
0070	High Power PD Controller (24 TQFN-EP)	2 U1, U2	
0071	Active Clamped, Current Mode PWM controller 16 TQFN-EP)	1 U3	
0072	OPTOCOUPLER (4 SSOP)	1 U4	
0073	2.5V Voltage reference (SOT-23)	1 U5	
0074	PC BOARD: MAX5992 Evaluation Kit	TI TL432VIDBZ	
	Not Installed ceramic capacitors (0603)	0 C35, C40, C42, C43	
	Not installed Mosfets (PowerPaks)	0 N8, N10, N12	
	Not installed, resistors (0603)	0 R6, R12, R47, R48	
		R52, R53, R54, R57	
		R58, R59	
0075	BOX, BROWN 9 3/16" x 7" x 7/8"		
0076	Label		
0077	WEB Instructions for Maxim Data Sheet		
0078	BAG, STATIC SHIELD ZIP 4" x 6", W/ESD LOGO		
0079	FOAM, ANTI-STATIC PE 12" x 12" x 5MM		
	Revision History		

Rev P1 3/14/12: Initial Prototype BOM

~~DE~~ Pin-Out Approval
DE

Robert Brewer

From: Andrea Vigna
Sent: Wednesday, March 14, 2012 3:40 AM
To: Robert Brewer
Subject: Re: MAX5992A Pin-Out Verification (Approval Within Next few Hours)

Hi Robert,

I approve.

Regards

Andrea

Robert Brewer wrote:

Andrea,

Attached is a copy of the MAX5992A IC pin-out verification. Please send email approval within the next few hours. Thanks.

Robert Brewer

Member of Technical Staff

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MAX5992A Evaluation Kit# (NQ84)
Initial Objective Specification Summary

ICs Pin Out, Package and Code:

MAX5992A (NQ84)

IC Pin-Out, Package and Code Confirmation:

Please confirm the following:

- IC PINOUT is CORRECT.
- IC PACKAGE is 24 TQFN-EP
- IC PACKAGE CODE is T2444+4

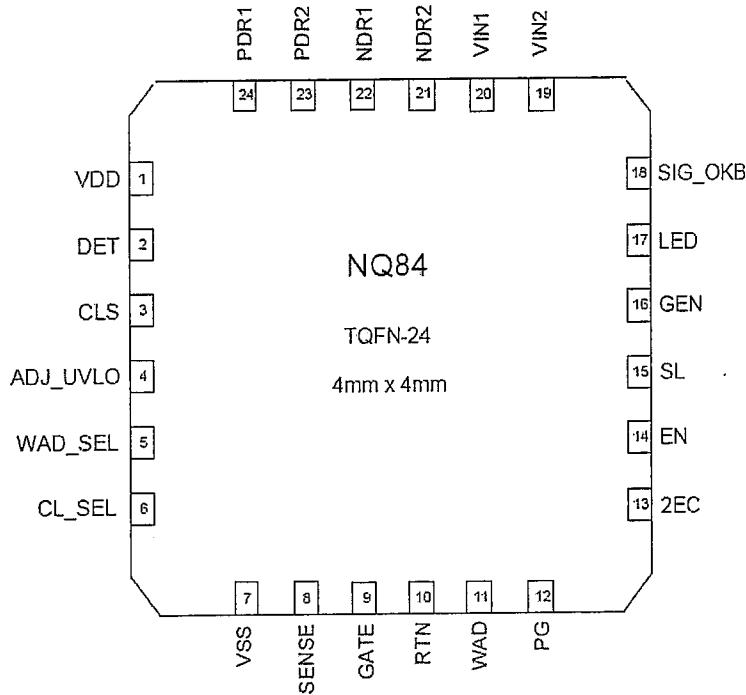
DE SIGNATURE:

Date:

Email Approval:

Date:

Pin Configuration



Pin Description

MAX5992A Evaluation Kit# (NQ84)
Initial Objective Specification Summary

PIN	NAME	FUNCTION
1	VDD	Positive Supply Input. Connect a 68nF (min) bypass capacitor between VDD and VSS.
2	DET	Detection Resistor Input. Connect a signature resistor ($R_{DET} = 24.9k\Omega$) from DET to VSS.
3	CLS	Classification Resistor Input. Connect a 1% resistor (R_{CLS}) from CLS to VSS to set the desired classification current. See the classification current specifications in the Electrical Characteristics table to find the resistor value for a particular PD classification.
4	ADJ_UVLO	UVLO Select Input. Leave this pin floating to set the PoE UVLO threshold, connect to VSS to set the Industrial UVLO threshold (see EC Table for details).
5	WAD_SEL	WAD Behavior Select Input. Leave WAD_SEL pin floating to be always powered from WAD when an Adaptor is detected at WAD input. Pull down this pin to VSS to be powered from WAD only when Adaptor voltage is higher than PoE voltage.
6	CL_SEL	Power on Current Limit Select Input. Leave this pin floating to set the 800mA current limit, connect to VSS to set the 1.9A current limit (see EC Table for details).
7	VSS	Negative Supply Input.
8	SENSE	Current Sense Input. Connect SENSE to the source of the external isolation MOSFET. Place a 180mOhm sense resistor between this pin and VSS.
9	GATE	Isolation FET Gate Control Output. Connect GATE to the gate of the external isolation MOSFET.
10	RTN	Drain Sense Input. Connect RTN to the drain of the external isolation MOSFET. RTN is connected to an isolation diode when NQ84 is used in Redundancy/FTTB application. It is directly connected to the downstream DC-DC converter ground in all other cases. See application diagrams.
11	WAD	Wall Power Adaptor Detector Input. Wall adapter detection is enabled when VIN crosses the mark event threshold. Detection occurs when the voltage from WAD to RTN is greater than 8V. When a wall power adaptor is detected, the isolation MOSFET turns off (unless WAD_SEL is forced low) and 2EC current sink turns on. Connect WAD directly to RTN when the wall power adaptor or other auxiliary power source is not used.
12	PG	Open-Drain Power-Good Indicator Output. It is referred to VDD. It is used to drive the DC-DC enable pin. See the application circuit below for details.
13	2EC	2-Event Classification Detector/Wall Adaptor Detect Output. A 1.5mA current sink is enabled at 2EC when a Type 2 PSE or a wall adaptor is detected. When powered by a Type 2 PSE, the 2EC current sink is enabled after the isolation MOSFET is fully on until VIN drops below the UVLO threshold. 2EC is latched when powered by a Type 2 PSE until VIN drops below the reset threshold. 2EC also asserts when a wall adaptor supply is applied between WAD and RTN. 2EC is not latched if asserted by WAD. The 2EC current sink is turned off when the device is in sleep and green modes.
14	EN	Inrush Behavior Select Input. By leaving the pin floating, NQ84 is set for non-redundancy case. When the pin is pulled down to VSS, NQ84 is set for redundancy/FTTB application.

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15	SL	Sleep Mode Enable Input/Wake Input. Referred to VSS. A falling edge on SL (or a 5s period below the threshold if trim option is selected) brings the device into sleep mode (VSL must drop below 0.75V). An external resistor (RSL) connected between SL and VSS sets the LED current (ILED). SL can be used in combination with GEN as wake pin. Once the part is in sleep/green mode, a falling edge on GEN while SL is asserted low brings the device back to normal operating mode (wake mode).
16	GEN	Green Mode Enable Input. Referred to VSS. GEN can be used in combination with SL to enter green mode. A falling edge on SL for a 5s period below the threshold if trim option is selected) while GEN is asserted low enables green mode. In wake mode GEN can act as LED driver. In this case only 60K resistor on SL pin is allowed.
17	LED	LED Driver Output. During sleep and green mode, LED sources a periodic current (ILED) at 250Hz frequency with 25% duty cycle. The amplitude of LED is set by RSL according to the formula ILED (in A) = 645.75/(RSL + 1200).
18	SIG_OKB	I/O pin SIG_OKB is internally held high to VDD until UVLO is released. When SIG_OKB goes below the threshold (w.r.t. VSS) the isolation FET is turned on and Inrush mode is entered. Connect this pin to the SIG_OKB of another INQ84 working in 2x2P configuration. Leave it floating in any other application.
19	VIN2	Bridge Input 2. Connect VIN2 to bridge inputs from RJ45 connector. If V(VIN2)<V(VIN1), VIN2 is used to provide current pulses to PSE when Maintain Power Signature is enabled.
20	VIN1	Bridge Input 1. Connect VIN1 to bridge inputs from RJ45 connector. If V(VIN1)<V(VIN2), VIN1 is used to provide current pulses to PSE when Maintain Power Signature is enabled.
21	NDR2	Active Bridge NFET2 Gate Control Output. Connect NDR2 to the gate of the NFET2 in active bridge.
22	NDR1	Active Bridge NFET1 Gate Control Output. Connect NDR1 to the gate of the NFET1 in active bridge.
23	PDR2	Active Bridge PFET2 Gate Control Output. Connect PDR2 to the gate of the PFET2 in active bridge.
24	PDR1	Active Bridge PFET1 Gate Control Output. Connect PDR1 to the gate of the PFET1 in active bridge.
-	EP	Exposed Pad. Do not use EP as an electrical connection to VSS. EP is internally connected to VSS through a resistive path and must be connected to VSS externally. To optimize power dissipation, solder the exposed pad to a large copper power plane.

Rev P1 3/14/12: Initial Prototype BOM

Surface
mount type

TQC Series

Update

RoHS compliance

High voltage

TQC series is perfect for high voltage, low ESR and low profile applications.
 It is most suitable to be used as a bypass capacitor on a 12V motor driver
 or on the input side of a DC/DC converter.

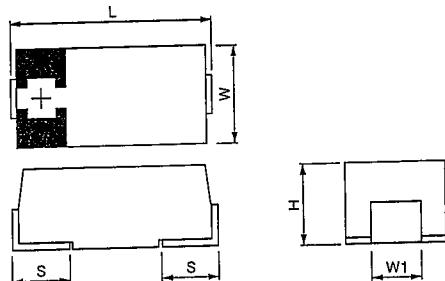


C26

Specifications

Test Item / Specification	Condition	Specifications			
Rated voltage (V)	—	16	20	25	35
Surge voltage (V)	—	20	23	29	40
Category, temperature range (C)	—	-55 to +105			
Capacitance tolerance (%)	120Hz/20°C	M: ±20			
Rated capacitance range (μF)	120Hz/20°C	5.6 to 100			
Dissipation Factor (DF)	120Hz/20°C	Please see the attached characteristics list			
Leakage current	Rated voltage applied, after 5 minutes	Please see the attached characteristics list			
Equivalent series resistance (ESR)	100kHz/20°C	Please see the attached characteristics list			
Characteristics of impedance ratio at high temp. and low temp.	100kHz/+20°C -55°C Z/20°C +105°C Z/20°C	0.6 to 1.0			
Endurance	105°C, 2,000h Rated voltage applied	ΔC/C	Within ±20% of the initial value		
		DF	Within 1.5 times of the initial limit		
		LC	Within the initial limit		
Damp heat (Steady State)	60°C, 90 to 95%RH, 500h No applied voltage	ΔC/C	Within +40%, -20% of the initial value		
		DF	Within 1.5 times of the initial limit		
		LC	Within 3 times of the initial limit		
Surge	15 to 35°C, 1,000 cycles, 1kΩ discharge resistance, surge voltage applied	ΔC/C	Within ±5% of the initial value		
		DF	Within the initial limit		
		LC	Within 3 times of the initial limit		

Dimensions



Size code	(unit: mm)				
	H=0.2±0.1	H=0.2±0.2	H=0.1±0.1	H=0.2±0.2	W=0.2±0.1
B2	3.5	2.8	1.9	0.8	2.2
D2	7.3	4.3	1.9	1.3	2.4
D3L	7.3	4.3	2.8	1.3	2.4
D3	7.3	4.3	3.1	1.3	2.4

*1 ±0.3:D3L *2 ±0.2:D3LD3

Size list

	RV : Rated voltage	16V	20V	25V	35V
5.6			B2		
8.2		B2			
10	B2			D2	
115	B2			D2	
22		D2	D2		
33	D2		D2		
47	D2	D2			
68	D2				
100	D2,D3				
150	D3L				

● TQC series characteristics list

Size code	Part number	Rated voltage (V)	Rated temperature (°C)	Rated capacitance (nF)	Category voltares	Category temperature (°C)	Capacitance (pF) max.	ESR (mΩ) max./min.	ESR (mΩ) 100kHz/200kHz	ESR (mΩ) 100kHz/200kHz	ESR (mΩ) 100kHz/200kHz	ESR (mΩ) 100kHz/200kHz	ESR (mΩ) 100kHz/200kHz
B2	25TQC5R6M	25	105	5.6	25	105	10.0	42.0	100	800	—	—	3
	20TQC8R2M	20	105	8.2	20	105	10.0	49.2	100	800	—	—	3
	16TQC15M	16	105	15	16	105	10.0	72.0	90	1000	—	—	3
	16TQC10M	16	105	10	16	105	10.0	48.0	100	800	—	—	3
D2	35TQC10M	35	105	10	35	105	10.0	35.0	120	1000	—	—	3
	25TQC33MYF	25	105	33	25	105	10.0	82.5	60	1400	—	—	3
	25TQC22M	25	105	22	25	105	10.0	55.0	90	1000*2	—	—	3
	25TQC22MV	25	105	22	25	105	10.0	55.0	45	1500*2	—	—	3
	25TQC15M	25	105	15	25	105	10.0	38.0	90	1000*2	—	—	3
	25TQC15MV	25	105	15	25	105	10.0	38.0	45	1500*2	—	—	3
	20TQC47MYF	20	105	47	20	105	10.0	94.0	55	1450	—	—	3
	20TQC22M	20	105	22	20	105	10.0	44.0	80	1300	—	—	3
	16TQC100MYF	16	105	100	16	105	10.0	160.0	50	1500	—	—	3
	16TQC68MYF	16	105	68	16	105	10.0	108.8	50	1500	—	—	3
D3	16TQC47M	16	105	47	16	105	10.0	75.2	70	1400	—	—	3
	16TQC47MW	16	105	47	16	105	10.0	75.2	40	1800	—	—	3
	16TQC33M	16	105	33	16	105	10.0	52.8	70	1400	—	—	3
	16TQC150MYF	16	105	150	16	105	10.0	240.0	50	1800	—	—	3
D3	16TQC100M	16	105	100	16	105	10.0	160.0	50	1800	—	—	3

*1 100k to 500kHz,105°C *2 100k to 300kHz,105°C

POSCAP

25S6P
25S8P
25S10P
25S12P
25S15P
25S18P
25S22P
25S25P
25S33P
25S47P
25S68P
25S100P
25S150P

Base system
Insulation
Imaging
Case size
Case style
Case color
Exclusion of
corner numbers
Packing
Specifications

Technical data
Dimensions
Recommended
lead pattern
dimensions
Recommended
soldering
technique
Fundamental
structure
Characteristics
Reliability

TPU
TPH
TPG
TPSF
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TPA
TPB
TPC
TPD
TPF
TPG
TPH
TPU
TPA
TPB
TPC
TPD
TPF
TPG
TPH
TPU

107

※ Red letters : New models

TQC

Surface Mount Type

Series: FK Type : V

■ Features

Endurance: 2000 to 5000h at 105°C
 Low impedance (40 to 60% less than FC series)
 Miniaturized(30 to 50% less than FC series)
 Vibration-proof product is available upon request.(Φ8 ≤)
 RoHS directive compliant(Parts No:EEV* Φ12.5 ≤,EEE*)



■ Specifications

Category temp. range	-55 to +105°C									
Rated W.V. Range	6.3 to 100V DC									
Nominal Cap. Range	3.3 to 6800 μF									
Capacitance Tolerance	±20 % (120Hz/+20°C)									
DC Leakage Current	I ≤ 0.01CV or 3(μA) After 2 minutes application of rated working voltage at +20°C. (Whichever is greater)									
tan δ	Please see the attached standard products list									
Characteristics at Low Temperature	W.V. (V)	6.3	10	16	25	35	50	63	80	100
	Z(-25°C) / Z(+20°C)	2	2	2	2	2	2	2	2	2
	Z(-40°C) / Z(+20°C)	3	3	3	3	3	3	3	3	3
	Z(-55°C) / Z(+20°C)	4	4	4	3	3	3	3	3	3

(Impedance ratio
at 120 Hz)

After applying rated working voltage at +105±2°C for 2000 hours (≥dia.12.5 and suffix "G" in dia.8 to 10 are 5000 hours) the capacitors shall meet the limits specified below. Post-test requirement at +20°C.

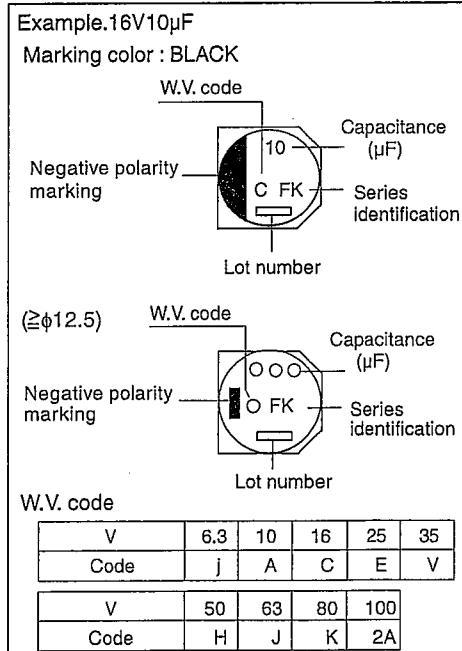
Capacitance change	±30% of initial measured value (Suffix "G" is 35%)
tan δ	≤200 % of initial specified value (Suffix "G" is 300%)
DC leakage current	≤initial specified value

After storage for 1000 hours at +105±2 °C with no voltage applied and then being stabilized at +20°C, capacitors shall meet the limits specified in Endurance(With voltage treatment)

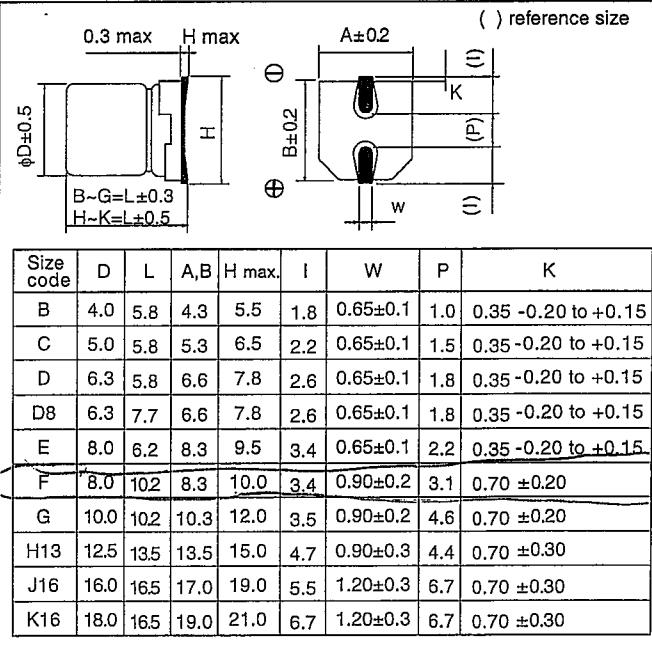
After reflow soldering (Refer to page 86 for recommended temperature profile) and then being stabilized at +20°C, capacitor shall meet the following limits.

Capacitance change	±10% of initial measured value
tan δ	≤initial specified value
DC leakage current	≤initial specified value

■ Marking



■ Dimensions in mm (not to scale)



■ Case size VS. Capacitance, Impedance and Ripple current

Impedance; (Ω /100kHz,+20°C),
Ripple current; (mA·r.m.s./100kHz+105°C)

Capacitance (μ F)	W.V.			6.3			10			16		
	Size	Impedance	Ripple current	Size	Impedance	Ripple current	Size	Impedance	Ripple current	Size	Impedance	Ripple current
10				B	1.35	90	C(B)	0.7(1.35)	160(90)	B	1.35	90
22	B	1.35	90	C(B)	0.7(1.35)	160(90)	D(C)	0.36(0.7)	240(160)			
33							D	0.36	240			
47	C(B)	0.7(1.35)	160(90)				D	0.36	240			
68							E	0.26	300	E	0.26	300
100	D(C)	0.36(0.7)	240(160)	D	0.36	240	D8	0.34	280			
150				D8	0.34	280	D8	0.34	280			
220	D	0.36	240	E	0.26	300	OF	0.16	600			
330	D8	0.34	280	OF	0.16	600						
	E	0.26	300									
470	OF	0.16	600	OF	0.16	600	OF	0.16	600			
680				OF	0.16	600	OG	0.08	850			
1000	OF	0.16	600	OG	0.08	850	H13	0.06	1100			
1500	OG	0.08	850				J16	0.035	1800			
2200				H13	0.06	1100	K16	0.033	2060			
3300	H13	0.06	1100									
4700				J16	0.035	1800	J16	0.035	1800			
6800	J16	0.035	1800	K16	0.033	2060						
Capacitance (μ F)	W.V.			25			35			50		
	Size	Impedance	Ripple current	Size	Impedance	Ripple current	Size	Impedance	Ripple current	Size	Impedance	Ripple current
4.7				B	1.35	90	D(C)	0.88(1.52)	165(85)	B	2.9	60
10	B	1.35	90	C(B)	0.7(1.35)	160(90)	D8	0.88	165			
22	C	0.7	160	C	0.7	160	D	0.88	165			
33	D(C)	0.36(0.7)	240(160)	D	0.36	240	D8	0.68	195			
							E	0.68	195			
47	D	0.36	240	D	0.36	240	E(D8)	0.68	195			
68	D	0.36	240	D8	0.34	280						
100	D8	0.34	280	D8	0.34	280	OF	0.34	350			
	E	0.26	300	OF	0.16	600						
150	OF	0.16	600	OF	0.16	600	OG	0.18	670			
220	OF	0.16	600	OF	0.16	600	OG	0.18	670			
330	OF	0.16	600	OG	0.08	850	H13	0.12	900			
390							H13	0.12	900			
470	OG	0.08	850	H13	0.06	1100	J16	0.073	1610			
680				H13	0.06	1100	J16	0.073	1610			
1000	H13	0.06	1100	J16	0.035	1800	J16	0.073	1610			
1500				J16	0.035	1800						
2200	J16	0.035	1800									
3300	K16	0.033	2060									
Capacitance (μ F)	W.V.			63			80			100		
	Size	Impedance	Ripple current	Size	Impedance	Ripple current	Size	Impedance	Ripple current	Size	Impedance	Ripple current
3.3				C	5	25						
4.7	C	3	50	D	3	40						
10	D	1.5	80	D8	2.4	60						
				E	2.4	60						
22	D8	1.2	120	F	1.3	130	F	1.3	130			
	E	1.2	120	F	1.3	130						
33	F	0.65	250	F	1.3	130	G	0.7	200			
	F	0.65	250	G	0.7	200	H13	0.32	500			
47	F	0.65	250	H13	0.32	500	H13	0.32	500			
68	F	0.65	250	H13	0.32	500	J16	0.17	793			
100	G	0.35	400	H13	0.32	500	J16	0.17	793			
150	H13	0.16	800	H13	0.32	500	J16	0.17	793			
220	H13	0.16	800				K16	0.153	917			
330				J16	0.17	793	K16	0.153	917			
470	J16	0.082	1410	K16	0.153	917						
680	K16	0.080	1690									

(); Miniaturization type ©Life time 5000h available upon request(suffix : G)

Design and specifications are subject to change without notice. Ask factory for technical specifications before purchase and/or use.
Whenever a doubt about safety arises from this product, please contact us immediately for technical consultation.

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■ Standard Products

W.V. (V)	Cap. (±20%) (μF)	Case size			Specification			Part No. (RoHS: not compliant)	Reflow R	Part No. (RoHS: compliant)	Min. Packaging Q'ty	
		Dia. (mm)	Length (mm)	Size Code	Ripple current (100kHz +105°C) (mA)	Impedance (100kHz +20°C) (Ω)	tan δ (120Hz +20°C)					
63	4.7	5	5.8	C	50	3.0	0.08	EEVFK1J4R7R	(1)	EEEFK1J4R7R	(4)	1000
	10	6.3	5.8	D	80	1.5	0.08	EEVFK1J100P	(1)	EEEFK1J100P	(4)	1000
	22	6.3	7.7	D8	120	1.2	0.08	EEVFK1J220XP	(1)	EEEFK1J220XP	(4)	900
		8	6.2	E	120	1.2	0.08	EEVFK1J220P	(2)	EEEFK1J220P	(5)	1000
	33	8	10.2	F	250	0.65	0.08	EEVFK1J330P	(2)	EEEFK1J330P	(5)	500
	47	8	10.2	F	250	0.65	0.08	EEVFK1J470P	(2)	EEEFK1J470P	(5)	500
	68	8	10.2	F	250	0.65	0.08	EEVFK1J680UP	(2)	EEEFK1J680UP	(5)	500
	100	10	10.2	G	400	0.35	0.08	EEVFK1J101P	(2)	EEEFK1J101P	(5)	500
	150	12.5	13.5	H13	800	0.16	0.08			EEVFK1J151Q	(2)	200
	220	12.5	13.5	H13	800	0.16	0.08			EEVFK1J221Q	(2)	200
	470	16	16.5	J16	1410	0.082	0.08			EEVFK1J471M	(2)	125
	680	18	16.5	K16	1690	0.08	0.08			EEVFK1J681M	(2)	125
80	3.3	5	5.8	C	25	5.0	0.08	EEVFK1K3R3R	(1)	EEEFK1K3R3R	(4)	1000
	4.7	6.3	5.8	D	40	3.0	0.08	EEVFK1K4R7P	(1)	EEEFK1K4R7P	(4)	1000
	10	6.3	7.7	D8	60	2.4	0.08	EEVFK1K100XP	(1)	EEEFK1K100XP	(4)	900
		8	6.2	E	60	2.4	0.08	EEVFK1K100P	(2)	EEEFK1K100P	(5)	1000
	22	8	10.2	F	130	1.3	0.08	EEVFK1K220P	(2)	EEEFK1K220P	(5)	500
	33	8	10.2	F	130	1.3	0.08	EEVFK1K330P	(2)	EEEFK1K330P	(5)	500
	47	10	10.2	G	200	0.7	0.08	EEVFK1K470P	(2)	EEEFK1K470P	(5)	500
	68	12.5	13.5	H13	500	0.32	0.08			EEVFK1K680Q	(2)	200
	100	12.5	13.5	H13	500	0.32	0.08			EEVFK1K101Q	(2)	200
	150	12.5	13.5	H13	500	0.32	0.08			EEVFK1K151Q	(2)	200
	330	16	16.5	J16	793	0.17	0.08			EEVFK1K331M	(2)	125
	470	18	16.5	K16	917	0.153	0.08			EEVFK1K471M	(2)	125
100	22	8.0	10.2	F	130	1.3	0.07	EEVFK2A220P	(2)	EEEFK2A220P	(5)	500
	33	10	10.2	G	200	0.7	0.07	EEVFK2A330P	(2)	EEEFK2A330P	(5)	500
	47	12.5	13.5	H13	500	0.32	0.07			EEVFK2A470Q	(2)	200
	68	12.5	13.5	H13	500	0.32	0.07			EEVFK2A680Q	(2)	200
	100	16	16.5	J16	793	0.17	0.07			EEVFK2A101M	(2)	125
	150	16	16.5	J16	793	0.17	0.07			EEVFK2A151M	(2)	125
	220	18	16.5	K16	917	0.153	0.07			EEVFK2A221M	(2)	125
	330	18	16.5	K16	917	0.153	0.07			EEVFK2A331M	(2)	125

An explanation of the taping dimensions can be found on page 84.

Reflow profiles can be found on page 86.

Endurance: 105°C 2000h - 5000h

■ Frequency Correction Factor of Rated Ripple Current

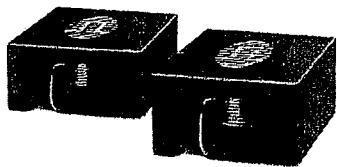
	Frequency (Hz)				
	50,60	120	1k	10k	100k~
coefficient	0.70	0.75	0.90	0.95	1.00

SMT POWER INDUCTORS

Flat Coils - PG0083 Series



Pulse®
A TECHNITROL COMPANY



- Height: 4.2mm Max
- Footprint: 6.8mm x 6.8mm Max
- Current Rating: up to 17.5A
- Inductance Range: 0.32μH to 3.76μH

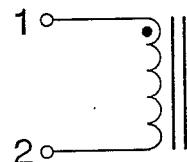
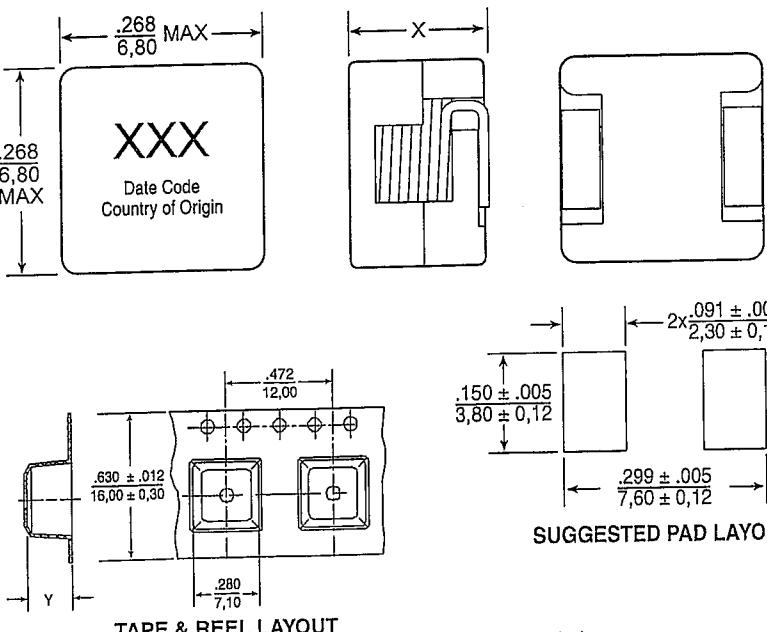
Electrical Specifications @ 25°C — Operating Temperature -40°C to +95°C¹

Part ⁸ Number	Inductance @I _{rated} ² (μH TYP)	I _{rated} ³ (A)	DCR (mΩ)		Inductance @0A _{dc} (μH ±25%)	Saturation ⁴ Current I _{SAT} (A)	Heating ⁵ Current I _{HC} (A)	Core Loss ⁶ Factor	
			TYP	MAX				(K1)	(K2)
PG0083.401	0.32	17.5	3.0	3.2	0.40	27	17.5	2.25E-10	85.4
PG0083.601	0.48	15	4.5	4.8	0.60	21	15	2.25E-10	99.7
PG0083.102	0.80	12	6.6	7.2	1.0	17	12	2.25E-10	135.9
PG0083.182	1.44	8.0	15.6	16.0	1.8	13	8.0	2.25E-10	179.4
PG0083.232	1.84	7.0	17.5	18.0	2.3	11.5	7.5	2.25E-10	202.2
PG0083.332	2.64	5.5	26.6	27.5	3.3	9.5	5.8	2.25E-10	234.9
PG0083.472	3.76	4.5	36.6	38.0	4.7	8.0	4.5	2.25E-10	281.1

NOTE: To order RoHS compliant part, add the suffix "NL" to the part number (i.e. PG0083.401 becomes PG0083.401NL and PG0083.401T becomes PG0083.401NLT).

Mechanical

Schematic



Part No.	Max. Height "X" (in./mm)
PG0083.401	.165/4,20
PG0083.601	.165/4,20
PG0083.102	.165/4,20
PG0083.182	.157/4,00
PG0083.232	.157/4,00
PG0083.332	.157/4,00
PG0083.472	.157/4,00

Dimensions: Inches
mm
Unless otherwise specified, all tolerances are $\pm .010$
 $.025$

Weight.....1.0 grams
Tape & Reel1000/reel
T&R Height0.189/4,80
("Y" - in./mm)

SMT POWER INDUCTORS

Flat Coils - PG0083 Series



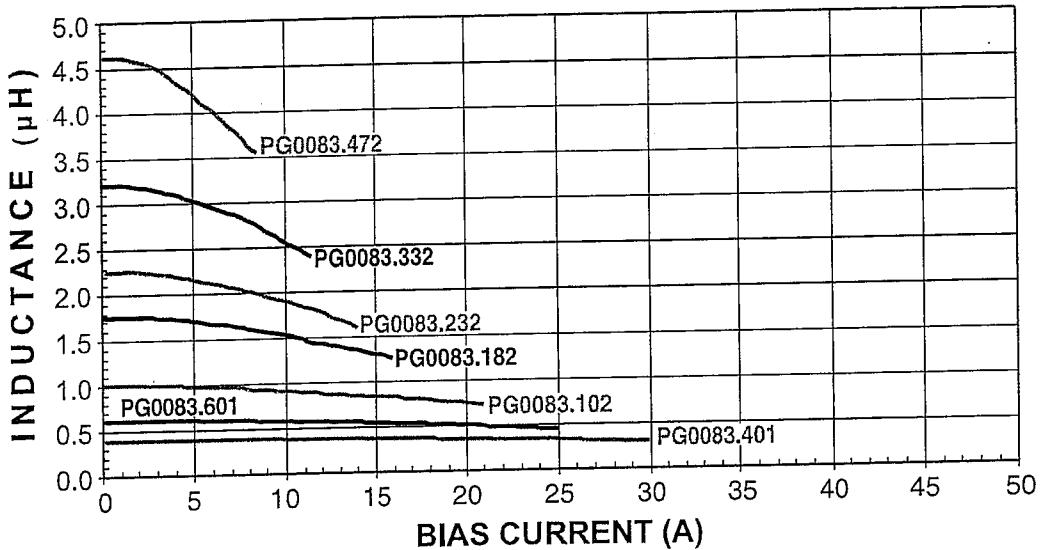
Notes from Tables

1. The temperature of the component (ambient plus temperature rise) must be within the specified operating temperature range.
2. Inductance at Irated is a typical inductance value for the component taken at rated current.
3. The rated current listed is the lower of the saturation current @ 25°C or the heating current.
4. The saturation current, Isat, is the current at which the component inductance drops by 20% (typical) at an ambient temperature of 25°C. This current is determined by placing the component in the specified ambient environment and applying a short duration pulse current (to eliminate self-heating effects) to the component.
5. The heating current, Ibc, is the DC current required to raise the component temperature by approximately 40°C. The heating current is determined by mounting the component on a typical PCB and applying current for 30 minutes. The temperature is measured by placing the thermocouple on top of the unit under test. Take note that the component's performance varies depending on the system condition. It is suggested that the component be tested at the system level, to verify the temperature rise of the component during system operation.
6. Core loss approximation is based on published core data:

$$\text{Core Loss} = K1 * (f)^{1.035} * (K2\Delta I)^{2.263}$$

Where: Core Loss = in Watts
 f = switching frequency in kHz
 $K1$ & $K2$ = core loss factors
 ΔI = delta I across the component in Ampere
 $K2\Delta I$ = one half of the peak to peak flux density across the component in Gauss
7. Unless otherwise specified, all testing is made at 100kHz, 0.1VAC.
8. Optional Tape & Reel packaging can be ordered by adding a "T" suffix to the part number (i.e. PG0083.472 becomes PG0083.472T). Pulse complies to industry standard tape and reel specification EIA481.

Inductance vs Current Characteristics





SMAJ5.0(C)A – SMAJ200(C)A

400W SURFACE-MOUNT TRANSIENT-VOLTAGE SUPPRESSOR

D7

Features

- 400W Peak Pulse Power Dissipation
- Glass Passivated Die Construction
- Unidirectional and Bidirectional Versions Available
- Excellent Clamping Capability
- Fast Response Time
- Lead Free Finish/RoHS Compliant (Note 1)
- Green Molding Compound (No Halogen and Antimony) (Note 2)

Mechanical Data

- Case: SMA
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Lead Free Plating (Matte Tin Finish). Solderable per MIL-STD-202, Method 208
- Polarity Indicator: Cathode Band (Note: Bi-directional devices have no polarity indicator.)
- Weight: 0.064 grams (approximate)



Top View



Bottom View

Ordering Information (Note 3)

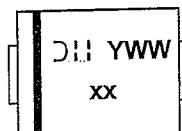
Part Number	Case	Packaging
SMAJXXX(C)A-13-F	SMA	5000/Tape & Reel

*x = Device Voltage, e.g., SMCJ170A-13-F. Example: SMAJ170A-13-F.

Notes:

1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied, see EU Directive 2002/95/EC Annex Notes
2. Product manufactured with Date Code 0924 (week 24, 2009) and newer are built with Green Molding Compound.
3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



xx = Product type marking code
 (See Electrical Characteristics Table)
 DII = Manufacturers' code marking
 YWW = Date code marking
 Y = Last digit of year (ex: 2 for 2002)
 WW = Week code (01 to 53)

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Peak Pulse Power Dissipation (Non repetitive current pulse derated above $T_A = 25^\circ\text{C}$) (Note 4)	P_{PK}	400	W
Peak Forward Surge Current, 8.3ms Single Half Sine Wave Superimposed on Rated Load (Notes 4, 5 & 6)	I_{FSM}	40	A
Steady State Power Dissipation @ $T_L = 75^\circ\text{C}$	$P_M(AV)$	1.0	W
Instantaneous Forward Voltage @ $I_{PP} = 35\text{A}$ (Notes 4, 5, & 6)	V_F	3.5	V

Notes:

4. Valid provided that terminals are kept at ambient temperature.
5. Measured with 8.3ms single half sine-wave. Duty cycle = 4 pulses per minute maximum.
6. Unidirectional units only.

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Operating Temperature Range	T_J	-55 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to +175	$^\circ\text{C}$

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Part Number Add C For Bidirectional (Note 7)	Reverse Standoff Voltage V_{RWM} (V)	Breakdown Voltage V_{BR} @ I_T (Note 8)		Test Current I_T (mA)	Max. Reverse Leakage @ V_{RWM} (Note 9)	Max. Clamping Voltage @ I_{pp}	Max. Peak Pulse Current I_{pp}	Marking Code	
		Min (V)	Max (V)					I_R (μA)	V_C (V)
SMAJ5.0(C)A	5.0	6.40	7.25	10	800	9.2	43.5	TE	HE
SMAJ6.0(C)A	6.0	6.67	7.37	10	800	10.3	38.8	TG	HG
SMAJ6.5(C)A	6.5	7.22	7.98	10	500	11.2	35.7	TK	HK
SMAJ7.0(C)A	7.0	7.78	8.60	10	200	12.0	33.3	TM	HM
SMAJ7.5(C)A	7.5	8.33	9.21	1.0	100	12.9	31.0	TP	HP
SMAJ8.0(C)A	8.0	8.89	9.83	1.0	50	13.6	29.4	TR	HR
SMAJ8.5(C)A	8.5	9.44	10.4	1.0	10	14.4	27.7	TT	HT
SMAJ9.0(C)A	9.0	10.0	11.1	1.0	5.0	15.4	26.0	TV	HV
SMAJ10(C)A	10	11.1	12.3	1.0	5.0	17.0	23.5	TX	HX
SMAJ11(C)A	11	12.2	13.5	1.0	5.0	18.2	22.0	TZ	HZ
SMAJ12(C)A	12	13.3	14.7	1.0	5.0	19.9	20.1	UE	IE
SMAJ13(C)A	13	14.4	15.9	1.0	5.0	21.5	18.6	UG	IG
SMAJ14(C)A	14	15.6	17.2	1.0	5.0	23.2	17.2	UK	IK
SMAJ15(C)A	15	16.7	18.5	1.0	5.0	24.4	16.4	UM	IM
SMAJ16(C)A	16	17.8	19.7	1.0	5.0	26.0	15.3	UP	IP
SMAJ17(C)A	17	18.9	20.9	1.0	5.0	27.6	14.5	UR	IR
SMAJ18(C)A	18	20.0	22.1	1.0	5.0	29.2	13.7	UT	IT
SMAJ20(C)A	20	22.2	24.5	1.0	5.0	32.4	12.3	UV	IV
SMAJ22(C)A	22	24.4	26.9	1.0	5.0	35.5	11.2	UX	IX
SMAJ24(C)A	24	26.7	29.5	1.0	5.0	38.9	10.3	UZ	IZ
SMAJ26(C)A	26	28.9	31.9	1.0	5.0	42.1	9.5	VE	JE
SMAJ28(C)A	28	31.1	34.4	1.0	5.0	45.4	8.8	VG	JG
SMAJ30(C)A	30	33.3	36.8	1.0	5.0	48.4	8.3	VK	JK
SMAJ33(C)A	33	36.7	40.6	1.0	5.0	53.3	7.5	VM	JM
SMAJ36(C)A	36	40.0	44.2	1.0	5.0	58.1	6.9	VP	JP
SMAJ40(C)A	40	44.4	49.1	1.0	5.0	64.5	6.2	VR	JR
SMAJ43(C)A	43	47.8	52.8	1.0	5.0	69.4	5.7	VT	JT
SMAJ45(C)A	45	50.0	55.3	1.0	5.0	72.7	5.5	VV	JV
SMAJ48(C)A	48	53.3	58.9	1.0	5.0	77.4	5.2	VX	JX
SMAJ51(C)A	51	56.7	62.7	1.0	5.0	82.4	4.9	VZ	JZ
SMAJ54(C)A	54	60.0	66.3	1.0	5.0	87.1	4.6	WE	RE
SMAJ58(C)A	58	64.4	71.2	1.0	5.0	93.6	4.3	WG	RG
SMAJ60(C)A	60	66.7	73.7	1.0	5.0	96.8	4.1	WK	RK
SMAJ64(C)A	64	71.1	78.6	1.0	5.0	103	3.9	WM	RM
SMAJ70(C)A	70	77.8	86.0	1.0	5.0	113	3.5	WP	RP
SMAJ75(C)A	75	83.3	92.1	1.0	5.0	121	3.3	WR	RR
SMAJ78(C)A	78	86.7	95.8	1.0	5.0	126	2.2	WT	RT
SMAJ85(C)A	85	94.4	104	1.0	5.0	137	2.9	WV	RV
SMAJ90(C)A	90	100	111	1.0	5.0	146	2.7	WX	RX
SMAJ100(C)A	100	111	123	1.0	5.0	162	2.5	WZ	RZ
SMAJ110(C)A	110	122	135	1.0	5.0	177	2.3	XE	SE
SMAJ120(C)A	120	133	147	1.0	5.0	193	2.0	XG	SG
SMAJ130(C)A	130	144	159	1.0	5.0	209	1.9	XK	SK
SMAJ150(C)A	150	167	185	1.0	5.0	243	1.6	XM	SM
SMAJ160(C)A	160	178	197	1.0	5.0	259	1.5	XP	SP
SMAJ170(C)A	170	189	209	1.0	5.0	275	1.4	XR	SR
SMAJ200(C)A	200	224	248	1.0	1.0	324	1.2	YT	ST

Notes: 7. Suffix C denotes Bi-directional device.

8. V_{BR} measured with I_T current pulse = 300 μs

9. For Bidirectional devices having V_{RWM} of 10V and under, the I_R is doubled.

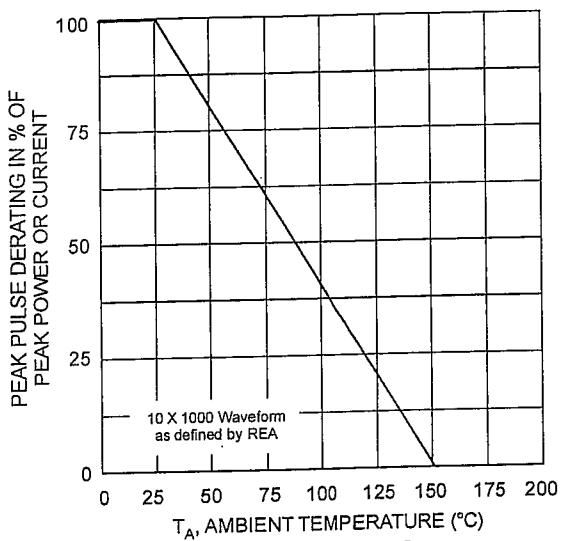


Fig. 1 Pulse Derating Curve

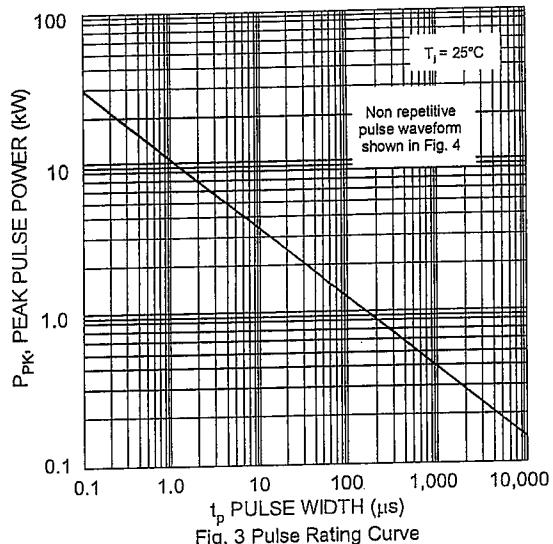


Fig. 3 Pulse Rating Curve

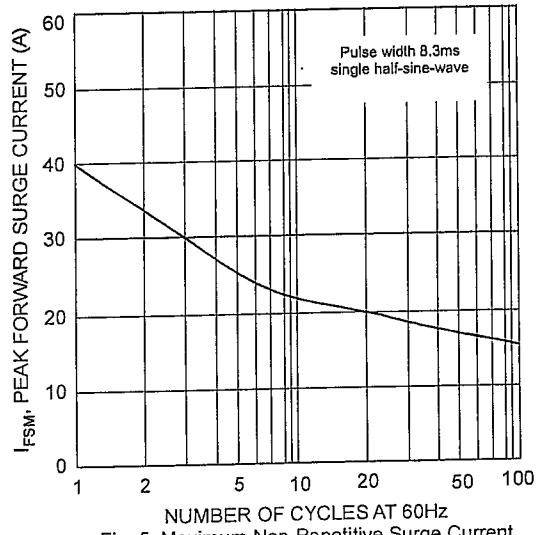


Fig. 5 Maximum Non-Repetitive Surge Current

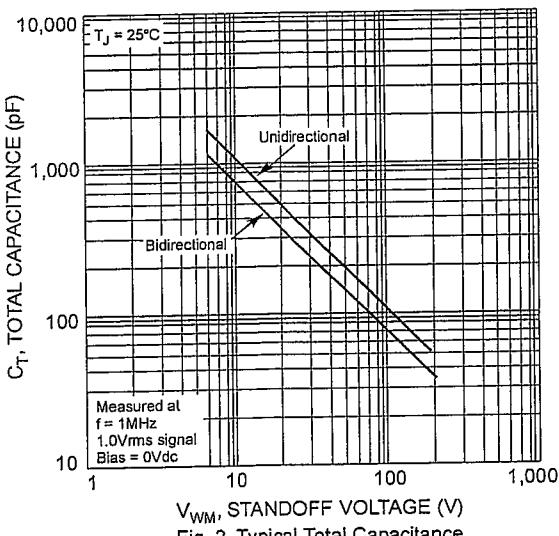


Fig. 2 Typical Total Capacitance

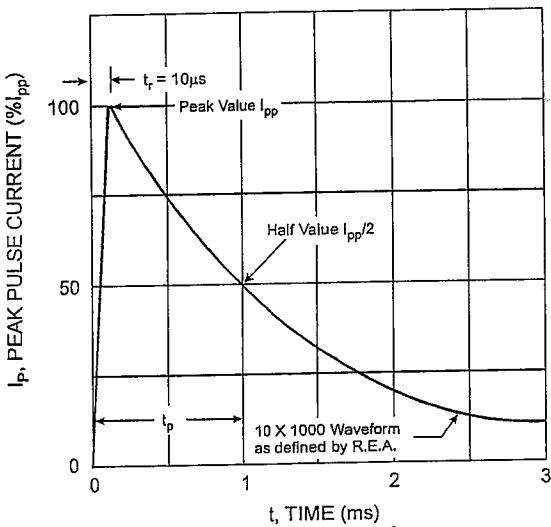


Fig. 4 Pulse Waveform

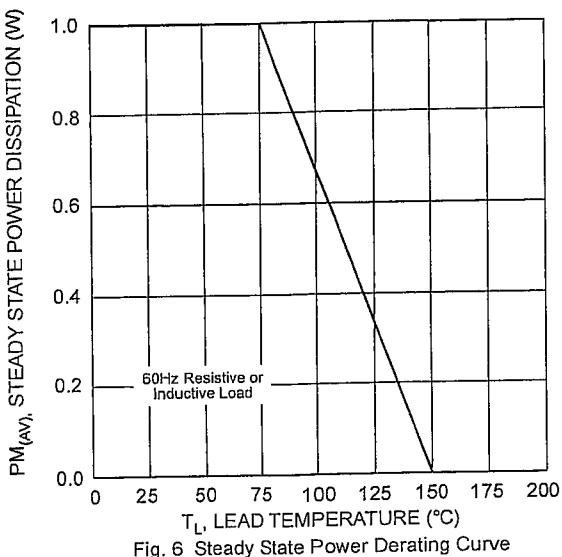
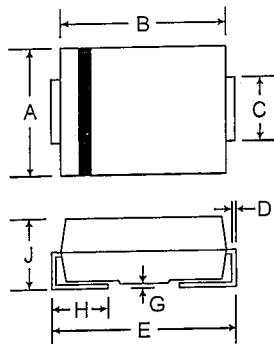


Fig. 6 Steady State Power Derating Curve

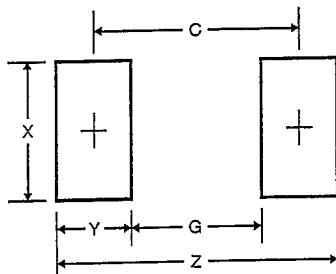
Package Outline Dimensions



SMA		
Dim	Min	Max
A	2.29	2.92
B	4.00	4.60
C	1.27	1.63
D	0.15	0.31
E	4.80	5.59
G	0.05	0.20
H	0.76	1.52
J	2.01	2.30

All Dimensions in mm

Suggested Pad Layout



SMA Dimensions	Value (in mm)
Z	6.5
G	1.5
X	1.7
Y	2.5
C	4.0

Q1
BCX 54 / 55 / 56

NPN SILICON PLANAR MEDIUM POWER TRANSISTORS IN SOT89

Features

- $I_c = 1A$ Continuous Collector Current
- Low Saturation Voltage $V_{CE(sat)} < 500mV$ @ 0.5A
- Gain groups 10 and 16
- Epitaxial Planar Die Construction
- Complementary PNP types: BCX51, 52 and 53
- Lead-Free, RoHS Compliant (Note 1)
- Halogen and Antimony Free. "Green" Devices (Note 2)
- Qualified to AEC-Q101 Standards for High Reliability

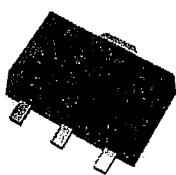
Mechanical Data

- Case: SOT89
- Case Material: Molded Plastic, "Green" Molding Compound (Note 2)
- UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish
- Weight: 0.072 grams (Approximate)

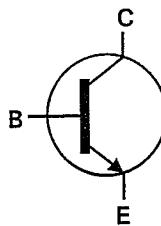
Applications

- Medium Power Switching or Amplification Applications
- AF driver and output stages

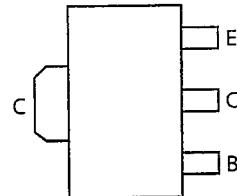
SOT89



Top View



Device Symbol

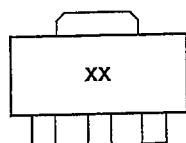
Top View
Pin-Out

Ordering Information (Note 3 & 4)

Product	Grade	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
BCX54TA	Commercial	BA	7	12	1,000
BCX5410TA	Commercial	BC	7	12	1,000
BCX5416TA	Commercial	BD	7	12	1,000
BCX55TA	Commercial	BE	7	12	1,000
BCX5510TA	Commercial	BG	7	12	1,000
BCX5516TA	Commercial	BM	7	12	1,000
BCX56TA	Commercial	BH	7	12	1,000
BCX5610TA	Commercial	BK	7	12	1,000
BCX5616TA	Commercial	BL	7	12	1,000
BCX5616QTA	Automotive	BL	7	12	1,000
BCX5616TC	Commercial	BL	13	12	4,000

- Notes:
1. No purposefully added lead.
 2. Diodes Inc's "Green" Policy can be found on our website at <http://www.diodes.com>
 3. For packaging details, go to our website <http://www.diodes.com>
 4. Products with Q-suffix are automotive grade. Automotive products are electrical and thermal the same as the commercial, except where specified.

Marking Information



xx = Product Type Marking Code, as follows:

BCX54 = BA
BCX5410 = BC
BCX5416 = BD

BCX55 = BE
BCX5510 = BG
BCX5516 = BM

BCX56 = BH
BCX5610 = BK
BCX5616 = BL

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	BCX54	BCX55	BCX56	Unit
Collector-Base Voltage	V_{CBO}	45	60	100	V
Collector-Emitter Voltage	V_{CEO}	45	60	80	V
Emitter-Base Voltage	V_{EBO}		5		V
Continuous Collector Current	I_C		1		A
Peak Pulse Collector Current	I_{CM}		1.5		
Continuous Base Current	I_B		100		
Peak Pulse Base Current	I_{BM}		200		mA

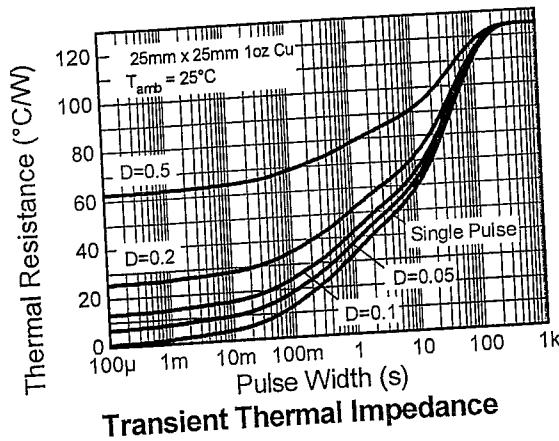
Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	P_D	1	W
Thermal Resistance, Junction to Ambient (Note 4)	$R_{\theta JA}$	124	°C/W
Thermal Resistance, Junction to Leads (Note 5)	$R_{\theta JL}$	10.0	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to +150	°C

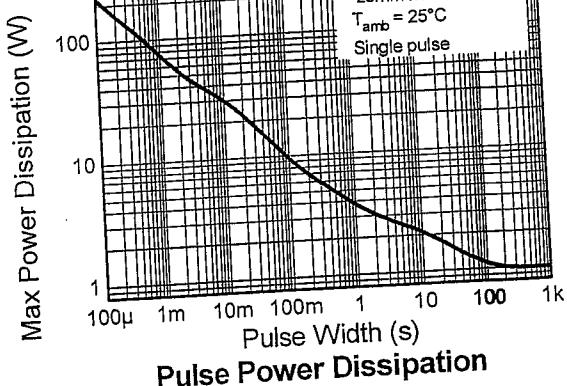
Notes:

- 4. For a device surface mounted on 25mm X 25mm FR4 PCB with high coverage of single sided 1 oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
- 5. Thermal resistance from junction to solder-point (on the exposed collector pad).

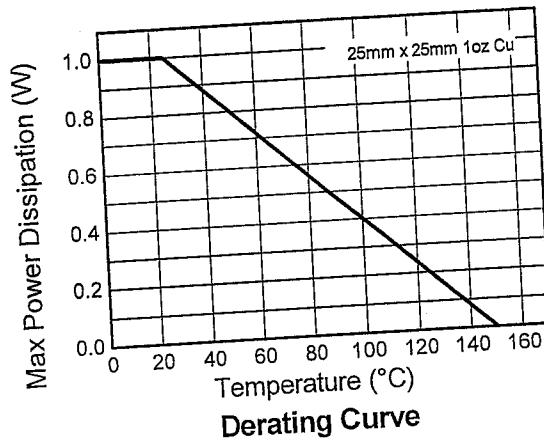
Thermal Characteristics



Transient Thermal Impedance



Pulse Power Dissipation



Derating Curve

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BCX54	BV_{CBO}	45	-	-	V	$I_C = 100\mu\text{A}$
	BCX55		60	-	-	V	
	BCX56		100	-	-	V	
Collector-Emitter Breakdown Voltage (Note 6)	BCX54	BV_{CEO}	45	-	-	V	$I_C = 10\text{mA}$
	BCX55		60	-	-	V	$I_E = 10\mu\text{A}$
	BCX56		80	-	-	V	
Emitter-Base Breakdown Voltage		BV_{EBO}	5	-	-	V	
Collector Cut-off Current		I_{CBO}	-	-	0.1 20	μA	$V_{\text{CB}} = 30\text{V}$ $V_{\text{CB}} = 30\text{V}, T_A = 150^\circ\text{C}$
Emitter Cut-off Current		I_{EBO}	-	-	20	nA	$V_{\text{EB}} = 4\text{V}$
Static Forward Current Transfer Ratio (Note 6)	All versions	h_{FE}	25	-	-		$I_C = 5\text{mA}, V_{\text{CE}} = 2\text{V}$
	10 gain grp		40	-	250		$I_C = 150\text{mA}, V_{\text{CE}} = 2\text{V}$
	16 gain grp		25	-	-		$I_C = 500\text{mA}, V_{\text{CE}} = 2\text{V}$
Collector-Emitter Saturation Voltage (Note 6)		$V_{\text{CE(sat)}}$	-	-	0.5	V	$I_C = 150\text{mA}, V_{\text{CE}} = 2\text{V}$
Base-Emitter Turn-On Voltage (Note 6)		$V_{\text{BE(on)}}$	-	-	1.0	V	$I_C = 50\text{mA}, V_{\text{CE}} = 10\text{V}$
Transition Frequency		f_T	150	-	-	MHz	$f = 100\text{MHz}$
Output Capacitance		C_{obo}	-	-	25	pF	$V_{\text{CB}} = 10\text{V}, f = 1\text{MHz}$

Notes: 6. Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$. Duty cycle $\leq 2\%$.

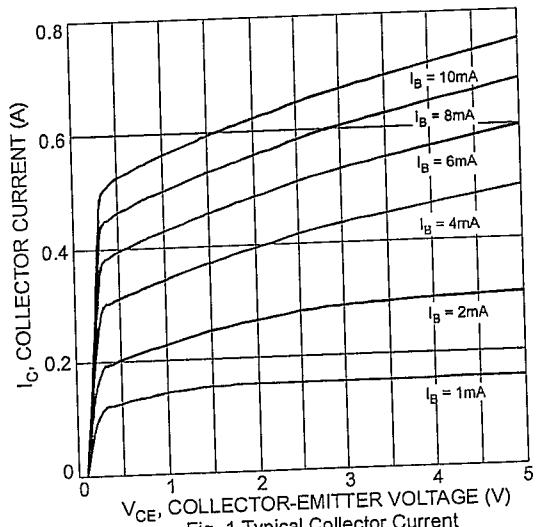


Fig. 1 Typical Collector Current vs. Collector-Emitter Voltage

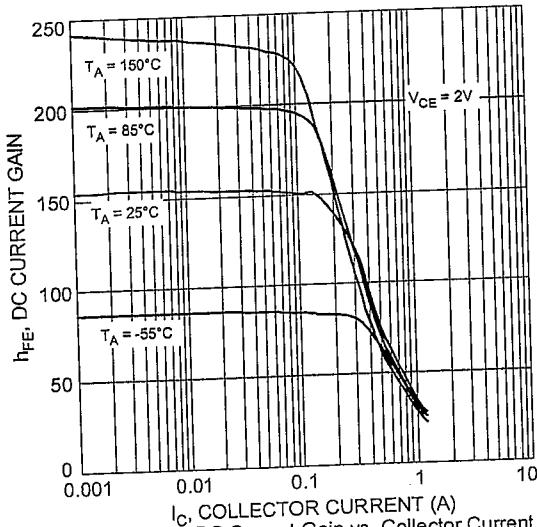


Fig. 2 Typical DC Current Gain vs. Collector Current

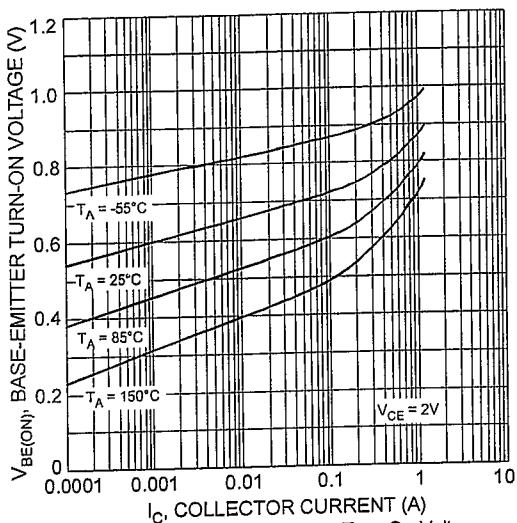


Fig. 3 Typical Base-Emitter Turn-On Voltage
vs. Collector Current

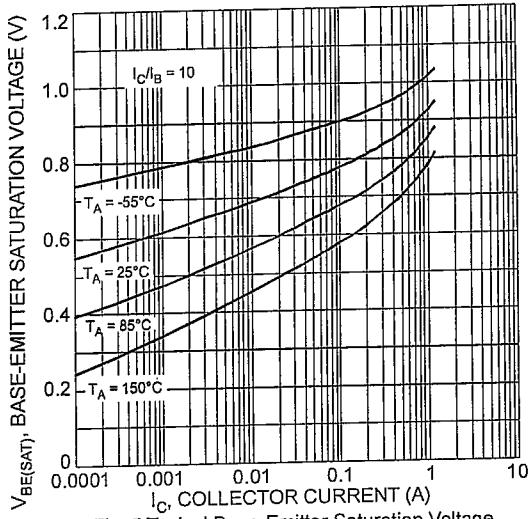


Fig. 5 Typical Base-Emitter Saturation Voltage
vs. Collector Current

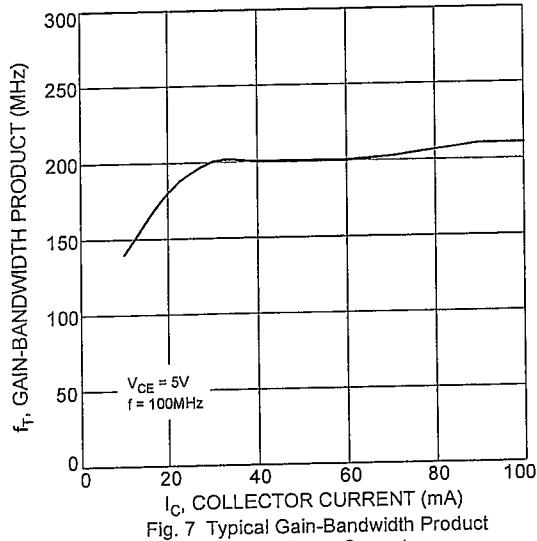


Fig. 7 Typical Gain-Bandwidth Product
vs. Collector Current

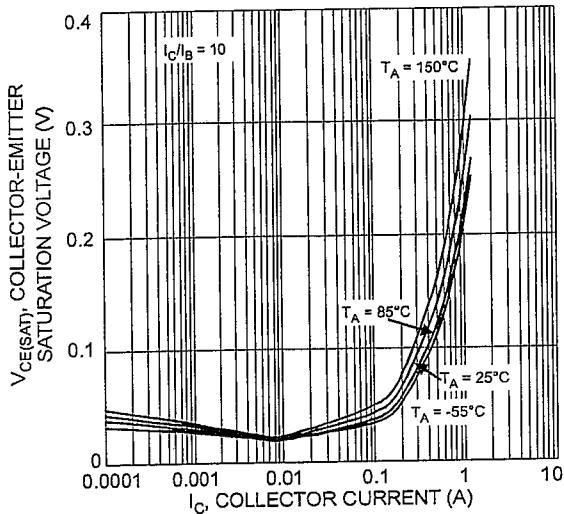


Fig. 4 Typical Collector-Emitter Saturation Voltage
vs. Collector Current

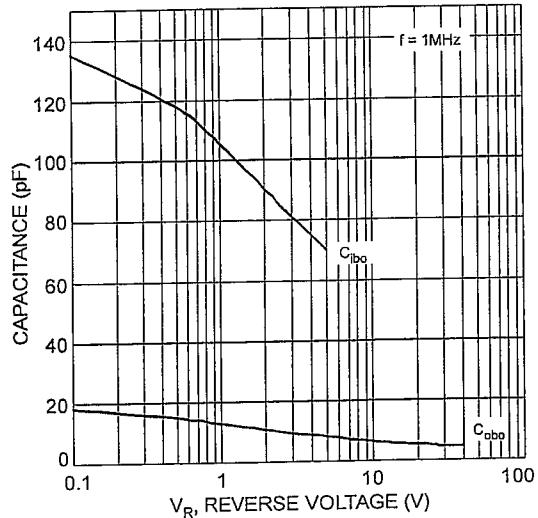
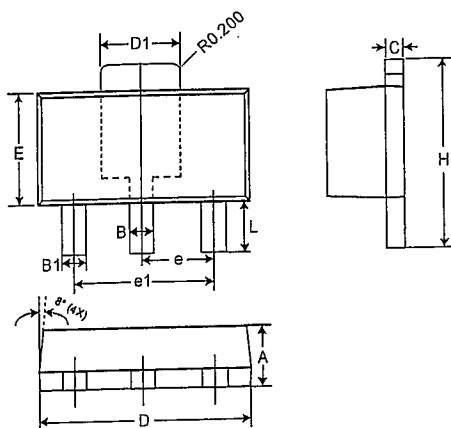


Fig. 6 Typical Capacitance Characteristics

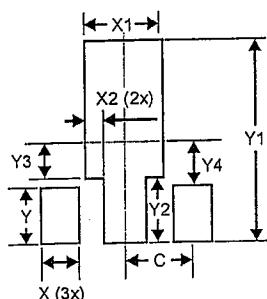
Package Outline Dimensions



SOT89		
Dim	Min	Max
A	1.40	1.60
B	0.44	0.62
B1	0.35	0.54
C	0.35	0.43
D	4.40	4.60
D1	1.52	1.83
E	2.29	2.60
E	1.50 Typ	
e1	3.00 Typ	
H	3.94	4.25
L	0.89	1.20

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
X	0.900
X1	1.733
X2	0.416
Y	1.300
Y1	4.600
Y2	1.475
Y3	0.950
Y4	1.125
C	1.500

N1-N4



FDD3510H

Dual N & P-Channel PowerTrench® MOSFET

N-Channel: 80V, 13.9A, 80mΩ P-Channel: -80V, -9.4A, 190mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 80mΩ at $V_{GS} = 10V$, $I_D = 4.3A$
- Max $r_{DS(on)}$ = 88mΩ at $V_{GS} = 6V$, $I_D = 4.1A$

Q2: P-Channel

- Max $r_{DS(on)}$ = 190mΩ at $V_{GS} = -10V$, $I_D = -2.8A$
- Max $r_{DS(on)}$ = 224mΩ at $V_{GS} = -4.5V$, $I_D = -2.6A$
- 100% UIL Tested
- RoHS Compliant

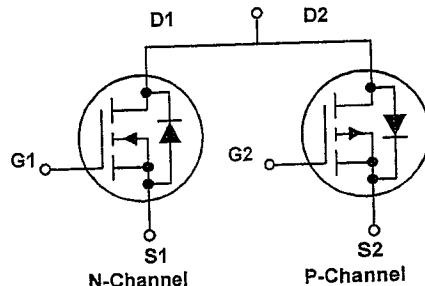
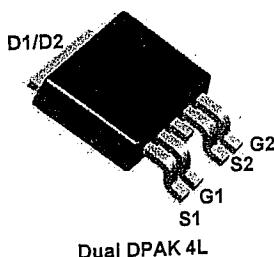


General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Applications

- Inverter
- H-Bridge



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	80	-80	V
V_{GS}	Gate to Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous $T_C = 25^\circ C$	13.9	-9.4	A
	- Continuous $T_A = 25^\circ C$	4.3	-2.8	
	- Pulsed	20	-10	
P_D	Power Dissipation for Single Operation $T_C = 25^\circ C$ (Note 1)	35	32	W
	$T_A = 25^\circ C$ (Note 1a)	3.1		
	$T_A = 25^\circ C$ (Note 1b)	1.3		
E_{AS}	Single Pulse Avalanche Energy (Note 3)	37	54	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

R_{JC}	Thermal Resistance, Junction to Case, Single Operation for Q1 (Note 1)	3.5	°C/W
R_{JC}	Thermal Resistance, Junction to Case, Single Operation for Q2 (Note 1)	3.9	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3510H	FDD3510H	TO-252-4L	13"	12mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	Q1 Q2	80 -80			V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}, \text{referenced to } 25^\circ\text{C}$ $I_D = -250\mu\text{A}, \text{referenced to } 25^\circ\text{C}$	Q1 Q2		84 -67		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = -64\text{V}, V_{GS} = 0\text{V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	Q1 Q2			± 100 ± 100	nA nA

On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	Q1 Q2	2.0 -1.0	2.6 -1.6	4.0 -3.0	V
$\Delta V_{GS(\text{th})}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}, \text{referenced to } 25^\circ\text{C}$ $I_D = -250\mu\text{A}, \text{referenced to } 25^\circ\text{C}$	Q1 Q2		-6.7 4.6		$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 4.3\text{A}$ $V_{GS} = 6.0\text{V}, I_D = 4.1\text{A}$ $V_{GS} = 10\text{V}, I_D = 4.3\text{A}, T_J = 125^\circ\text{C}$	Q1		64 70 121	80 88 152	$\text{m}\Omega$
		$V_{GS} = -10\text{V}, I_D = -2.8\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -2.6\text{A}$ $V_{GS} = -10\text{V}, I_D = -2.8\text{A}, T_J = 125^\circ\text{C}$	Q2		153 184 259	190 224 322	
		$V_{DD} = 10\text{V}, I_D = 4.3\text{A}$ $V_{DD} = -5\text{V}, I_D = -2.8\text{A}$	Q1 Q2		15 6.8		S
g_{FS}	Forward Transconductance						

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		600 660	800 880	pF
C_{oss}	Output Capacitance	Q2 $V_{DS} = -40\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		56 50	75 70	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		27 25	41 40	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	Q1 Q2		1.7 7.2		Ω

Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	Q1 $V_{DD} = 40\text{V}, I_D = 4.3\text{A}, V_{GS} = 10\text{V}, R_{\text{GEN}} = 6\Omega$	Q1 Q2		7 6	13 11	ns
t_r	Rise Time	Q2 $V_{DD} = -40\text{V}, I_D = -2.8\text{A}, V_{GS} = -10\text{V}, R_{\text{GEN}} = 6\Omega$	Q1 Q2		2 3	10 10	ns
$t_{d(\text{off})}$	Turn-Off Delay Time	Q2 $V_{DD} = -40\text{V}, I_D = -2.8\text{A}, V_{GS} = -10\text{V}, R_{\text{GEN}} = 6\Omega$	Q1 Q2		16 25	29 40	ns
t_f	Fall Time	Q1 $V_{GS} = 10\text{V}, V_{DD} = 40\text{V}, I_D = 4.3\text{A}$	Q1 Q2		2 5	10 10	ns
$Q_{g(\text{TOT})}$	Total Gate Charge	Q1 $V_{GS} = 10\text{V}, V_{DD} = 40\text{V}, I_D = 4.3\text{A}$	Q1 Q2		13 14	18 20	nC
Q_{gs}	Gate to Source Charge	Q2 $V_{GS} = -10\text{V}, V_{DD} = -40\text{V}, I_D = -2.8\text{A}$	Q1 Q2		2.3 1.9		nC
Q_{gd}	Gate to Drain "Miller" Charge	Q1 $V_{GS} = -10\text{V}, V_{DD} = -40\text{V}, I_D = -2.8\text{A}$	Q1 Q2		3.2 2.9		nC

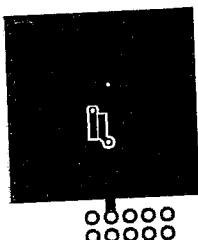
Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units	
Drain-Source Diode Characteristics								
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 2.6A$ $V_{GS} = 0V, I_S = -2.6A$	(Note 2)	Q1 Q2		0.8 -0.8	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 4.3A, di/dt = 100A/\text{s}$		Q1 Q2		29 30	46 48	ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -2.8A, di/dt = 100A/\text{s}$		Q1 Q2		28 30	45 48	nC

Notes:

1. R_{QJA} is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5×1.5 in. board of FR-4 material. R_{QJC} is guaranteed by design while R_{QCA} is determined by the user's board design.

Q1



a. $40^\circ\text{C}/\text{W}$ when mounted on
a 1in^2 pad of 2 oz copper

Scale 1 : 1 on letter size paper



b. $96^\circ\text{C}/\text{W}$ when mounted on a
minimum pad of 2 oz copper

Q2



a. $40^\circ\text{C}/\text{W}$ when mounted on
a 1in^2 pad of 2 oz copper

Scale 1 : 1 on letter size paper



b. $96^\circ\text{C}/\text{W}$ when mounted on a
minimum pad of 2 oz copper

2. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3. Starting $T_J = 25^\circ\text{C}$, N-ch: $L = 3\text{mH}$, $I_{AS} = 5\text{A}$, $V_{DD} = 80\text{V}$, $V_{GS} = 10\text{V}$; P-ch: $L = 3\text{mH}$, $I_{AS} = -5\text{A}$, $V_{DD} = -80\text{V}$, $V_{GS} = -10\text{V}$.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

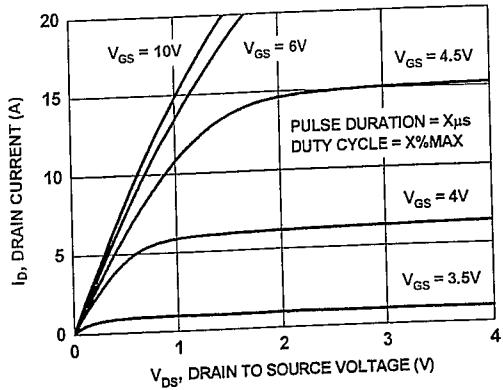


Figure 1. On Region Characteristics

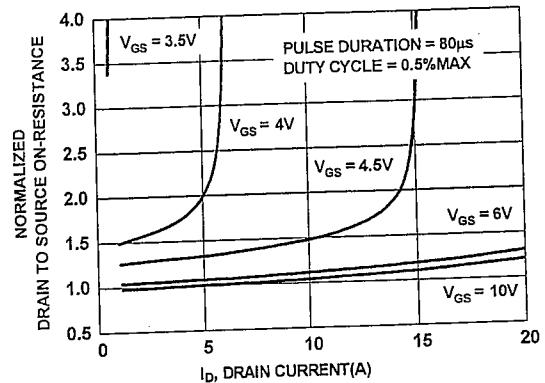


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

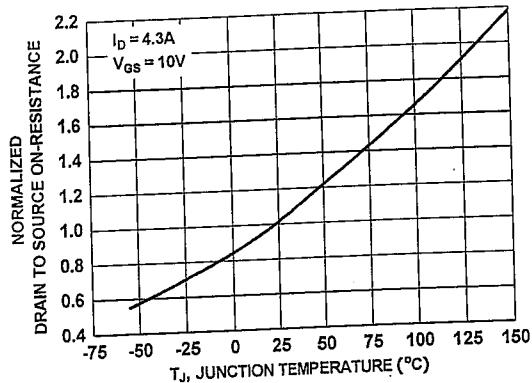


Figure 3. Normalized On Resistance vs Junction Temperature

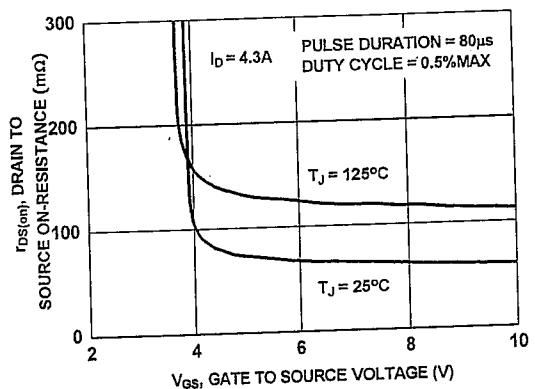


Figure 4. On-Resistance vs Gate to Source Voltage

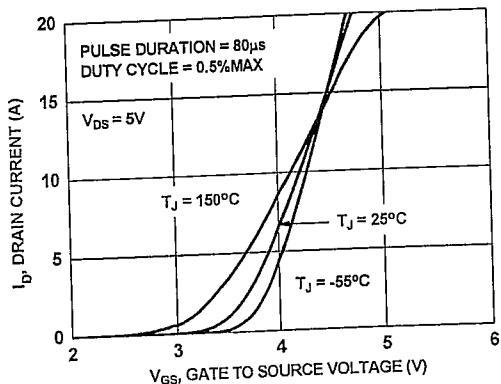


Figure 5. Transfer Characteristics

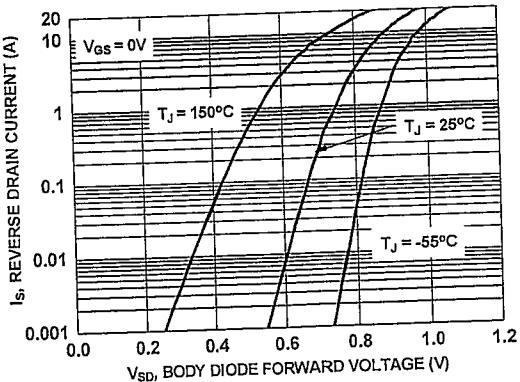


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

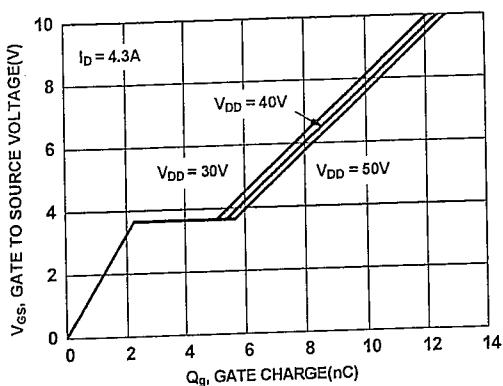


Figure 7. Gate Charge Characteristics

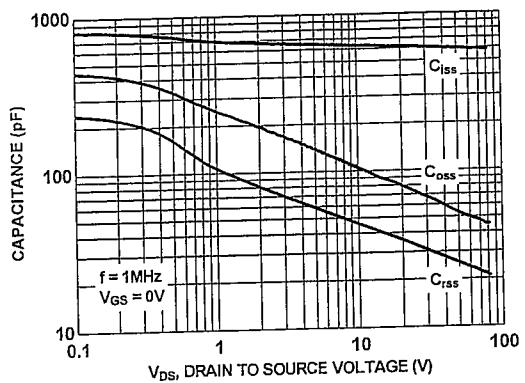


Figure 8. Capacitance vs Drain to Source Voltage

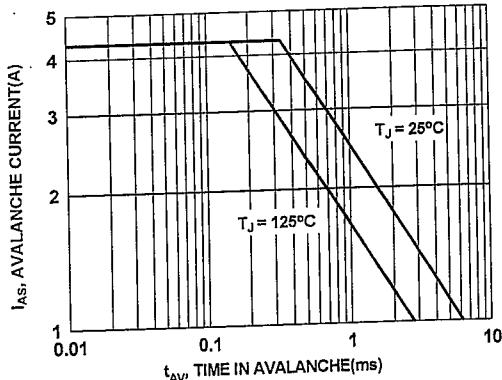


Figure 9. Unclamped Inductive Switching Capability

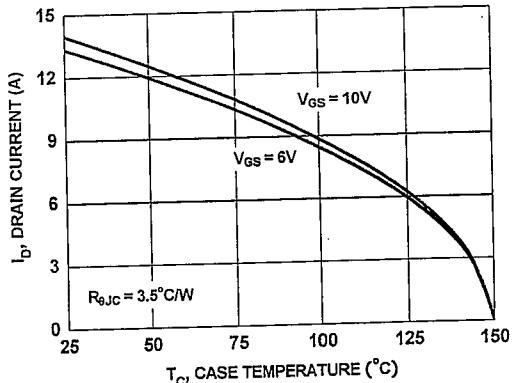


Figure 10. Maximum Continuous Drain Current vs Case Temperature

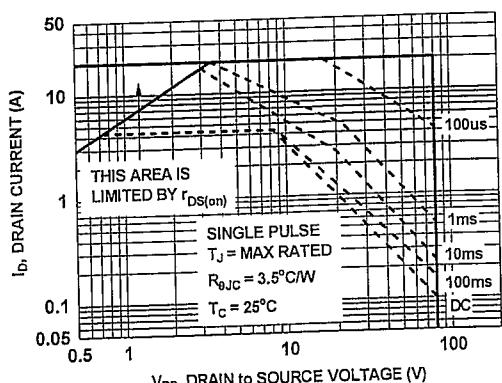


Figure 11. Forward Bias Safe Operating Area

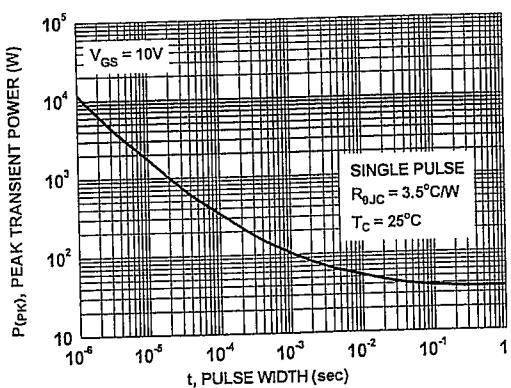


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

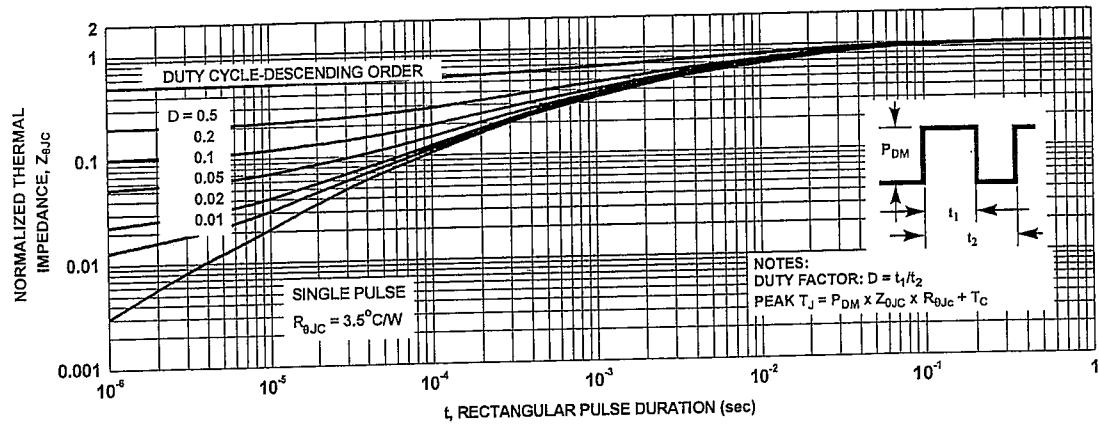


Figure 13. Transient Thermal Response Curve

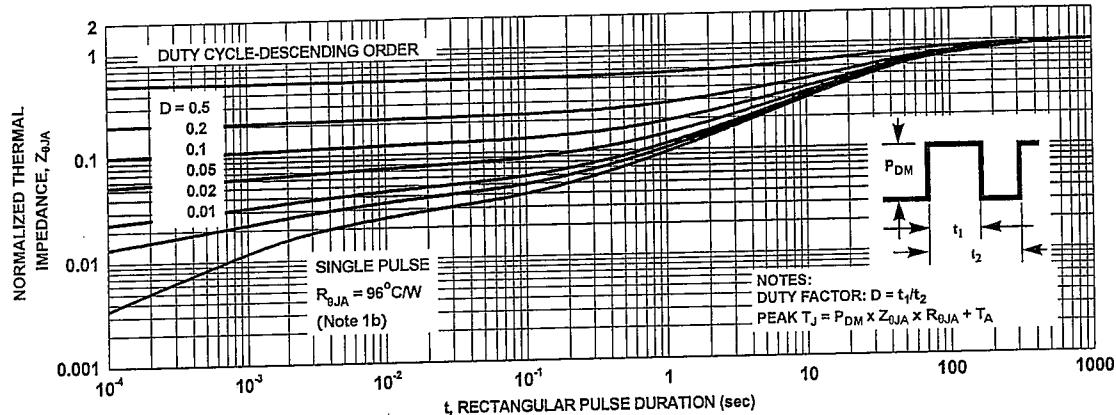


Figure 14. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

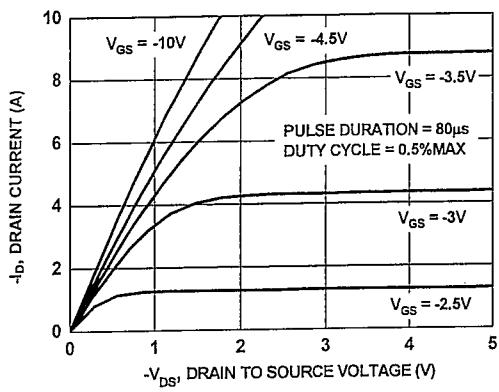


Figure 15. On-Region Characteristics

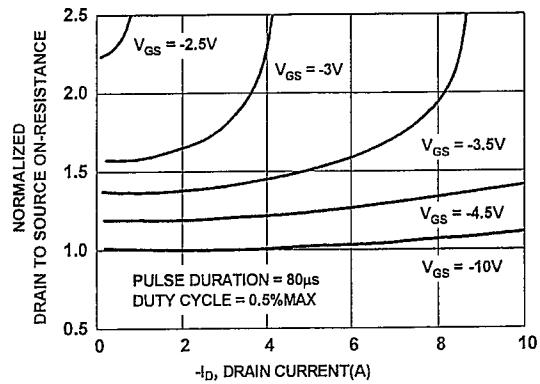


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

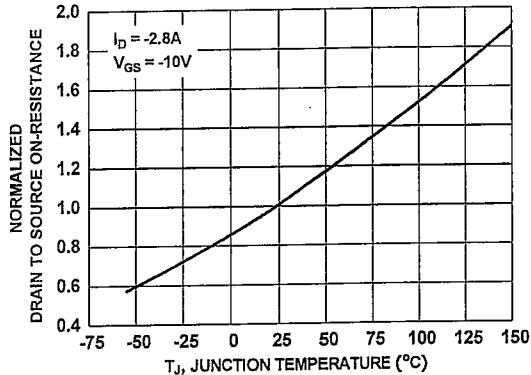


Figure 17. Normalized On-Resistance vs Junction Temperature

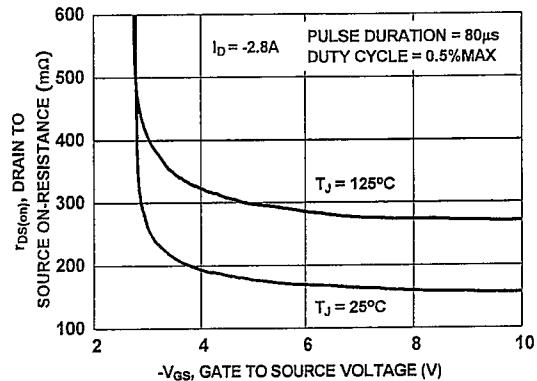


Figure 18. On-Resistance vs Gate to Source Voltage

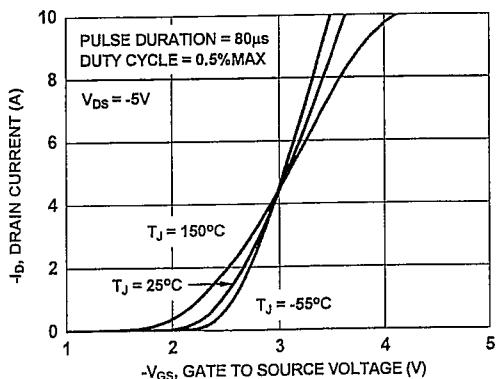


Figure 19. Transfer Characteristics

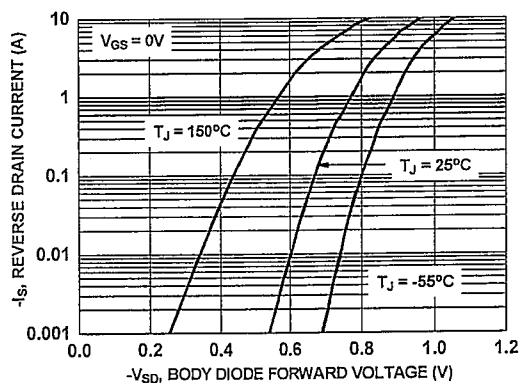


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

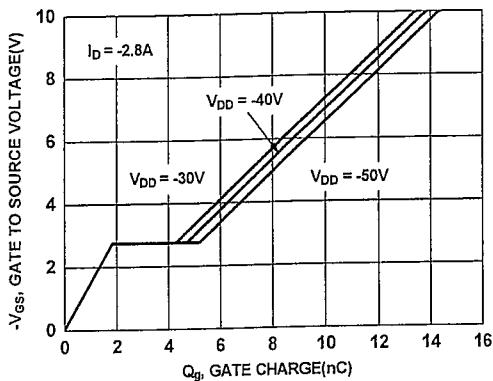


Figure 21. Gate Charge Characteristics

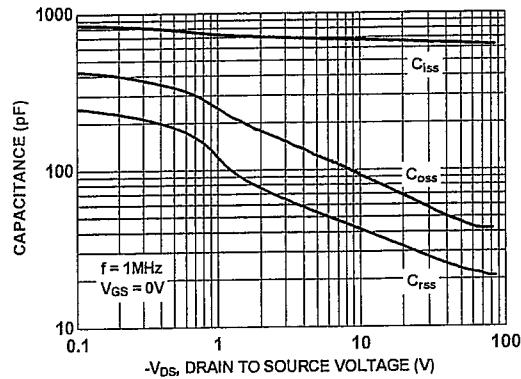


Figure 22. Capacitance vs Drain to Source Voltage

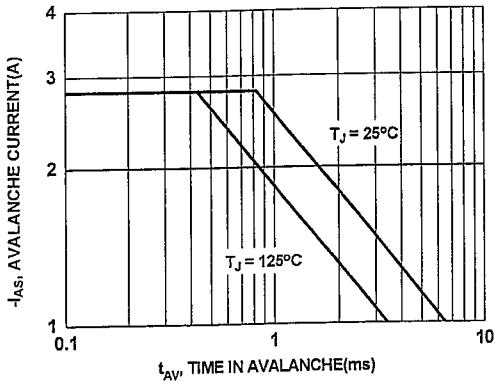


Figure 23. Unclamped Inductive Switching Capability

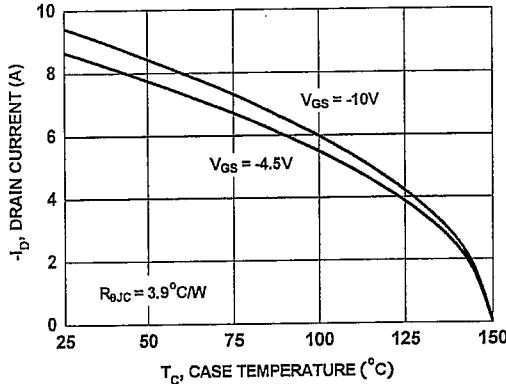


Figure 24. Maximum Continuous Drain Current vs Case Temperature

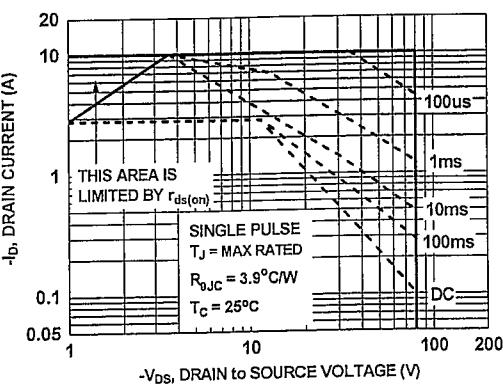


Figure 25. Forward Bias Safe Operating Area

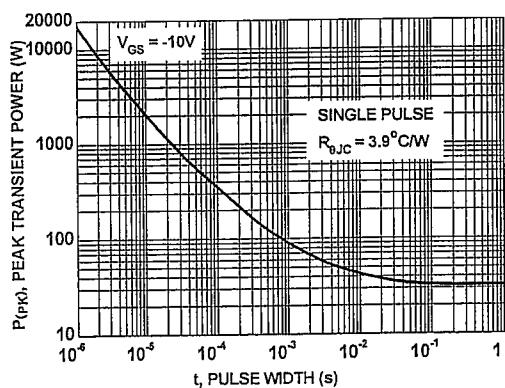


Figure 26. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

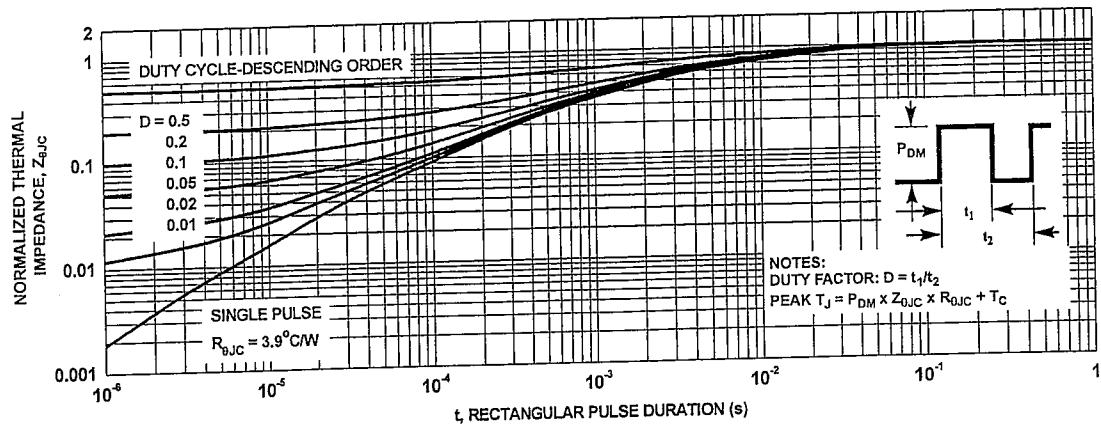


Figure 27. Transient Thermal Response Curve

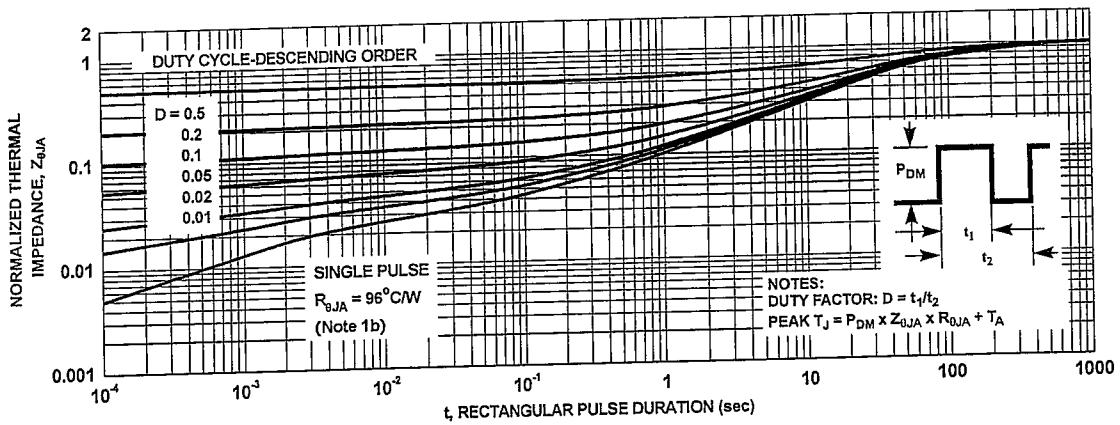


Figure 28. Transient Thermal Response Curve

N5, N6



FDS86141

N-Channel PowerTrench® MOSFET

100 V, 7 A, 23 mΩ

Features

- Maximum $R_{DS(on)} = 23 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 7 \text{ A}$
- Maximum $R_{DS(on)} = 36 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 5.5 \text{ A}$
- High-Performance Trench Technology; Extremely Low $R_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant



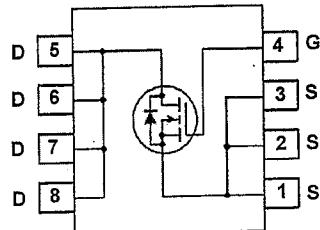
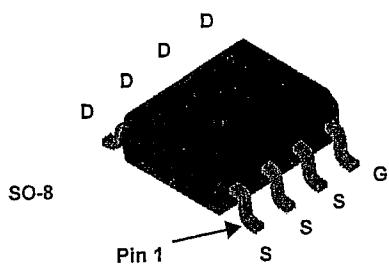
FDS86141 — N-Channel PowerTrench® MOSFET

General Description

This N-channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and maintain superior switching performance.

Applications

- DC-DC Conversion



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	7	A
	-Pulsed	30	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	W
	Power Dissipation	$T_A = 25^\circ\text{C}$	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS86141	FDS86141	SO-8	13 "	12 mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		67		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			± 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2	3.1	4	V
$\Delta V_{GS(\text{th})}/\Delta T_J$	Gate-to-Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C		-10		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$		19	23	$\text{m}\Omega$
		$V_{GS} = 6 \text{ V}, I_D = 5.5 \text{ A}$		27	37	
		$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}, T_J = 125^\circ\text{C}$		33	40	
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 7 \text{ A}$		19		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		703	934	pF
C_{oss}	Output Capacitance			186	247	pF
C_{rss}	Reverse Transfer Capacitance			8.6	13	pF
R_g	Gate Resistance			0.5		Ω

Switching Characteristics

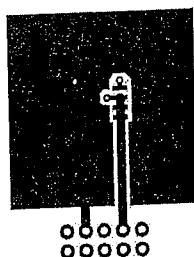
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 7 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		8.3	17	ns
t_r	Rise Time			3.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14.3	26	ns
t_f	Fall Time			3.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$		11.8	16.5	nC
	Total Gate Charge		$V_{DD} = 50 \text{ V}$	6.7	9.4	nC
Q_{gs}	Total Gate Charge	$I_D = 7 \text{ A}$		3.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.1		nC

Drain-Source Diode Characteristics

V_{SD}	Source-to-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 7 \text{ A}$	(Note 2)	0.8	1.3	V
		$V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$	(Note 2)	0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 7 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$		43	69	ns
				39	62	

NOTES:

1. R_{DJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{DJA} is guaranteed by design while R_{DCJA} is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



b) 125 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0 %.
3. Starting $T_J = 25^\circ\text{C}$; N-ch: L = 3 mH, $I_{AS} = 9 \text{ A}$, $V_{DD} = 100 \text{ V}$, $V_{GS} = 10 \text{ V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

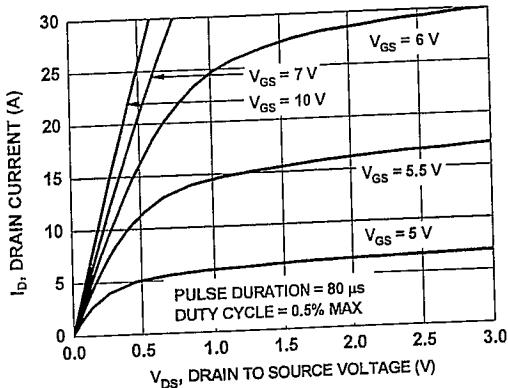


Figure 1. On-Region Characteristics

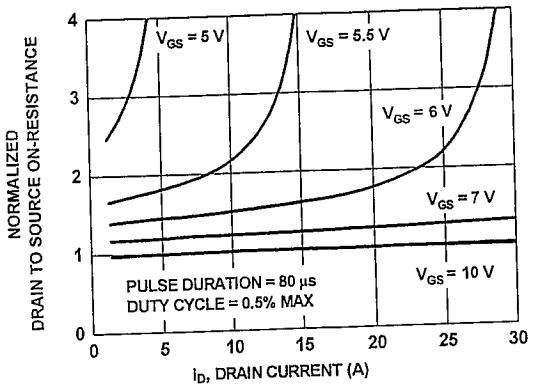


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

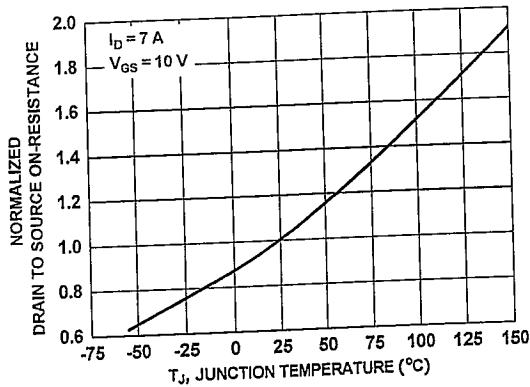


Figure 3. Normalized On-Resistance vs. Junction Temperature

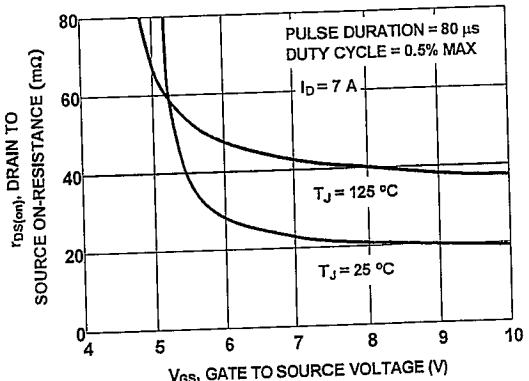


Figure 4. On-Resistance vs. Gate-to-Source Voltage

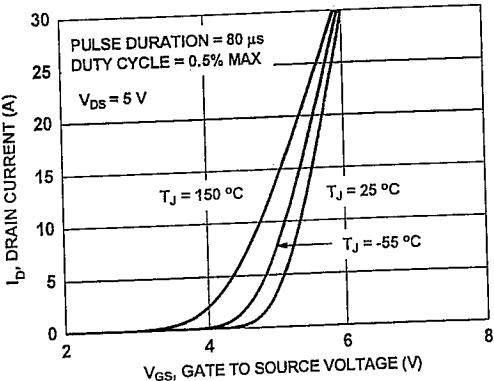


Figure 5. Transfer Characteristics

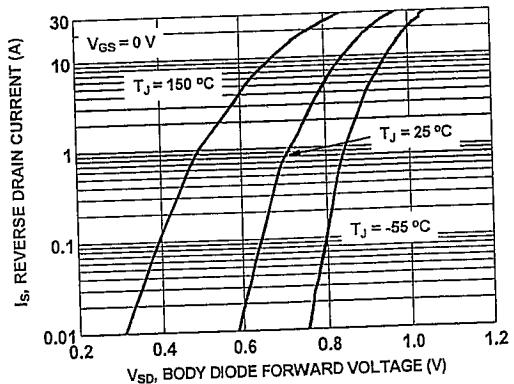


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

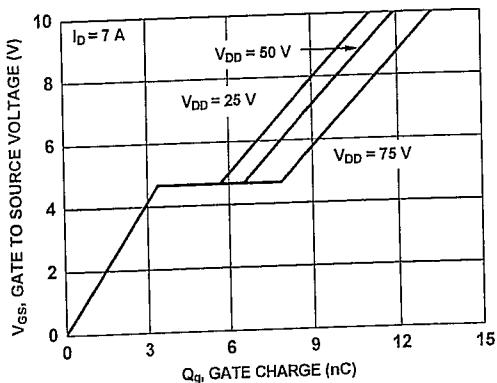


Figure 7. Gate Charge Characteristics

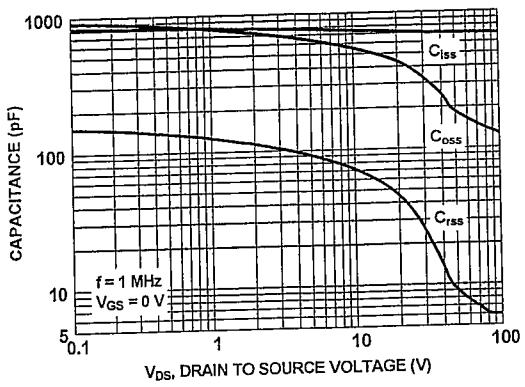


Figure 8. Capacitance vs. Drain-to-Source Voltage

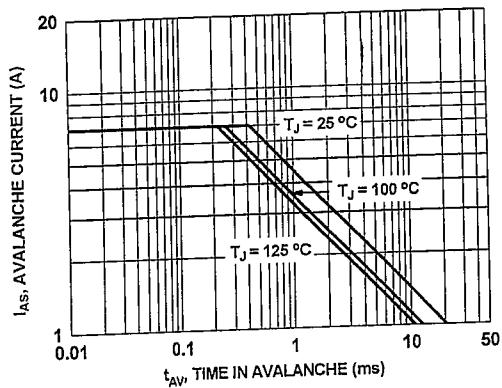


Figure 9. Unclamped Inductive Switching Capability

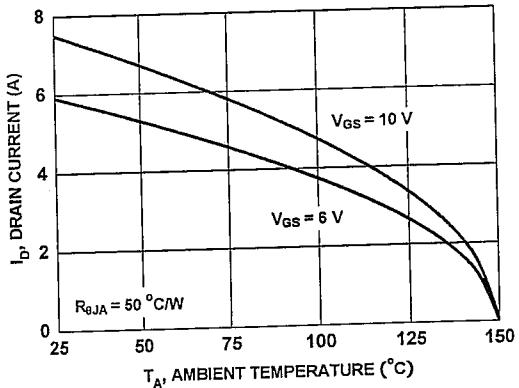


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

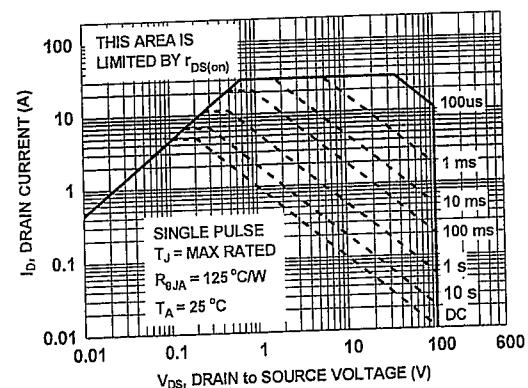


Figure 11. Forward Bias Safe Operating Area

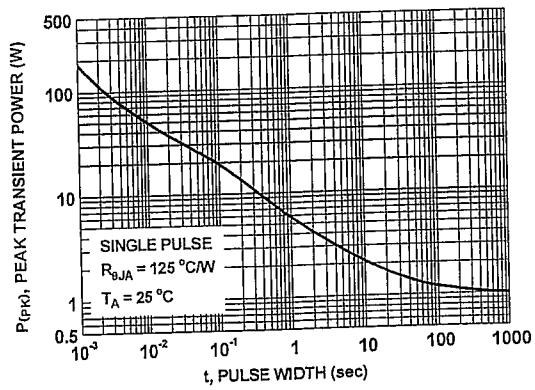


Figure 12. Single-Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

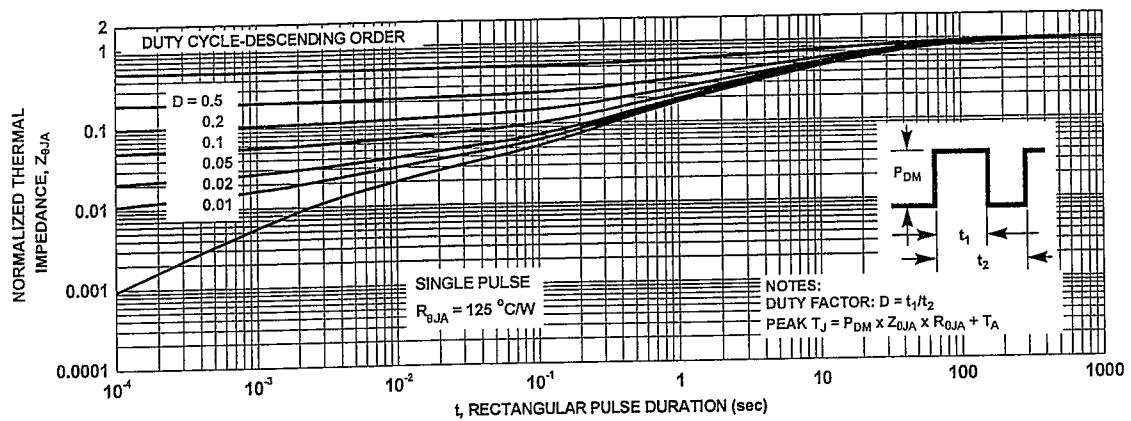


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Physical Dimensions

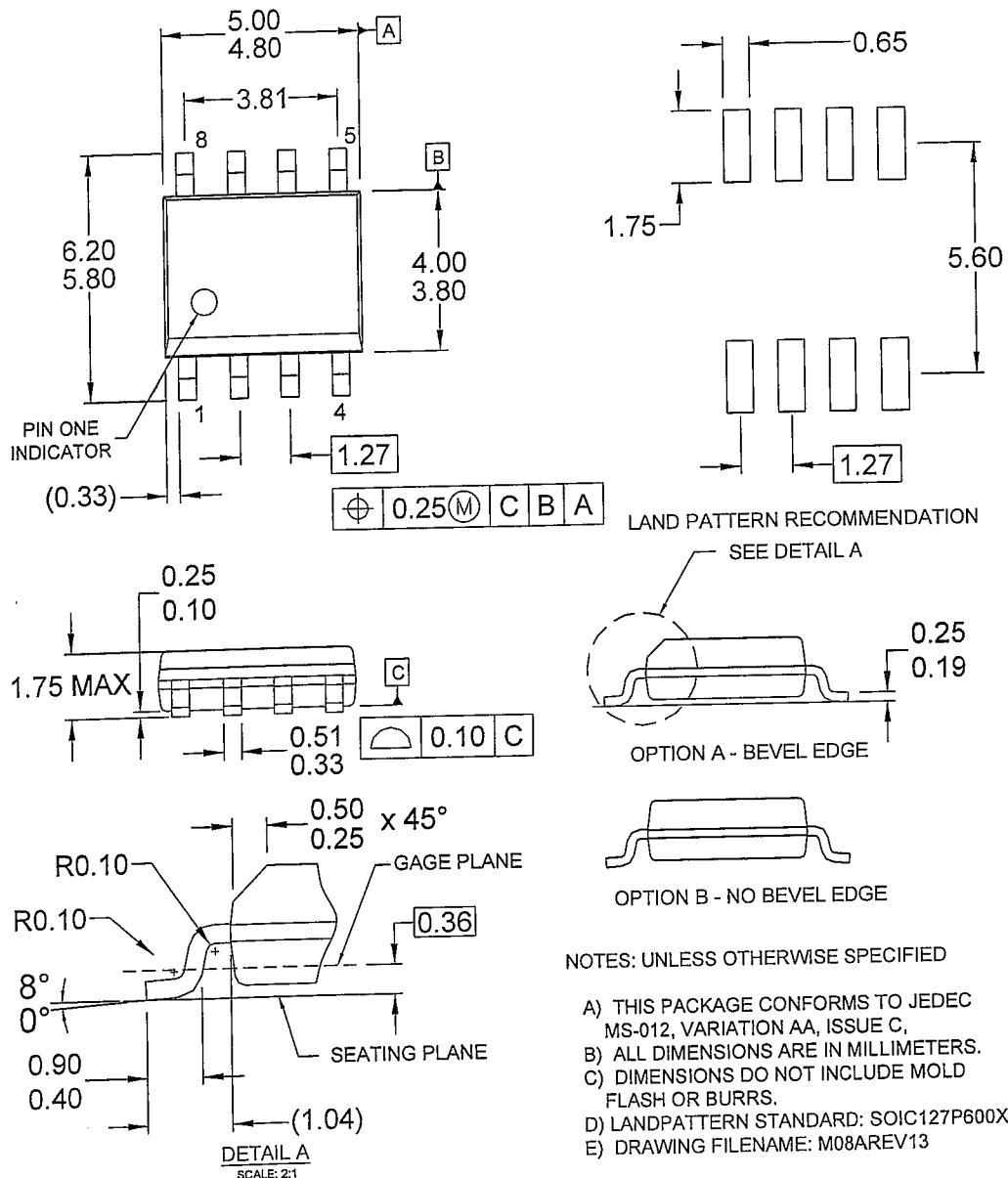


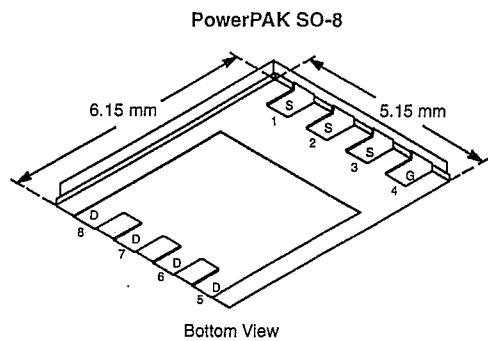
Figure 1. 8-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .150" Narrow Body

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

*Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>.*

N-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
150	0.045 at V _{GS} = 10 V	26	23 nC
	0.047 at V _{GS} = 8 V	25	



Ordering Information: Si7430DP-T1-E3 (Lead (Pb)-free)
Si7430DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

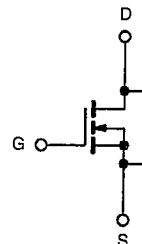
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Reduced dV/dt, Q_{gd} and Shoot-Through
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Primary Side Switch
- Single-Ended Power Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	150	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	26	A
		21	
		7.2 ^{b, c}	
		5.7 ^{b, c}	
Pulsed Drain Current	I _{DM}	50	
Continuous Source-Drain Diode Current	I _S	32	mJ
		4.5 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	20	
Single Pulse Avalanche Energy	E _{AS}	20	
Maximum Power Dissipation	P _D	64	W
		44	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{Stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	19	24	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	1.5	1.8	

Notes:

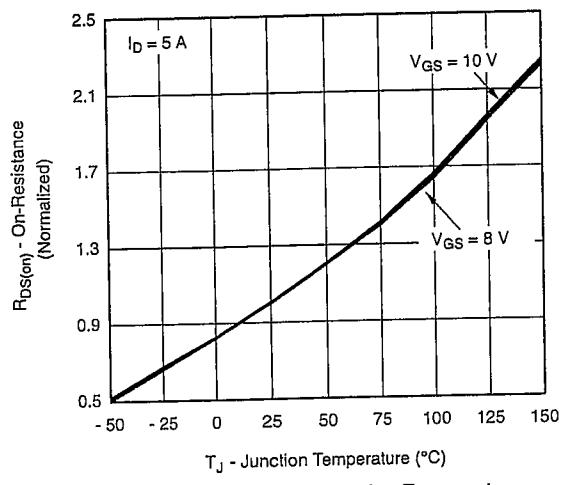
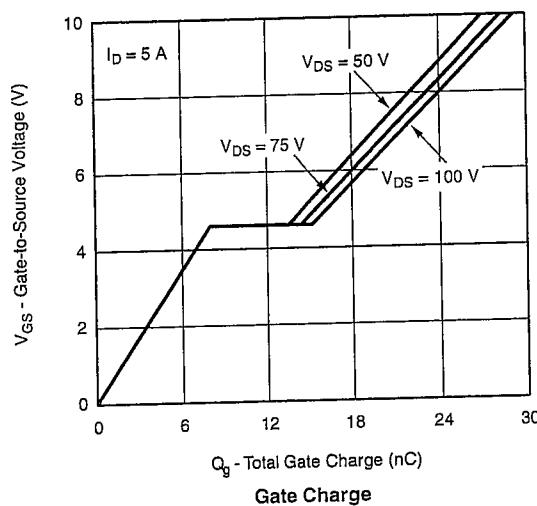
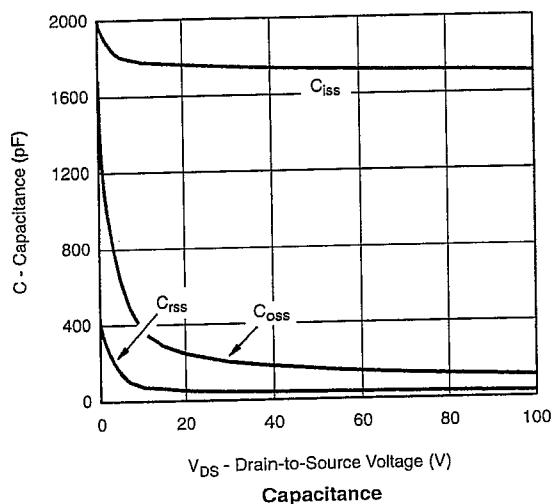
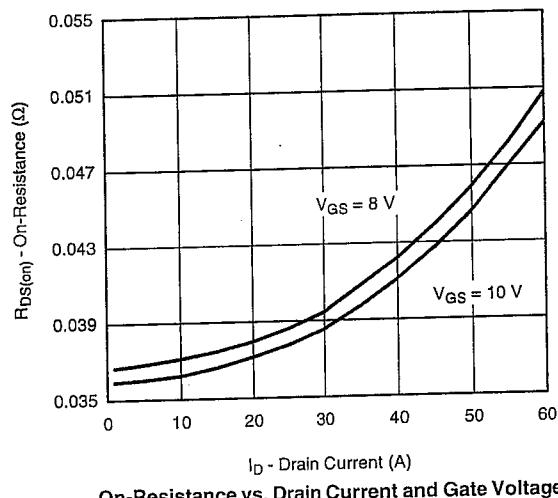
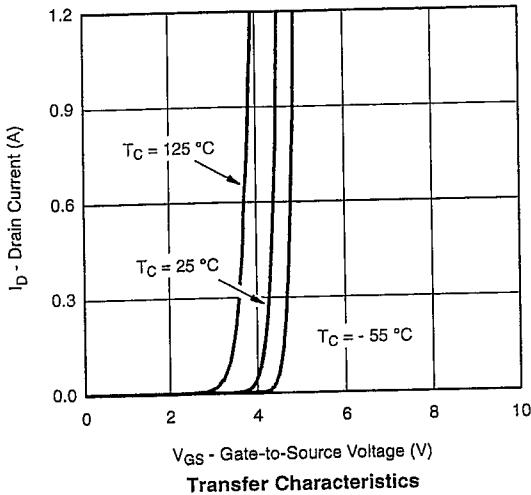
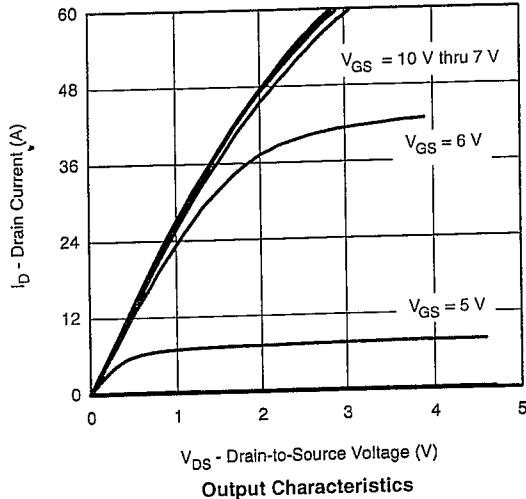
- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 65 °C/W.

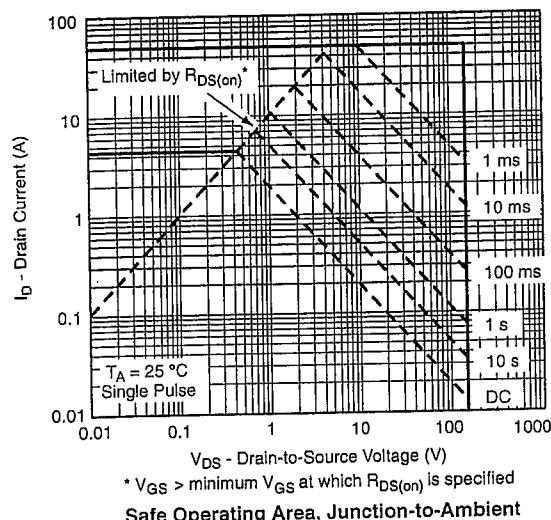
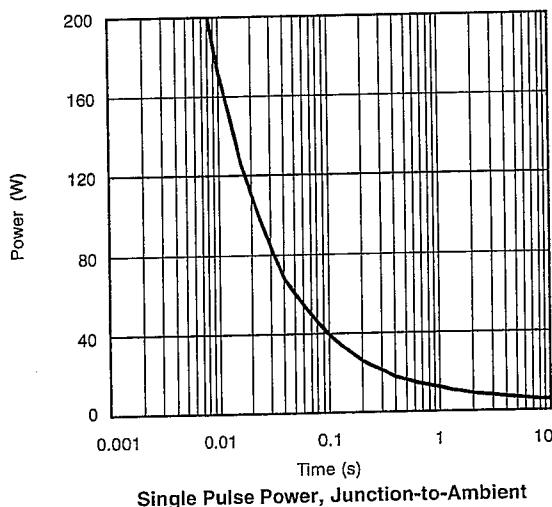
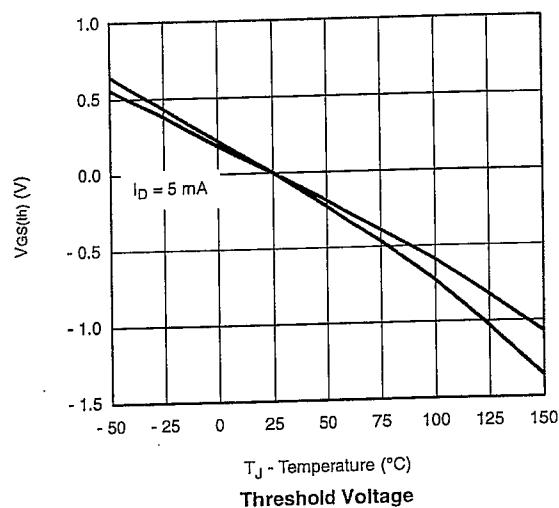
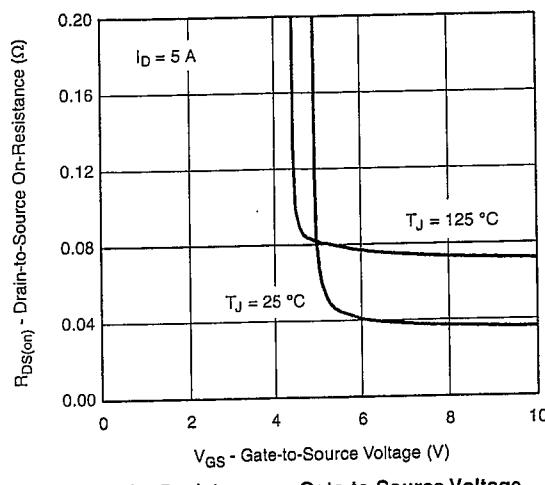
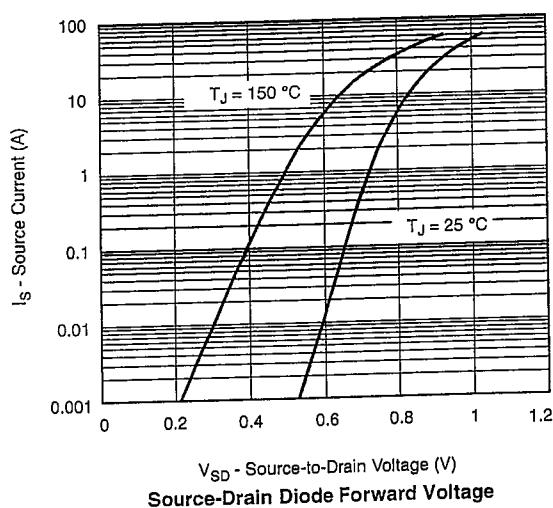
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	150			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		172		mV/ $^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 10		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2.5	4.5		V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$		± 100		nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 150 \text{ V}$, $V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 150 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$		10		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 10 \text{ V}$, $V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$		0.036	0.045	Ω
		$V_{GS} = 8 \text{ V}$, $I_D = 5 \text{ A}$		0.0375	0.047	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 5 \text{ A}$		23		S
Dynamic						
Input Capacitance	C_{iss}	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		1735		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			37		
Total Gate Charge	Q_g	$V_{DS} = 75 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$		28.5	43	nC
				23	35	
Gate-Source Charge	Q_{gs}	$V_{DS} = 75 \text{ V}$, $V_{GS} = 8 \text{ V}$, $I_D = 5 \text{ A}$		8		
Gate-Drain Charge	Q_{gd}			6.5		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		0.85	1.3	Ω
Turn-on Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$, $R_L = 10 \Omega$ $I_D \equiv 5 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		14	21	ns
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(\text{off})}$			22	33	
Fall Time	t_f			6	10	
Turn-On Delay Time	$t_{d(\text{on})}$			16	24	
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(\text{off})}$	$V_{DD} = 50 \text{ V}$, $R_L = 10 \Omega$ $I_D \equiv 5 \text{ A}$, $V_{GEN} = 8 \text{ V}$, $R_g = 1 \Omega$		20	30	ns
Fall Time	t_f			7	12	
Drain-Source/Body-Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			32	A
Pulse Diode Forward Current ^a	I_{SM}				50	
Body Diode Voltage	V_{SD}	$I_S = 3 \text{ A}$		0.77	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		63	95	ns
Body Diode Reverse Recovery Charge	Q_{rr}			110	165	nC
Reverse Recovery Fall Time	t_a			49		ns
Reverse Recovery Rise Time	t_b			14		

Notes:

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
 a. Guaranteed by design, not subject to production testing.

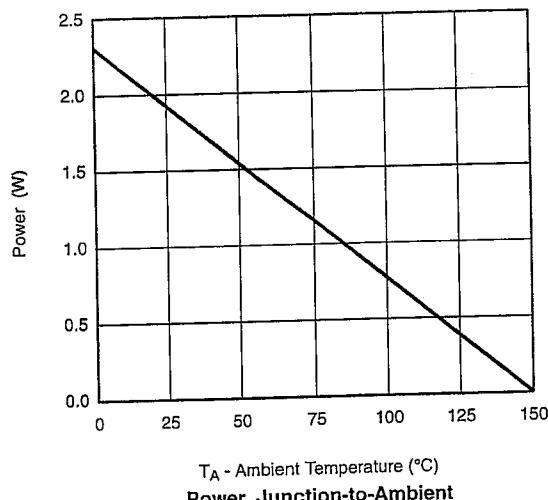
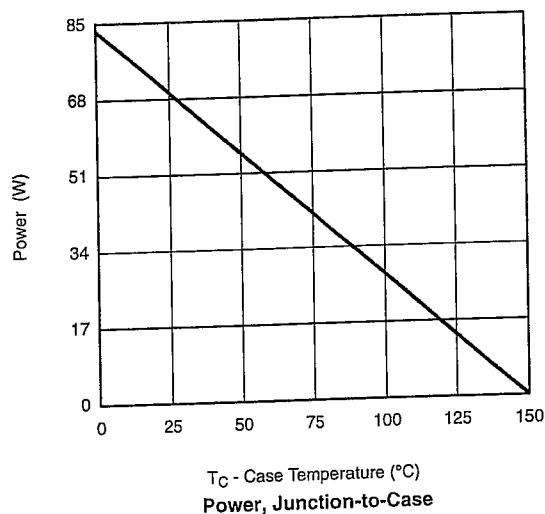
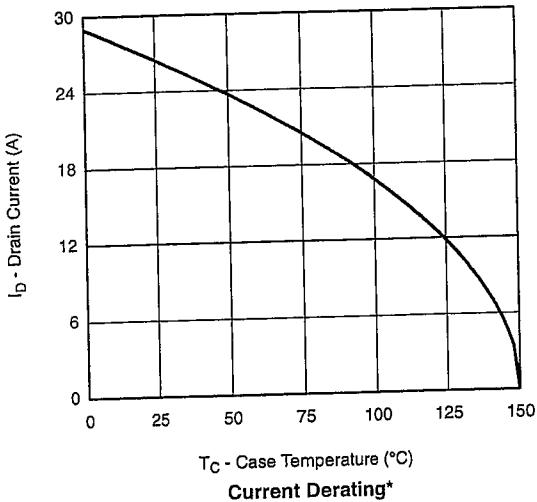
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

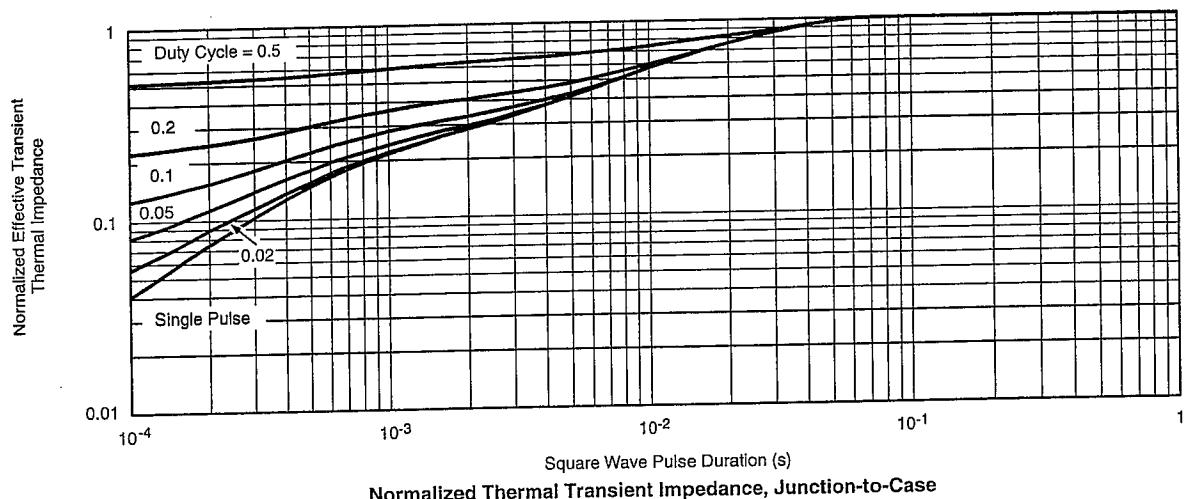
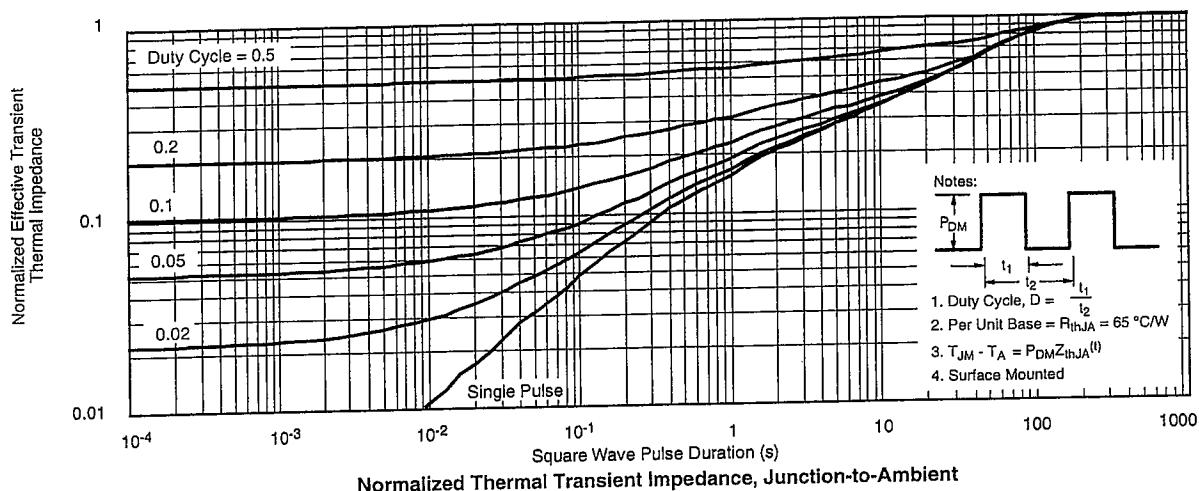
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si7430DP

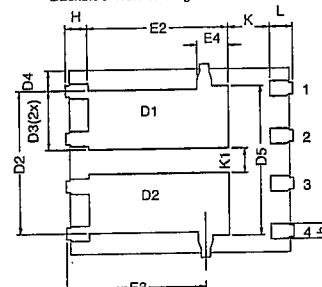
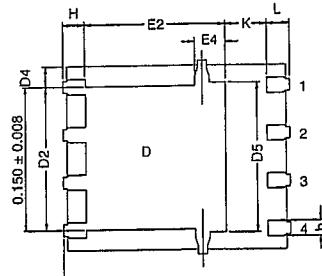
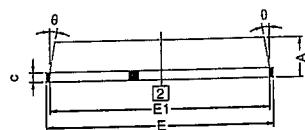
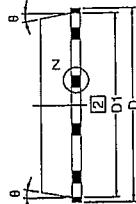
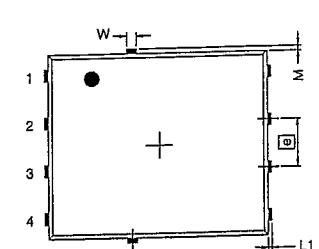
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74282.

PowerPAK® SO-8, (SINGLE/DUAL)



Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 TYP.			0.0225 TYP.		
D5	3.98 TYP.			0.157 TYP.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 TYP.			0.030 TYP.		
[e]	1.27 BSC			0.050 BSC		
K	1.27 TYP.			0.050 TYP.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

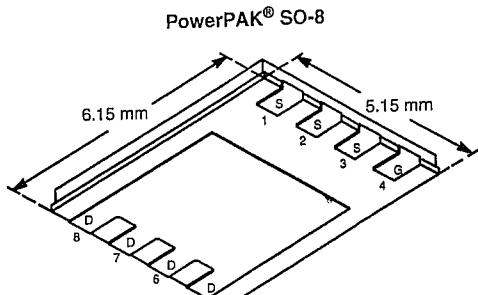
ECN: T10-0055-Rev. J, 15-Feb-10

DWG: 5881



N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
100	0.0087 at V _{GS} = 10 V	60	18.3 nC
	0.0094 at V _{GS} = 7.5 V	60	
	0.0115 at V _{GS} = 4.5 V	60	



Bottom View



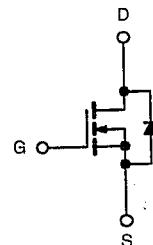
RoHS
COMPLIANT
HALOGEN
FREE

FEATURES

- Halogen-free According to IEC 61249-2-21
- Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- DC/DC Primary Side Switch
- Telecom/Server 48 V, Full/Half-Bridge dc-to-dc
- Industrial



N-Channel MOSFET

Ordering Information: SiR882DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	60 ^a	A
	T _C = 70 °C	55	
	T _A = 25 °C	17.6 ^{b, c}	
	T _A = 70 °C	13.9 ^{b, c}	
Pulsed Drain Current	I _{DM}	80	
Continuous Source-Drain Diode Current	T _C = 25 °C	60 ^a	
	T _A = 25 °C	4.9 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	30	
Single Pulse Avalanche Energy	E _{AS}	45	mJ
Maximum Power Dissipation	P _D	83	W
		53	
		5.4 ^{b, c}	
		3.4 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{slg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	1.0	1.5	

Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See solder profile (www.vishay.com/ppg273257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 65 °C/W.



SiR882DP

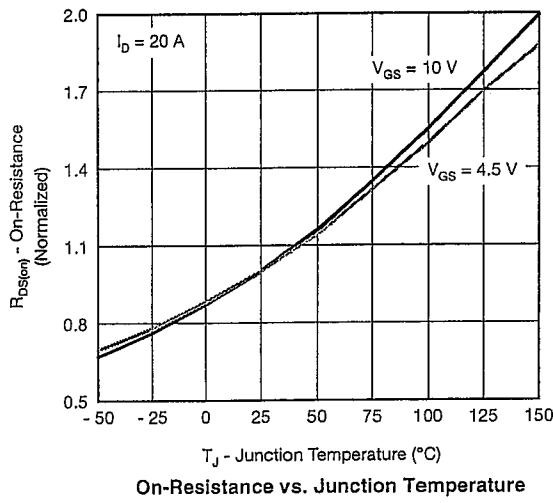
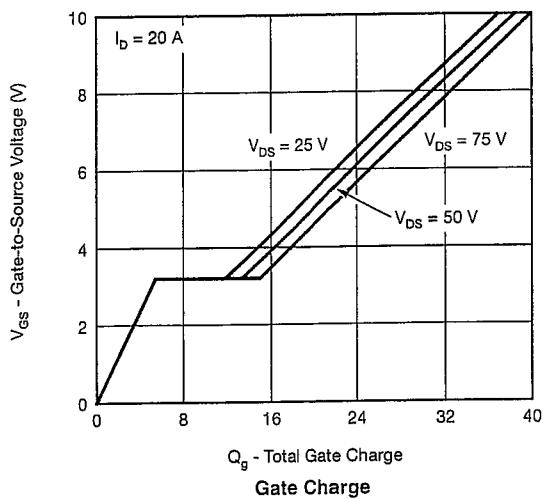
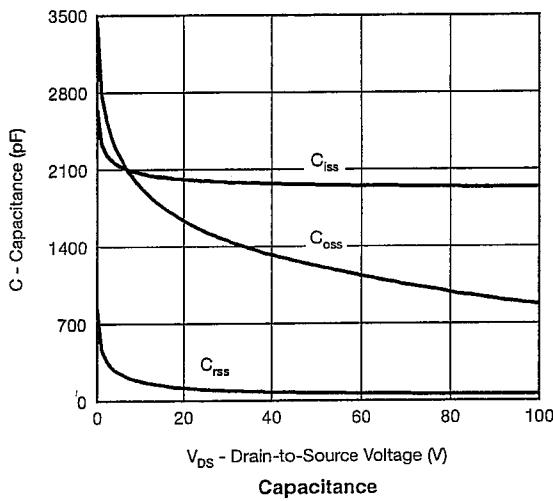
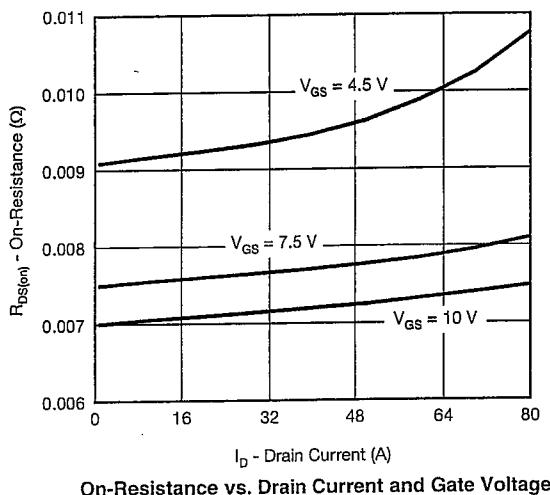
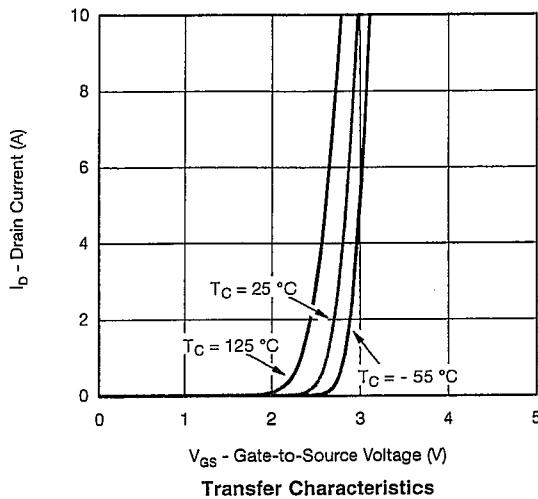
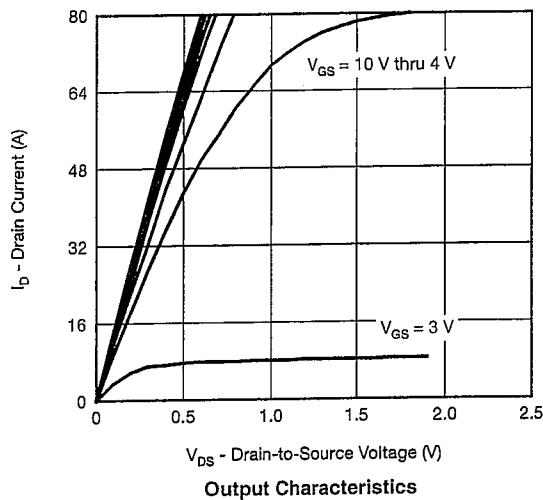
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SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)		Test Conditions	Min.	Typ.	Max.	Unit
Parameter	Symbol					
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$	50	- 5.8		mV/ $^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$					
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.2		2.8	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0071	0.0087	Ω
		$V_{GS} = 7.5 \text{ V}, I_D = 17 \text{ A}$		0.0076	0.0094	
		$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$		0.0092	0.0115	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ A}$		57		S
Dynamic						
Input Capacitance	C_{iss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	1930	1210	65	pF
Output Capacitance	C_{oss}					
Reverse Transfer Capacitance	C_{rss}					
Total Gate Charge	Q_g	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	38.5	58		nC
		$V_{DS} = 50 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 20 \text{ A}$	29	44		
Gate-Source Charge	Q_{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	18.3	27.5	5.5	
Gate-Drain Charge	Q_{gd}				7.8	
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.4	1.9	3.8	Ω
Turn-On Delay Time	$t_{d(on)}$				12	
Rise Time	t_r	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega$ $I_D \geq 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	12	24		ns
Turn-Off Delay Time	$t_{d(off)}$				36	
Fall Time	t_f				9	
Turn-On Delay Time	$t_{d(on)}$				13	
Rise Time	t_r	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega$ $I_D \geq 10 \text{ A}, V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	15	30		
Turn-Off Delay Time	$t_{d(off)}$				35	
Fall Time	t_f				8	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			60	A
Pulse Diode Forward Current ^a	I_{SM}				80	
Body Diode Voltage	V_{SD}	$I_S = 5 \text{ A}$		0.75	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	64	120	ns	
Body Diode Reverse Recovery Charge	Q_{rr}				80	
Reverse Recovery Fall Time	t_a				24	
Reverse Recovery Rise Time	t_b				40	

Notes:

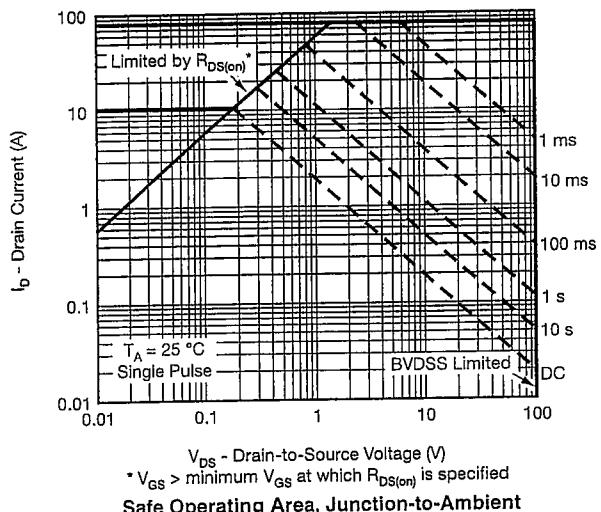
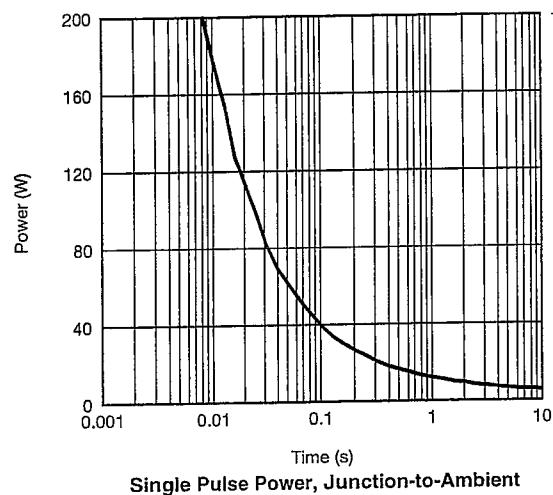
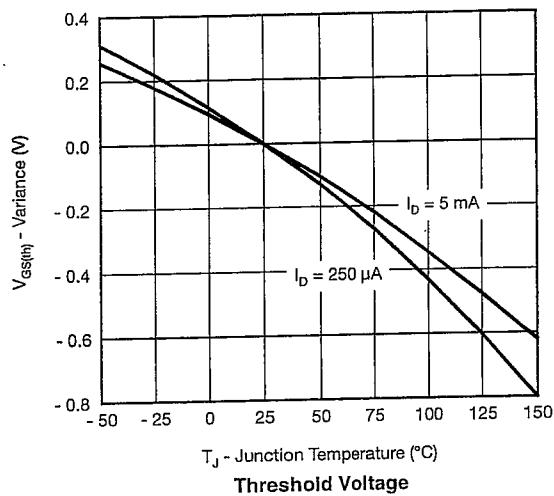
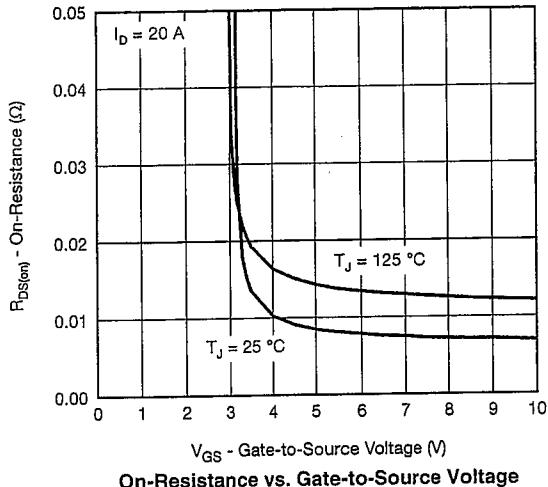
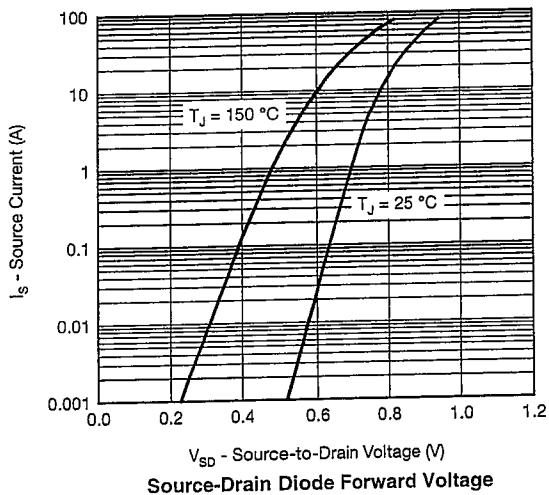
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

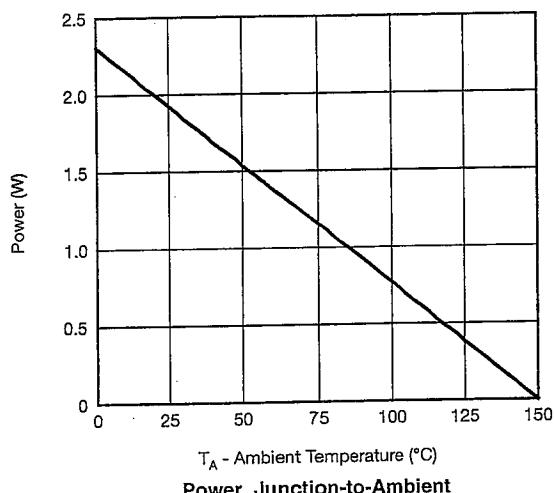
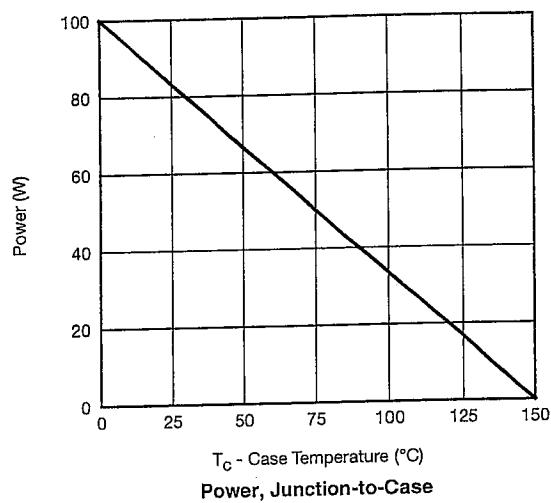
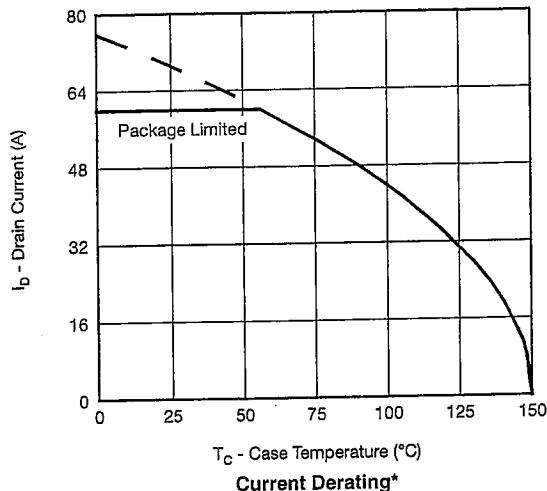
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

SiR882DP

Vishay Siliconix

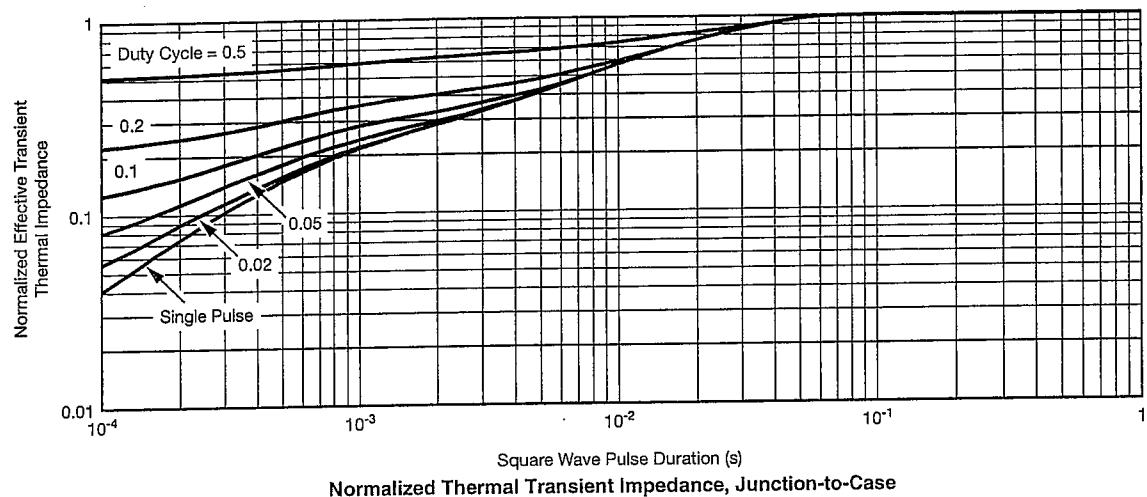
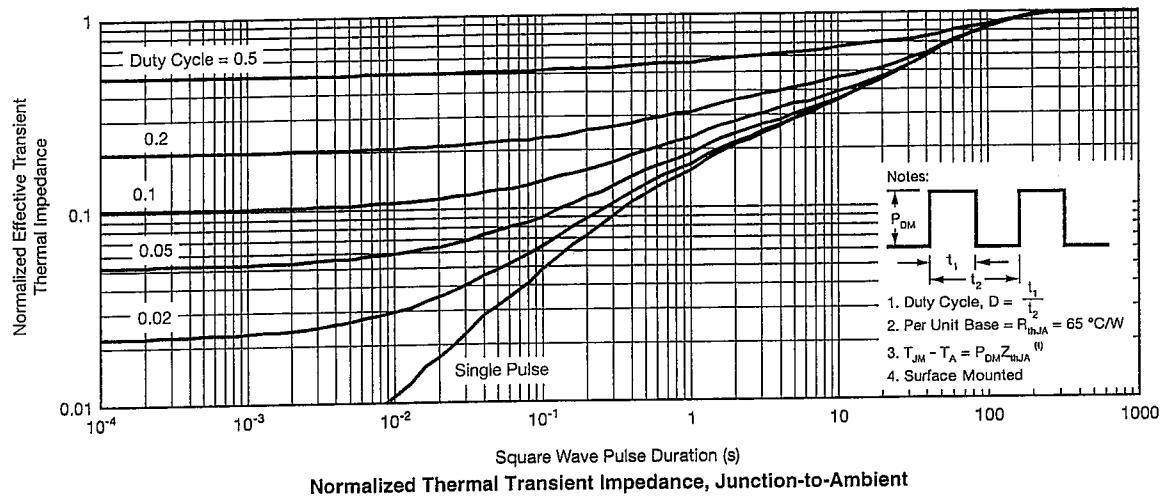
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiR882DP

Vishay Siliconix

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

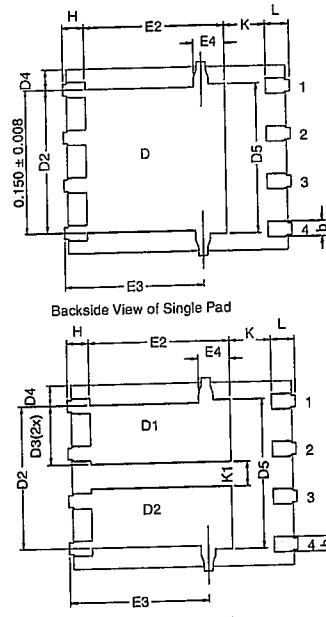
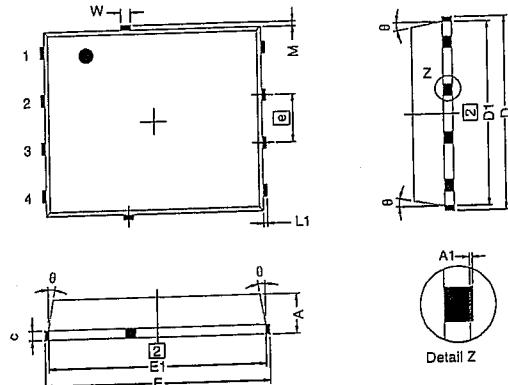
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/pgp26932.



Package Information

Vishay Siliconix

PowerPAK® SO-8, (SINGLE/DUAL)



Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 TYP.			0.0225 TYP.		
D5	3.98 TYP.			0.157 TYP.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 TYP.			0.030 TYP.		
[e]	1.27 BSC			0.050 BSC		
K	1.27 TYP.			0.050 TYP.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

ECN: T10-0055-Rev. J, 15-Feb-10

DWG: 5881



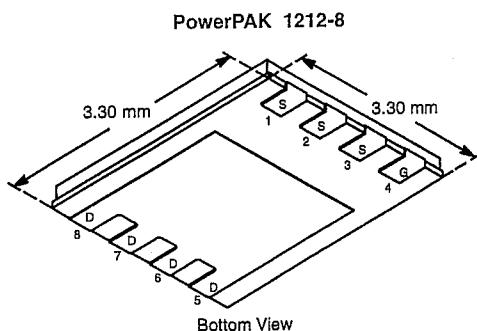
N12

Si7115DN

Vishay Siliconix

P-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
- 150	0.295 at V _{GS} = - 10 V	- 8.9 ^e	23.2 nC
	0.315 at V _{GS} = - 6 V	- 8.6 ^e	



Ordering Information:

Si7115DN-T1-E3 (Lead (Pb)-free)

Si7115DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

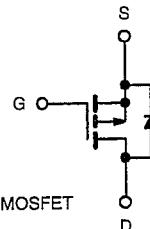
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1 mm Profile
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies
- H-Bridge High Side Switch for Lighting Application



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 150	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	- 8.9	A
	T _C = 70 °C	- 7.1	
	T _A = 25 °C	- 2.3 ^{a, b}	
	T _A = 70 °C	- 1.9 ^{a, b}	
Pulsed Drain Current	I _{DM}	- 15	
Continuous Source-Drain Diode Current	T _C = 25 °C	- 13	
	T _A = 25 °C	- 3 ^{a, b}	
Avalanche Current	I _{AS}	15	
Single-Pulse Avalanche Energy	E _{AS}	11.25	mJ
Maximum Power Dissipation	T _C = 25 °C	52	W
	T _C = 70 °C	33	
	T _A = 25 °C	3.7 ^{a, b}	
	T _A = 70 °C	2.4 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

Notes:

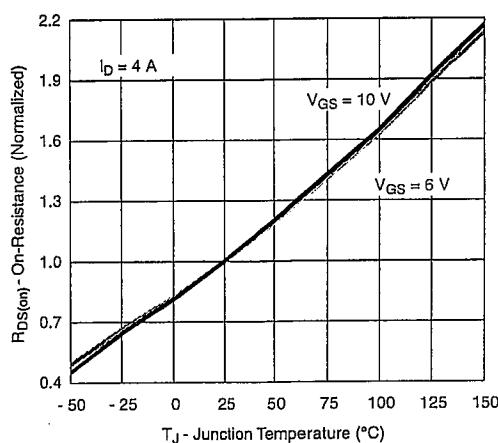
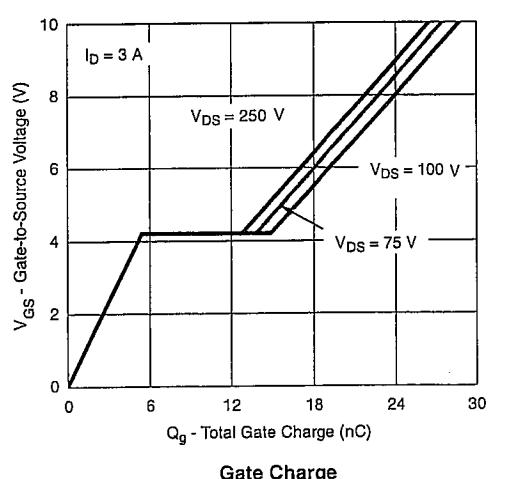
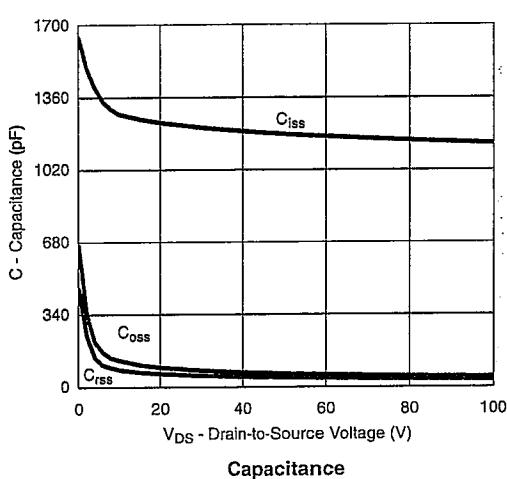
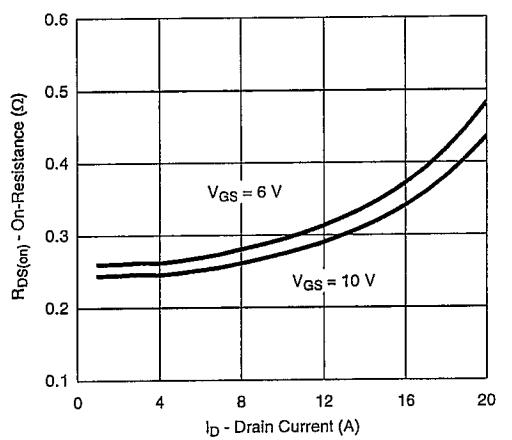
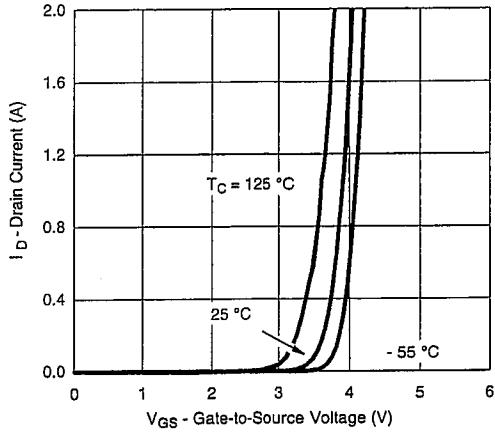
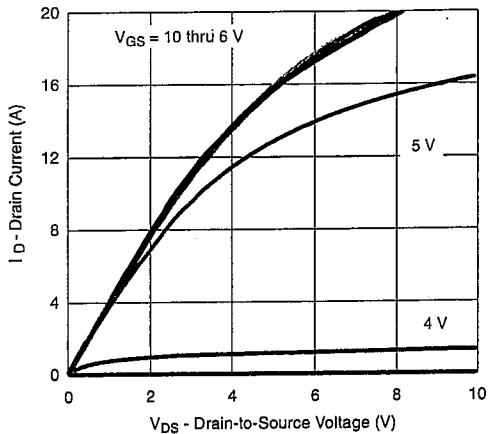
a. Surface mounted on 1" x 1" FR4 board.

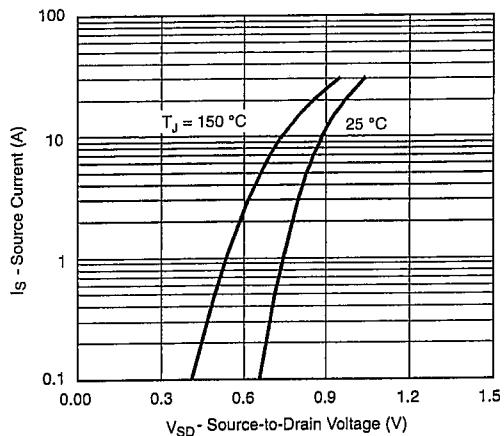
b. t = 10 s.

c. See solder profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

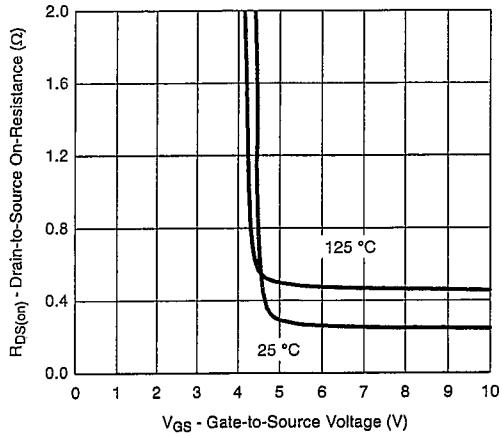
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Based on T_C = 25 °C.

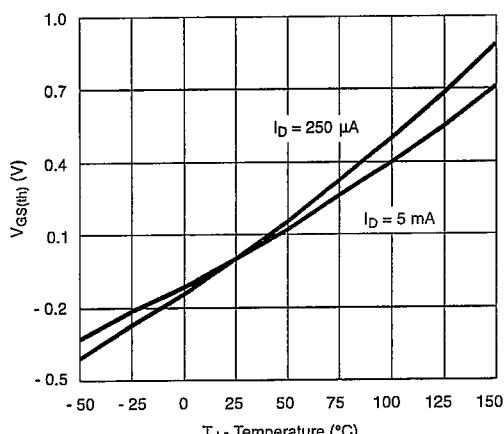
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

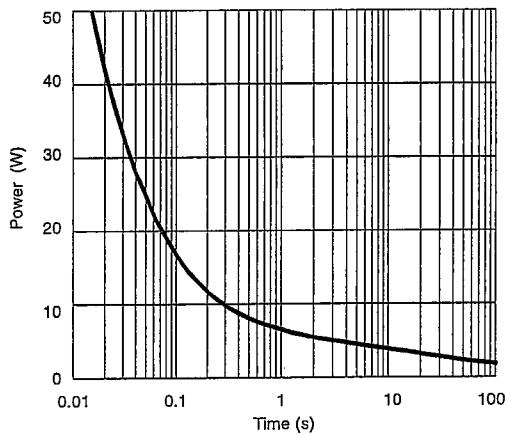
Source-Drain Diode Forward Voltage



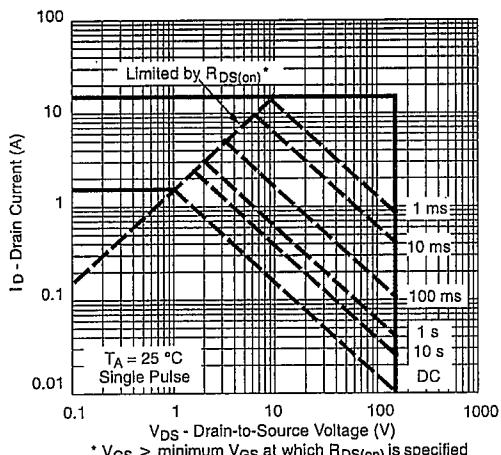
On-Resistance vs. Gate-to-Source Voltage



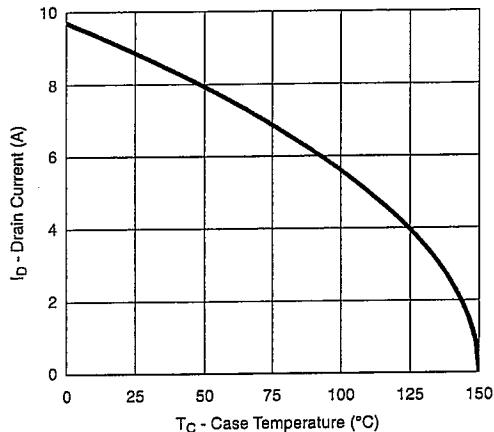
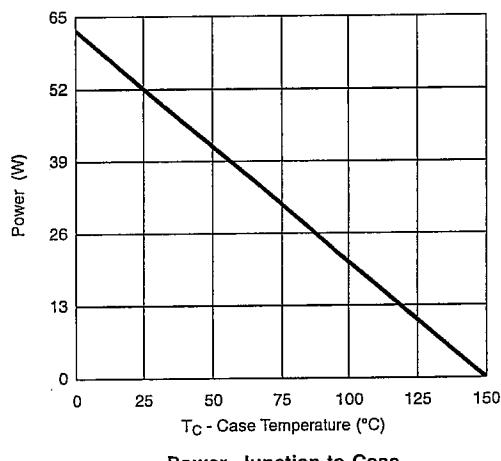
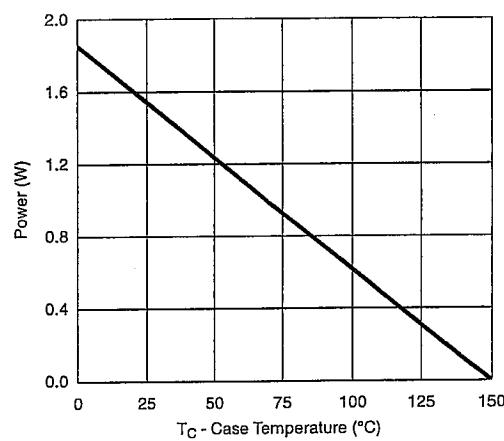
Threshold Voltage



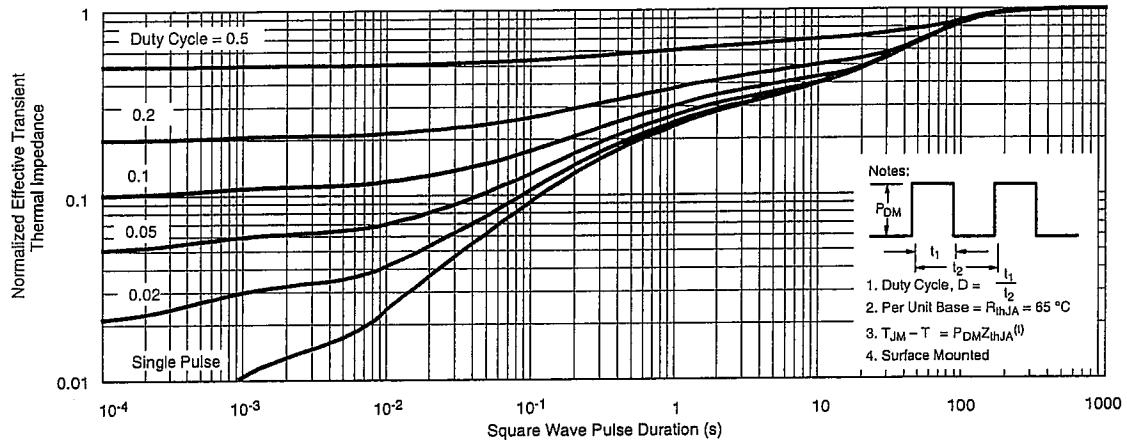
Single Pulse Power, Junction-to-Ambient



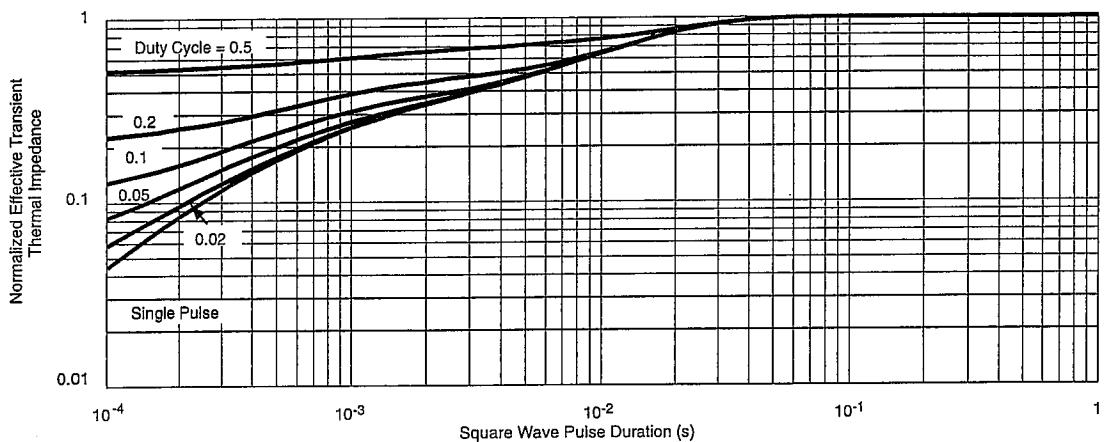
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power, Junction-to-Case

Power, Junction-to-Ambient

* The power dissipation PD is based on $T_J(\max) = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

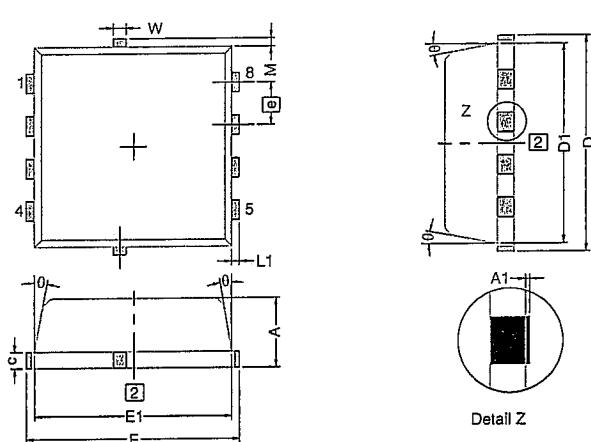
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Package Information

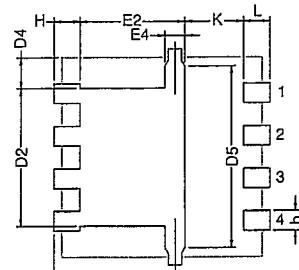
Vishay Siliconix

PowerPAK® 1212-8, (SINGLE/DUAL)

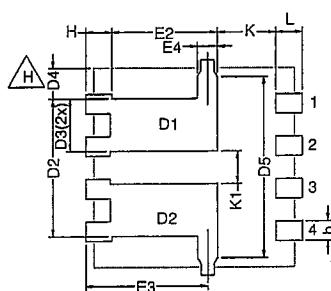


Notes:

1. Inch will govern
2. Dimensions exclusive of mold gate burrs
3. Dimensions exclusive of mold flash and cutting burrs



Backside View of Single Pad



Backside View of Dual Pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 TYP.			0.0185 TYP.		
D5	2.3 TYP.			0.090 TYP.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 TYP.			0.013 TYP.		
[e]	0.65 BSC			0.026 BSC		
K	0.86 TYP.			0.034 TYP.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

ECN: S10-0951-Rev. J, 03-May-10

DWG: 5882

CEL

U7

PHOTOCOUPLED PS2801-1, PS2801-4

HIGH ISOLATION VOLTAGE SSOP PHOTOCOUPLED

-NEPOC Series-

DESCRIPTION

The PS2801-1 and PS2801-4 are optically coupled isolators containing a GaAs light emitting diode and an NPN silicon phototransistor in a plastic SSOP for high density applications.

This package has shield effect to cut off ambient light.

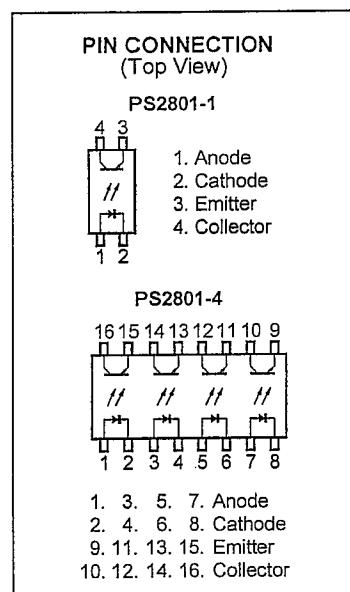
FEATURES

- High isolation voltage ($BV = 2\text{ }500\text{ Vr.m.s.}$)
- Small and thin package (4,16-pin SSOP, Pin pitch 1.27 mm)
- High collector to emitter voltage ($V_{CEO} = 80\text{ V}$)
- High-speed switching ($t_r = 3\text{ }\mu\text{s TYP.}, t_f = 5\text{ }\mu\text{s TYP.}$)
- Ordering number of tape product: PS2801-1-F3, F4, PS2801-4-F3, F4
- Pb-Free product
- Safety standards: PS2801-1, -4
 - UL approved: No. E72422
 - BSI approved: No. 8188, 8189
 - CSA approved: No. CA 101391
 - DIN EN60747-5-2 (VDE0884 Part2) approved: No. 40008902 (Option)

<R>

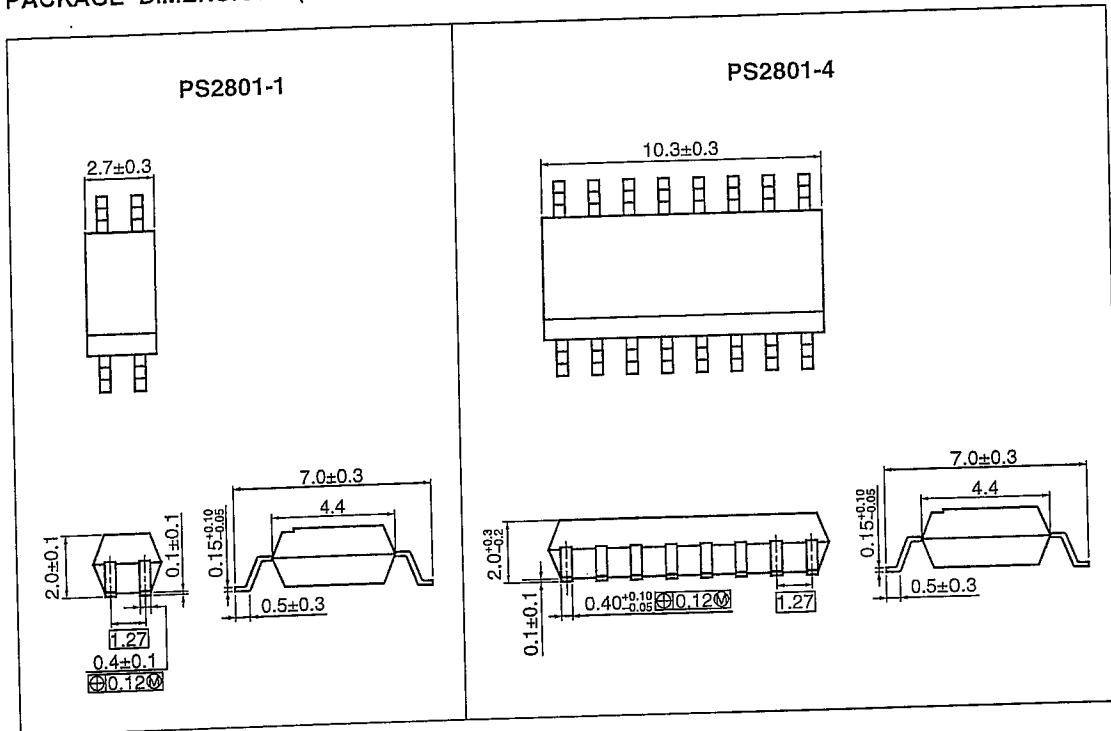
APPLICATIONS

- Programmable logic controllers
- Measuring instruments
- Power supply
- Hybrid IC



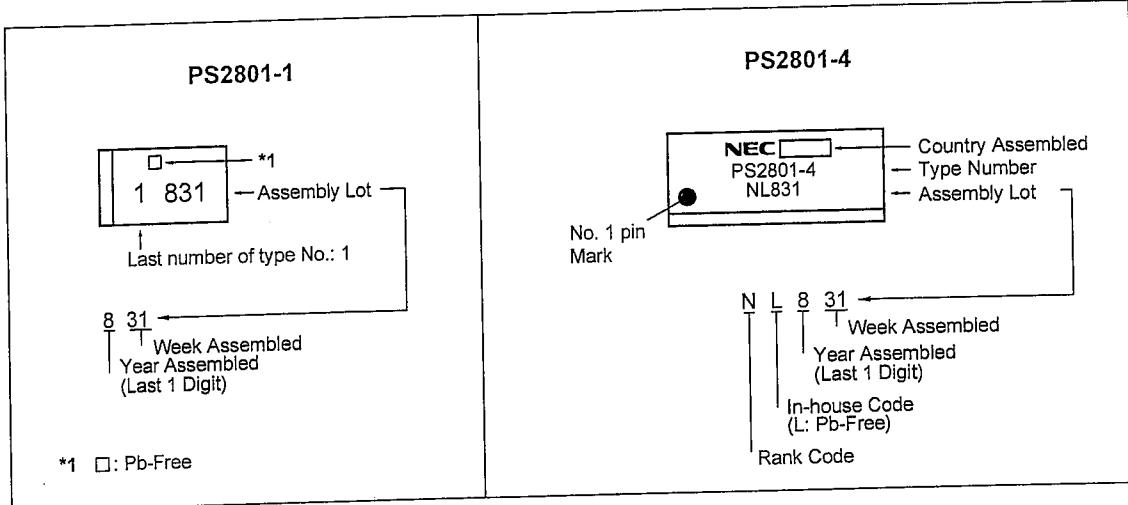
The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

PACKAGE DIMENSIONS (UNIT: mm)

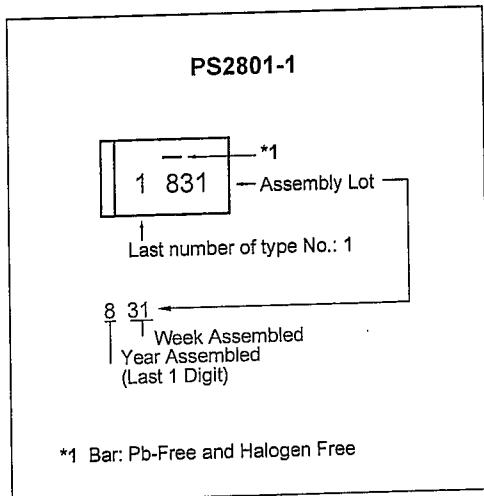


<R> MARKING EXAMPLE

Pb-Free



Special version (Pb-Free and Halogen Free)



<R> ORDERING INFORMATION

Part Number	Order Number	Solder Plating Specification	Packing Style	Safety Standard Approval	Application Part Number ^{*1}	
PS2801-1	PS2801-1-A	Pb-Free	50 pcs (Tape 50 pcs cut)	Standard products (UL, BSI, CSA approved)	PS2801-1	
PS2801-1-F3	PS2801-1-F3-A		Embossed Tape 3 500 pcs/reel			
PS2801-1-F4	PS2801-1-F4-A		50 pcs (Tape 50 pcs cut)	DIN EN60747-5-2 (VDE0884 Part2) Approved (Option)		
PS2801-1-V	PS2801-1-V-A		Embossed Tape 3 500 pcs/reel			
PS2801-1-V-F3	PS2801-1-V-F3-A		Magazine Case 45 pcs	PS2801-4		
PS2801-1-V-F4	PS2801-1-V-F4-A		Embossed Tape 2 500 pcs/reel			
PS2801-4	PS2801-4-A		Magazine Case 45 pcs		Standard products (UL, BSI, CSA approved)	
PS2801-4-F3	PS2801-4-F3-A		Embossed Tape 2 500 pcs/reel			
PS2801-4-F4	PS2801-4-F4-A		Embossed Tape 2 500 pcs/reel		DIN EN60747-5-2 (VDE0884 Part2) Approved (Option)	
PS2801-4-V	PS2801-4-V-A		Embossed Tape 2 500 pcs/reel			
PS2801-4-V-F3	PS2801-4-V-F3-A	Special version (Pb-Free and Halogen Free)	50 pcs (Tape 50 pcs cut)	Standard products (UL, BSI, CSA approved)	PS2801-1	
PS2801-4-V-F4	PS2801-4-V-F4-A		Embossed Tape 3 500 pcs/reel			
PS2801-1	PS2801-1Y-A		50 pcs (Tape 50 pcs cut)	DIN EN60747-5-2 (VDE0884 Part2) Approved (Option)		
PS2801-1-F3	PS2801-1Y-F3-A		Embossed Tape 3 500 pcs/reel			
PS2801-1-V	PS2801-1Y-V-A		Embossed Tape 3 500 pcs/reel			
PS2801-1-V-F3	PS2801-1Y-V-F3-A		Embossed Tape 3 500 pcs/reel			

*1 For the application of the Safety Standard, following part number should be used.

ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, $T_A = 25^\circ\text{C}$)

Parameter		Symbol	Ratings		Unit
			PS2801-1	PS2801-4	
Diode	Forward Current (DC)	I_F	50		mA/ch
	Reverse Voltage	V_R	6		V
	Power Dissipation Derating	$\Delta P_d/\text{°C}$	0.6	0.8	$\text{mW}/\text{°C}$
	Power Dissipation	P_d	60	80	mW/ch
	Peak Forward Current ^{*1}	I_{FP}	1		A/ch
Transistor	Collector to Emitter Voltage	V_{CEO}	80		V
	Emitter to Collector Voltage	V_{ECO}	6		V
	Collector Current	I_c	50		mA/ch
	Power Dissipation Derating	$\Delta P_c/\text{°C}$	1.2		$\text{mW}/\text{°C}$
	Power Dissipation	P_c	120		mW/ch
Isolation Voltage ^{*2}		BV	2 500		V.r.m.s.
Operating Ambient Temperature		T_A	-55 to +100		$^\circ\text{C}$
Storage Temperature		T_{stg}	-55 to +150		$^\circ\text{C}$

^{*1} PW = 100 μs , Duty Cycle = 1%^{*2} AC voltage for 1 minute at $T_A = 25^\circ\text{C}$, RH = 60% between input and output.

Pins 1-2 shorted together, 3-4 shorted together (PS2801-1).

Pins 1-8 shorted together, 9-16 shorted together (PS2801-4).

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Diode	Forward Voltage	V_F	$I_F = 5 \text{ mA}$		1.1	1.4	V
	Reverse Current	I_R	$V_R = 5 \text{ V}$			5	μA
	Terminal Capacitance	C_t	$V = 0 \text{ V}, f = 1.0 \text{ MHz}$		15		pF
Transistor	Collector to Emitter Dark Current	I_{CEO}	$V_{CE} = 80 \text{ V}, I_F = 0 \text{ mA}$			100	nA
Coupled	Current Transfer Ratio (I_C/I_F) ^{*1}	CTR	$I_F = 5 \text{ mA}, V_{CE} = 5 \text{ V}$	80		600	%
	Collector Saturation Voltage	$V_{CE(\text{sat})}$	$I_F = 10 \text{ mA}, I_C = 2 \text{ mA}$			0.3	V
	Isolation Resistance	R_{I-O}	$V_{I-O} = 1.0 \text{ kVdc}$	10^{11}			Ω
	Isolation Capacitance	C_{I-O}	$V = 0 \text{ V}, f = 1.0 \text{ MHz}$		0.4		pF
	Rise Time ^{*2}	t_r	$V_{CC} = 5 \text{ V}, I_C = 2 \text{ mA}, R_L = 100 \Omega$		3		μs
	Fall Time ^{*2}	t_f			5		

^{*1} CTR rank (PS2801-1 only)

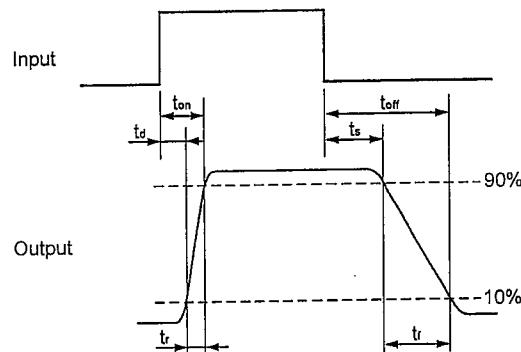
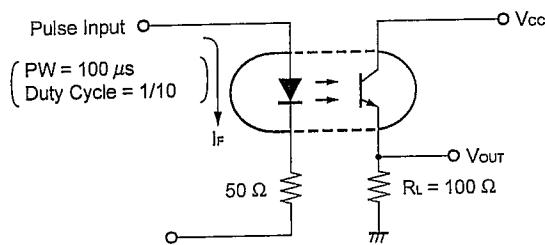
K : 300 to 600 (%)

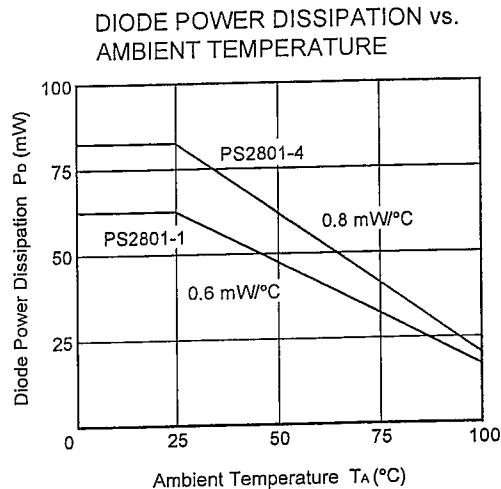
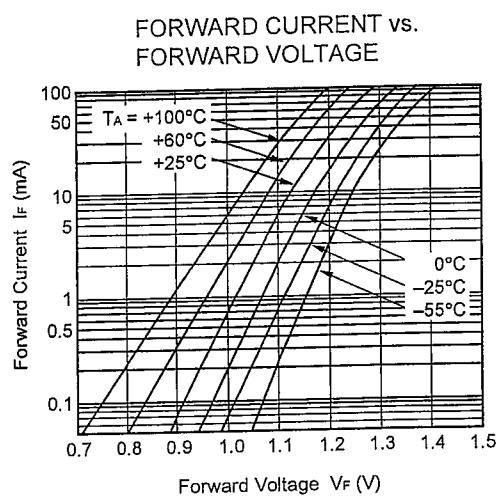
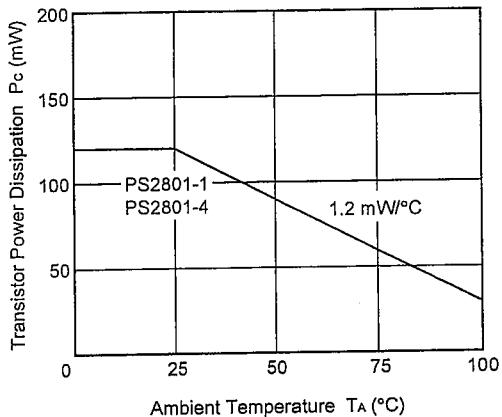
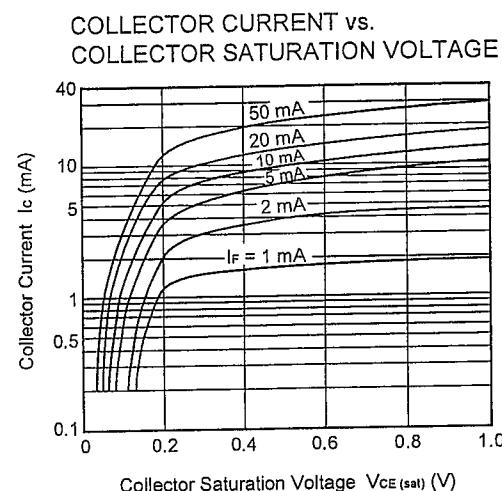
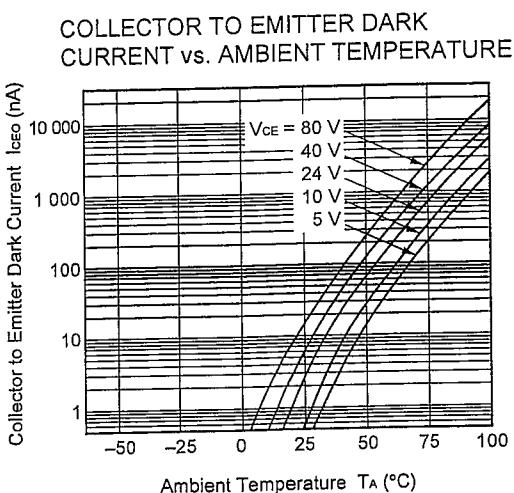
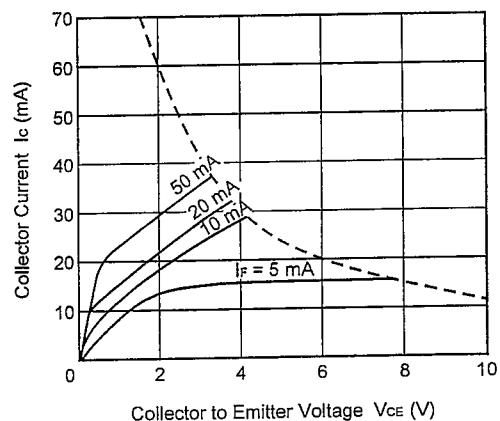
P : 150 to 300 (%)

L : 100 to 300 (%)

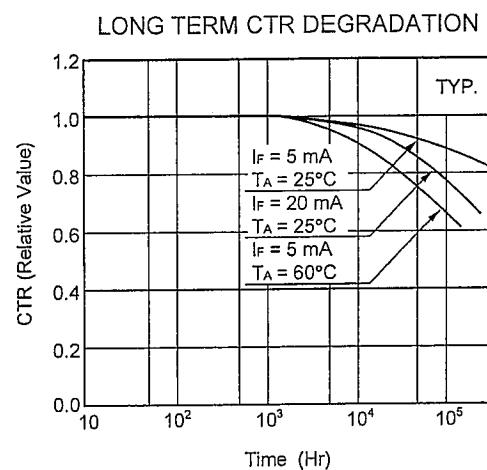
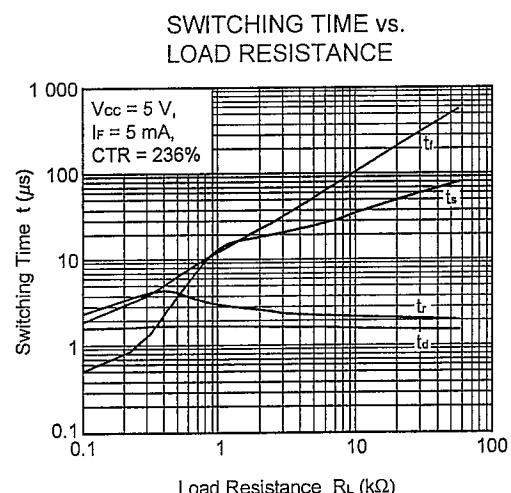
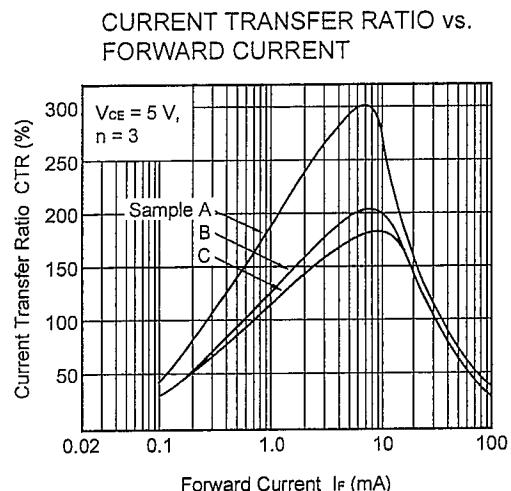
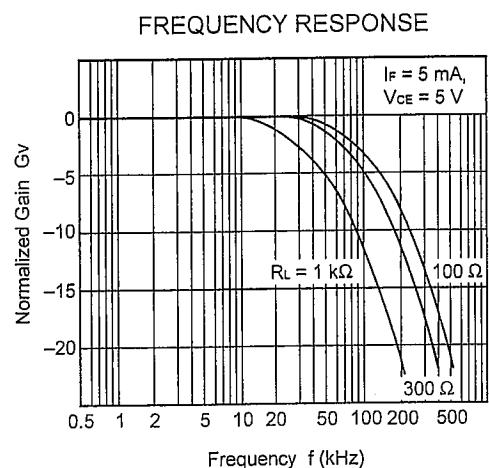
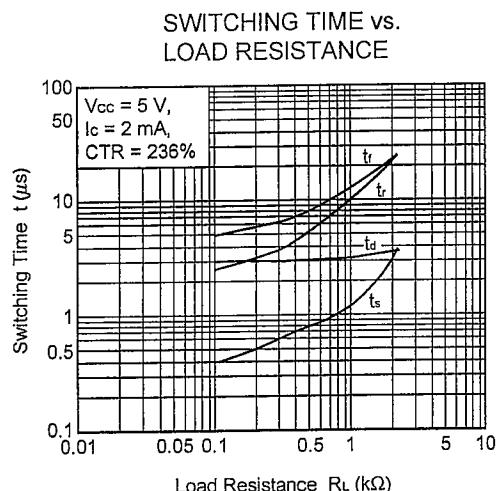
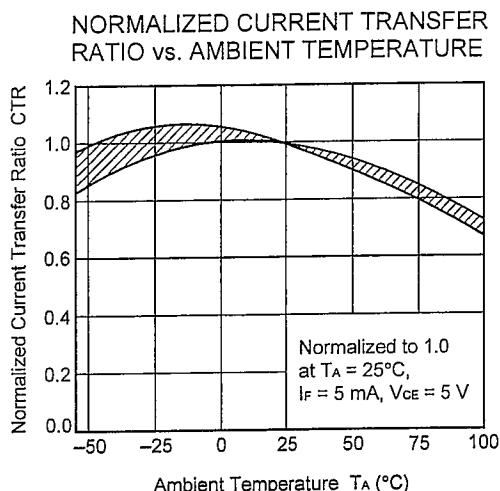
N : 80 to 600 (%)

<R> *2 Test circuit for switching time



TYPICAL CHARACTERISTICS (Unless otherwise specified, $T_A = 25^\circ\text{C}$)TRANSISTOR POWER DISSIPATION
vs. AMBIENT TEMPERATURECOLLECTOR CURRENT vs.
COLLECTOR TO Emitter VOLTAGE

Remark The graphs indicate nominal characteristics.



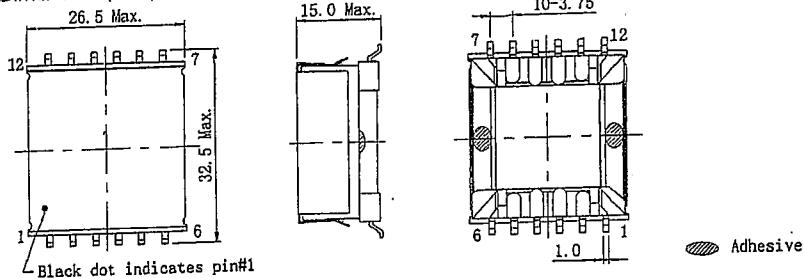
Remark The graphs indicate nominal characteristics.

PRELIMINARY SPECIFICATION

TYPE
CEFD2513B

1.A.PPEARANCE

1-1.DIMENSION(mm)

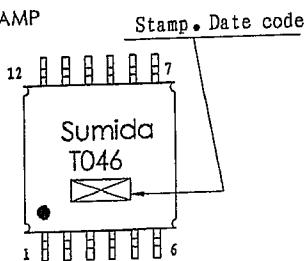


* TERMINALS SHOULD BE MEASURED EXCLUDING THE LENGTH OF THE SOLDERED POINT.

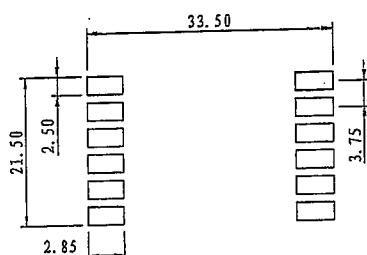
* DIMENSIONS WITHOUT TOLERANCE APPROX.

* THE COPLANARITY IS 0.15mm MAX.

1-2.STAMP



1-3. RECOMMENDED PCB LAYOUT (mm)



RoHS

Compliance
Cd:Max.0.01wt%
others: Max.0.1wt%

 sumida

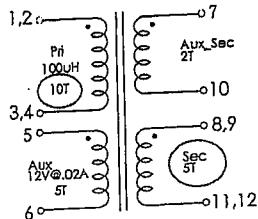
MADE: 2011-12-26			PART NO.		
CHK.	CHK.	DRG.	SUMIDA CODE		
			SAMPLE NO.	SPEC.NO. 10393-T046	2/3
			FIRST ISSUE		

PRELIMINARY SPECIFICATION

TYPE
CEFD2513B

2.COIL SPECIFICATION

2-1.CONNECTION (BOTTOM)



* DOTS INDICATES THE POLARITY.

2-2.ELECTRICAL CHARACTERISTICS (AT 25°C, UNLESS OTHERWISE SPECIFIED)

ITEM	SPECIFICATION	MEASURING CONDITIONS
INDUCTANCE (1,2-3,4)	100 μ H \pm 20%	100kHz, 310mV, TIE(1+2,3+4)
LEAKAGE INDUCTANCE (1,2-3,4)	2.5 μ H MAX. 250nH MAX.	250kHz, 310mV, TIE(1+2,3+4,5+6+7+8+9+10+11+12)
D.C.R. (1,2-3,4)	30m Ω MAX. (TYP. 23m Ω)	TIE(1+2,3+4)
D.C.R. (8,9-11,12)	5.0m Ω MAX. (TYP. 3.6m Ω)	TIE(8+9,11+12)
D.C.R. (5-6)	130m Ω MAX.	
D.C.R. (7-8)	5 σ m Ω MAX.	
URNS RATIO (1-3):(2-4):(5-6):(7-10):(8,9-11,12)	2:2:1:1:1 \pm 3%	30kHz, 1V
HI-POT (1,2,3,4,5,6-7,8,9,10,11,12)	AC 1500Vrms	1 Minute, 50Hz, 0.5mA

* TESTING EQUIPMENT HP-4284A OR EQUIVALENT.

3.NOTE

* OPERATING TEMPERATURE RANGE:-40°C +105°C .(INCLUDING COIL TEMPERATURE RISE.)

* STORAGE TEMPERATURE RANGE:-40°C +105°C .

* THIS PART CROSS TO PULSE PA3412NL.

NOTE :

SPEC. NO.
10393-T046

3/3

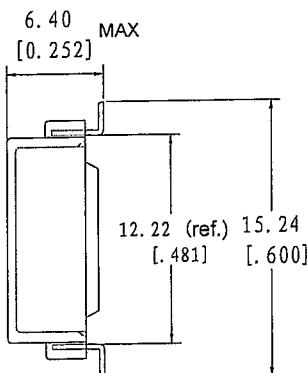
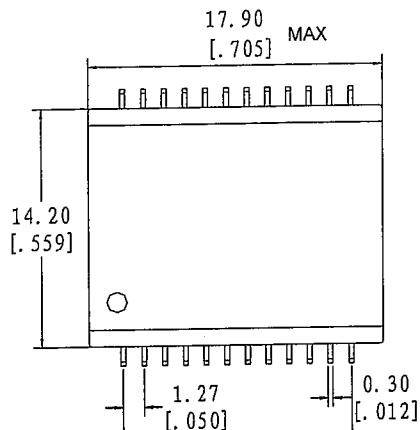
T2

PRELIMINARY SPECIFICATION

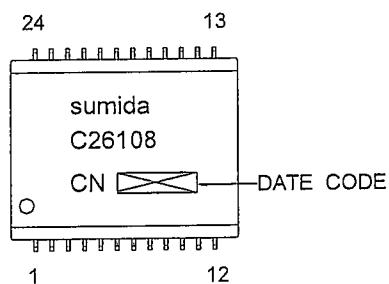
TYPE CLP176 (temp)

1. APPEARANCE

1-1. DIMENSIONS (mm[inch])



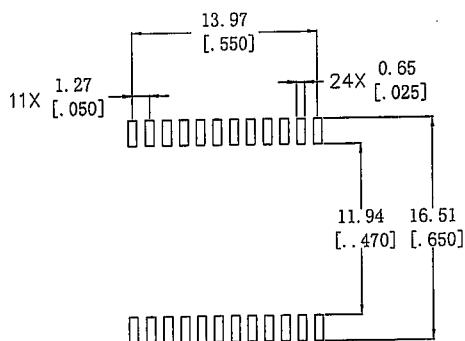
1-2. STAMP



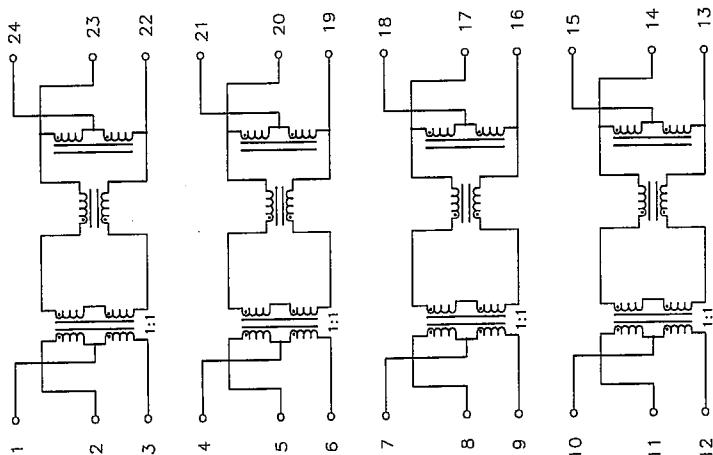
* ALL DIMENSIONS ARE $\pm 0.25\text{mm}$ [0.01inch].

* TERMINALS SHOULD BE MEASURED EXCLUDING THE LENGTH OF THE SOLDERED POINT.

1-3. RECOMMENDED LAND PATTERNS (mm[inch])



2-1. SCHEMATIC



MADE : 2011-05-03			PART NO.	C26108		
CHK.	CHK.	DRG.	SUMIDA CODE			
			SAMPLE NO.		SPEC. NO.	SI11-016
			FIRST ISSUE			2/3

PRELIMINARY SPECIFICATION

TYPE
CLP176 (temp)

2-2. ELECTRICAL CHARACTERISTICS

		MEASURING CONDITIONS
1. INDUCTANCE	350uH MIN.	100kHz, 100mV, 8mA DC bias
2. TURNS RATIO	1:1±2%	100kHz, 100mV
3. INSERTION LOSS	-1. 1dB MIN.	0. 1MHz
	-1. 0dB MIN.	100MHz
4. RETURN LOSS	-18. 0dB MAX.	30MHz
	-12. 0dB MAX.	60MHz
	-12. 0dB MAX.	80MHz
	-10. 0dB MAX.	100MHz
5. CROSSTALK	-43. 0dB MAX.	30MHz
	-37. 0dB MAX.	60MHz
	-33. 0dB MAX.	100MHz
6. HIPOT	AC 1500Vrms	50/60Hz, 0. 5mA, 6s
7. PoE CURRENT	2. 4A MAX	2 CHANNELS

3. REMARKS

PACKING SPECIFICATION: TAPE & REEL PACKAGING.

OPERATION TEMPERATURE: -40°C~85°C

NOTE :

SPEC. NO.

SI11-016

3/3