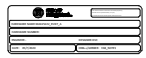
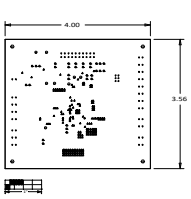
REVISIONS			
REV	DESCRIPTION	APPROVED	DATE





LAMINATION DIAGRAM				
LAYER NUMBER	LAYER NAME	COPPER THICKNESS OZ (INCH)	DIELECTRIC THICKNESS (INCH)	DIELECTRIC MATERIAL
1	TOP	1 OZ, 0.0014"		FOIL
			0.10	ISOLA 370HR/EQUIVALENT
2	INTERNAL2	1 OZ, 0.0014"		
			0.10	ISOLA 370HR/EQUIVALENT
3	INTERNAL3	1 OZ, 0.0014"		
			0.10	ISOLA 370HR/EQUIVALENT
4	BOTTOM	1 OZ, 0.0014"		FOIL
THE FINISHED PCB THICKNESS TO BE:			0.062IN" +/- 0.010"	

DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS					
FIGURE	SIZE	TOLERANCE	PLATED	QTY	NOTES
A	12.0	+3.0/-10.0	PLATED	183	
B	18.0	+3.0/-16.0	PLATED	7	
C	33.46	+3.0/-3.0	PLATED	20	
D	36.0	+3.0/-3.0	PLATED	32	
E	37.4	+3.0/-3.0	PLATED	6	
F	39.37	+3.0/-3.0	PLATED	40	
G	45.28	+3.0/-3.0	PLATED	10	
H	62.99	+3.0/-3.0	PLATED	8	
I	125.0	+3.0/-3.0	PLATED	4	

NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES [EXCEPT WHERE NOTED].

MATERIAL: (USE CHICKED ITEMS FOR MATERIAL)

2. BOARD MATERIAL:
   - (X) ISOLA 370HR OR EQUIVALENT
   - ( ) ISOLA FR408HR OR EQUIVALENT
   - ( ) NELCO-4000-13
   - ( ) MEGTRON 6
   - ( ) ROGERS 4350B
   - ( ) ROGERS 4350C
   - ( ) OTHER _____

3. THE PCB SHALL BE FABRICATED TO IPC-6012, TYPE II, CLASS 2.
   WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2, CURRENT REVISIONS.
4. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796
   WITH FLAMMABILITY RATING OF 94V-O.
5. OVERALL BOARD THICKNESS REFER TO LAMINATION DIAGRAM. TOLERANCE APPLIES
   AFTER ALL LAMINATION AND PLATING PROCESSES. IT IS TO BE MEASURED FROM
   TOP PCB METAL TO BOTTOM PCB METAL UNLESS OTHERWISE SPECIFIED.
6. BOW & TWIST NOT TO EXCEED 0.0075 IN. (0.75%) PER LINEAR INCH.
   BOW & TWIST SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.

TOOLING:

7. PHOTOTOOL CIRCUITRY PER ENCLOSED GERBER RS274X OR ODB++ FORMAT FILE.
   DRILL LOCATION AND SIZE CONTROLLED BY EXCELLON CNC DRILL FILE.
8. IMPEDANCE REQUIREMENTS: IF NO STACKUP IS DEFINED, THE VENDOR IS ALLOWED TO ADJUST THE DIELECTRIC
   THICKNESS AND TRACE WIDTHS TO MEET THE IMPEDANCE REQUIREMENT. IF SPECIFIED, VENDOR MUST FOLLOW AND
   MEET THE REQUIREMENTS LISTED IN THE IMPEDANCE TABLE. ANY ADJUSTMENTS MADE TO THE DEFINED STACKUP,
   TRACE WIDTH & SPACING THAT IMPACT THE REQUIREMENTS MUST HAVE WRITTEN APPROVAL FROM MAXIM.
9. ALL TRACES FILLETED OPTION TO ENHANCE RELIABILITY AT PAD JUNCTIONS
   WHERE SPACING PERMITS. UNLESS OTHERWISE SPECIFIED:
   - ( ) FILLETED
   - (X) NOT FILLETED
10. LAYER TO LAYER REGISTRATIONS SHALL BE WITHIN .003 INCHES.
    LEGEND TO LEGEND +/- 0.007 INCHES.
11. FINISHED COPPER WEIGHT/THICKNESS:
    - (X) REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIREMENTS.
      THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER
      WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE, UNLESS OTHERWISE SPECIFIED.
    - ( ) OTHER _____

SURFACE FINISH:

12. USE CHICKED ITEMS FOR PLATING
    - ( ) ELECTRODEPOSITED HARD GOLD PLATE, TYPE 1 (99.7% MIN GOLD), GRADE C
      (KNOOP HARDNESS 130-200), CLASS 1 (50-100 MICRO INCHES THICK) IN ACCORDANCE WITH MIL-G-45204C.
      GENERAL SURFACING REQUIREMENTS MUST MEET ANSI/IPC-A-600(CURRENT REV) SECTION 4.0,
      CLASS 3 (50-100 MICROINCHES THICK) OVER ELECTRODEPOSITED NICKEL PLATE
      IN ACCORDANCE WITH ANSI/IPC-A-600, SECTION 4.0, CLASS 3 (200-400 MICROINCHES THICK).
    - (X) FINISH CONDUCTOR SURFACES: IMMERSION GOLD, 1.54-3.94 MICRO INCHES OVER
      118-236 MICRO INCHES MINIMUM OF ELECTROLESS NICKEL.
    - ( ) FINGERS TO BE GOLD PLATED.
    - ( ) OTHER _____

13. DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN .005 DTP UNLESS SPECIFIED.
    MINIMUM BARREL PLATING OF .001 IN. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO
    HINDER PROPER SOLDER WICKING. BARREL RELIEF ON SOLDERMASK ALLOWED ON UNPLUGED VIA IN PAD HOLES.

SOLDERMASK:

14. SOLDERMASK OVER BARE COPPER OR BARE GOLD (BOTH SIDES) WITH LIQUID PHOTO IMAGEABLE (LPI) INK
    - (X) CUSTOM MASIM TRAL SOLDER MASK. PANTONE #526C
    - ( ) OTHER _____

SILKSCREEN:

15. APPLY SILKSCREEN USING A NON-CONDUCTIVE EPOXY INK
    - (X) WHITE
    - ( ) OTHER _____

16. VENDOR LOGO & DATE CODE REQUIREMENT. DATE CODE FORMAT MUST BE YYWW ONLY
    - (X) PLACE ON BOTTOM LEGEND LAYER. IF NO BOTTOM LEGEND SUPPLIED, CREATE BOTTOM LEGEND LAYER TO ADD.
    - ( ) PLACE ON TOP LEGEND LAYER. IF NO TOP LEGEND SUPPLIED,CREATE TOP LEGEND LAYER TO ADD.
    - ( ) OTHER _____

TESTING:

17. FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE.
    (REQUIRED UNLESS OTHERWISE SPECIFIED IN QUOTE)
    THE PCB SHALL HAVE A VERIFICATION STAMP.
18. A TIME DOMAIN REFLECTOMETER REPORT FOR EACH IMPEDANCE CONTROLLED LAYER AND A CERTIFICATE
    OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING
    CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES
    IS ACCEPTABLE, ALL OTHER INSTANCES MUST BE REPORTED.

MISCELLANEOUS:

19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE PLATED SHUT WITH COPPER WHEN
    USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE FILLED
    WITH NON-CONDUCTIVE EPOXY. UNLESS OTHERWISE SPECIFIED.
20. FOR ALL DRILL INFORMATION REFER TO DRILL CHART.
    - ( ) NON-CONDUCTIVE EPOXY. FILL AND CAP ALL 0.XXXX INCH DRILLED VIAS.
    - ( ) SILVER. FILL AND CAP ALL 0.XXXX INCH DRILLED VIAS.
21. FINISHED SURFACE CONTACTS AND FILLED VIAS TO BE FREE OF ANY PITS, SCRATCHES PROBE MARKS
    OR OTHER DEFORMITIES THAT COULD EFFECT THE APPEARANCE AND PERFORMACE OF THE CONTACT
    SURFACE. CONTACTS ARE TO BE AS FLAT AS POSSIBLE. NOT TO EXCEED +/- 0.001" OF FLATNESS.
22. THIEVING:
    - ( ) SUPPLIER MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS ON THIS DESIGN.
    - (X) SUPPLIER MAY NOT ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS ON THIS DESIGN.
23. PENALTY
    - ( ) PENALTS TO BE INSTALLED BY FABRICATOR.
    - ( ) PENALTS NOT TO BE INSTALLED BY FABRICATOR.
    - (X) NOT APPLICABLE.

TOLERANCES UNLESS OTHERWISE SPECIFIED

FRACTIONS +/- 1/64 | DECIMALS .XX +/- .01, .XXX +/- .005 | ANGLES +/- 1°

MATERIAL: SEE NOTES

FINISH: SEE NOTES

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DRAWN BY:DVC	DATE: 05/7/2020
CHECKED BY:	DATE:
APPR. BY:	DATE:
APPR. BY:	DATE:

maxim integrated

HARDWARE NAME: MAX25222_EVKIT_A

HARDWARE NUMBER: XX-XXXXX-XXX | REV A

NOT TO SCALE | TEMPLATE REV: | SHEET 1 OF 1