

# DRC CHECKLIST AND INITIAL RELEASE FORM

## Job Name: MAX20051 Evkit Rev:

**Evkit Engineer: Greg Fattig Date:** **3/26/2014**

**SCHEMATIC CHECKLIST**

**Engineer’s schematic \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_** **[]**

### Parts list complete \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []

### Package footprints identified \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []

**Mechanical specs for non-standard \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

### Critical or high-current traces identified \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []

#### Job folder created \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []

## All components marked with value and size (if needed) \_\_\_\_\_\_\_\_\_\_\_ []

**All components marked with a reference designation \_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Pins labeled on all multi-pin components \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Component pin outs verified \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Polarized components marked \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Lower case k for resistor and u,p for capacitors. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**All text legible \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**No text is covered by lines or other text \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**All excess text removed \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Excessive trace angles removed \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

## Job name, revision and data verified \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []

**PRINTED CIRCUIT BOARD LAYOUT CHECKLIST**

### Component footprints verified (check with specification)\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []

**EVKE approves the component placement \_\_\_\_\_\_\_\_\_** **[]** **Date:3/26/2014**

**Perform Design Rule Check.**

1. **Check Footprint decal with bill of material \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**
   1. **Special board house require []**
   2. **Check main IC (U1) footprint with IOS or check package code []**
2. **Copper layer checks**

**Board layout electrically matches the schematic \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Board layout matches the schematic manual check \_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**All transistors and FETs connected correctly \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**All multi-pin component pin sequence verified \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Special conditions checked: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**3. Continuity checks complete \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**4. Clearance checks complete**

**Pad-Pad, Pad-Trace, Trace-Trace clearance** **(0.008)X Minimum Pad size over Drill size**  **(0.015)****X**

**Silkscreen/Soldermask checks :**

**All solder mask are properly open for all components; special condition solder mask open check, is there dual footprint, short resistors, UCSP, BGA .etc.. []**

**All component designators properly placed \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Pins identified on multi-pin headers \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Polarized diodes and capacitors properly marked \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Pin 1 identified on multi-pin parts \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

**Excess text removed \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []**

### Boiler plate data correct \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ []

**Remove “For viewing purpose only ……..etc ……….” []**

**Maxim logo, Board identification, Revision level, Date. []**

**All changes completed, All checks completed, Tape out approval.**

**PCB Designer:**  **Date: 3/26/2014 PCB Manager: Date: 3/26/2014**



**EVKE: \_\_\_\_Greg Fattig\_\_\_\_\_\_\_\_\_\_ [] Date: \_\_\_3/26/2014\_\_**

**EVKE [ GF ] please initial if you are signing for all.**

**DE: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ [] Date: \_\_\_\_\_\_\_\_\_\_\_\_**

**CAE: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ [] Date: \_\_\_\_\_\_\_\_\_\_\_\_**

**(signatures above will indicate that the engineer has checked the schematic/layout with care, all connection are correct and no change is to be made to the schematic/layout.)**

**Gerber package included items check**

**Board Specification [ ]**

**Silkscreen Top [ ] Bottom [ ]**

**Solder Masks Top CSP?? [ ] Bottom [ ]**

**Layers Top [ ] Bottom [ ] Inner [ ]**

**Fabrication plot [ ] Instruction layer profile [ ]**

**Save Gerber zip file to Network Drive [ ]**

**Gerber check verify \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ [ ]**

**PDF for Marcom [] Test fixture []**