ADSP-BF537 EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
One Technology Way
Norwood, Mass. 02062-9106

ANALOG DEVICES

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Printed in the USA.

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The EZ-KIT Lite evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The ADSP-BF537 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The ADSP-BF537 EZ-KIT Lite evaluation system had been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

CONTENTS

PREFACE

EZ-KIT LITE HARDWARE REFERENCE

PREFACE

Thank you for purchasing the ADSP-BF537 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

The Blackfin processor family embodies a new type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and 8-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-BF537 Blackfin processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C and ADSP-BF537 assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF537 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF537 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to `http://www.analog.com/dsp/tools/`.

ADSP-BF537 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The ADSP-BF537 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF537 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.

- The linker restricts a users program to 20 KB of internal memory for code space with no restrictions for data space.

The board features:

- Analog Devices ADSP-BF537 processor
  - Core performance to 600 MHz
  - External bus performance to 133 MHz
  - 182-pin Mini-BGA package
  - 25 MHz crystal CLKIN oscillator
- Synchronous Dynamic Random Access Memory (SDRAM)
  - MT48LC32M8 - 64 MB (8M x8-bits x 4 banks) x 2 chips
- Flash Memory
  - 4MB (2M x 16-bits)
- Analog Audio Interface
  - AD1871 96 kHz analog-to-digital codec (ADC)
  - AD1854 96 kHz digital-to-audio codec (DAC)
  - 1 input stereo jack
  - 1 output stereo jack
- Ethernet Interface
  - 10-BaseT (10 Mbits/sec) and 100-BaseT (100 Mbits/sec) Ethernet Medium Access Controller (MAC)
  - SMSC LAN83C185 device
- Controller Area Network (CAN) Interface
  - Philips TJA1041 high-speed CAN transceiver

- National Instruments Educational Laboratory Virtual Instrumentation Suite Interface (ELVIS)
  - LabVIEW™-based virtual instruments
  - Multifunction data acquisition device
  - Bench-top workstation and prototype board
- Universal Asynchronous Receiver/Transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - `DB9` female connector
- LEDs
  - 10 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 6 general purpose (amber), and 1 USB monitor (amber)
- Push Buttons
  - 5 push buttons: 1 reset, 4 programmable flags with debounce logic
- Expansion Interface
  - All processor signals
- Other Features
  - JTAG ICE 14-pin header

The EZ-KIT Lite board has flash memory with a total of 4 MB. The flash memory can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. For more information, see "Flash Memory" on page 1-9. The board also has 64 MB of SDRAM, which can be used by the user at runtime.

SPORT0 interfaces with the audio circuit, facilitating development of audio signal processing applications. SPORT0 also connects to an off-board connector for communication with other serial devices. For information about SPORT0, see "SPORT0 Audio Interface" on page 2-3.

The UART of the processor connects to an RS232 line driver and a DB9 female connector, providing an interface to a PC or other serial device.

Additionally, the EZ-KIT Lite board provides access to all of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. For information about the expansion interface, see "Expansion Interface" on page 2-7.

Purpose of This Manual

The *ADSP-BF537 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes the operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF537 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

EZ-KIT Lite users should use this manual in conjunction with the *Getting Started with ADSP-BF537 EZ-KIT Lite*, which familiarizes users with the hardware capabilities of the evaluation system and demonstrates how to access these capabilities in the VisualDSP++ environment.

The product software installation is detailed in the *VisualDSP++ Installation Quick Reference Card*.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-BF537 Blackfin Processor Hardware Reference* and *Blackfin Processor Instruction Set Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user's or getting started guides. For the locations of these documents, see "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "Using EZ-KIT Lite" on page 1-1
  Describes the EZ-KIT Lite functionality from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, "Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.

- Appendix B, "Schematics" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.

This appendix is not part of the online Help. The online Help viewers should go to the PDF version of the *ADSP-BF537 EZ-KIT Lite Evaluation System Manual* located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics. Alternatively, the schematics can be found on the Analog Devices Web site, `www.analog.com/processors`.

What's New in This Manual

This is the first edition of the *ADSP-BF537 EZ-KIT Lite Evaluation System Manual*.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the Embedded Processing and DSP products Web site at `http://www.analog.com/processors/technicalSupport`
- E-mail tools questions to `dsptools.support@analog.com`
- E-mail processor questions to `dsp.support@analog.com`
- Phone questions to **1-800-ANALOGD**

- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:

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Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
USA
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Supported Processors

This evaluation system supports the Analog Devices ADSP-BF537 Blackfin embedded processors.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at `www.analog.com`. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit `www.myanalog.com` to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and DSPs, visit our Web site at `www.analog.com/processors`, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
  `dsp.support@analog.com`
- Fax questions or requests for information to
  1-781-461-3010 (North America)
  +49 (89) 76 903-557 (Europe)
- Access the FTP Web site at
  `ftp ftp.analog.com` or `ftp 137.71.23.21`
  `ftp://ftp.analog.com`

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF536/ADSP-BF537 Embedded Processor Data Sheet	General functional description, pinout, and timing.
ADSP-BF537 Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions.
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions.

Table 2. Related VisualDSP++ Publications

Title	Description
ADSP-BF537 EZ-KIT Lite Evaluation System Manual	Description of the hardware capabilities of the evaluation system; description of how to access these capabilities in the VisualDSP++ environment.
VisualDSP++ User's Guide	Description of VisualDSP++ features and usage.
VisualDSP++ Assembler and Preprocessor Manuals	Description of the assembler function and commands.
VisualDSP++ C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors.
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands.
VisualDSP++ Loader Manual	Description of the loader/splitter function and commands.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

`http://www.analog.com/processors/resources/technicalLibrary`

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary `.PDF` files of most manuals are provided in the `Docs` folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
`.CHM`	Help system files and manuals in Help format
`.HTM` or `.HTML`	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the `.HTML` files requires a browser, such as Internet Explorer 4.0 (or higher).
`.PDF`	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the `.PDF` files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows® Explorer, or the Analog Devices Web site.

Accessing Documentation From VisualDSP++

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and navigate to the VisualDSP++ documentation via the **Start** menu.

To view ADSP-BF537 EZ-KIT Lite Help, which is part of the VisualDSP++ Help system, use the **Contents** or **Search** tab of the Help window.

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (`.CHM`) are located in the `Help` folder, and `.PDF` files are located in the `Docs` folder of your VisualDSP++ installation CD-ROM. The `Docs` folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-BF537 EZ-KIT Lite evaluation system.

Accessing Documentation From Web

Download manuals at the following Web site:
`http://www.analog.com/processors/resources/technicalLibrary/manuals`.

Select a processor family and book title. Download archive (.ZIP) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call **1-603-883-2430**. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto http://www.analog.com/salesdir/continent.asp.

Hardware Tools Manuals

To purchase EZ-KIT Lite and In-Circuit Emulator (ICE) manuals, call **1-603-883-2430**. The manuals may be ordered by title or by product number located on the back cover of each manual.

Processor Manuals

Hardware reference and instruction set reference manuals may be ordered through the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**), or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.

Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**); they also can be downloaded from the Web site.

To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 USING EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF537 EZ-KIT Lite evaluation system.

- "Ethernet Interface" on page 1-11
  Describes the on-board Fast Ethernet Medium Access Controller interface.
- "ELVIS Interface" on page 1-11
  Describes the on-board National Instruments Educational Laboratory Virtual Instrumentation Suite interface.
- "Audio Interface" on page 1-12
  Describes the on-board audio circuit.
- "LEDs and Push Buttons" on page 1-13
  Describes the board's general-purpose IO pins and buttons.
- "Background Telemetry Channel" on page 1-14
  Highlights the advantages of the Background Telemetry Channel feature of VisualDSP++.
- "VisualDSP++ Interface" on page 1-14
  Describes the trace, target options, and breakpoint restriction facilities of the EZ-KIT Lite system available through VisualDSP++.

For more detailed information about programming the ADSP-BF537 Blackfin processor, see the documents referred to as "Related Documents".

Package Contents

Your ADSP-BF537 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF537 EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*

- CD containing:
  - VisualDSP++ software
  - ADSP-BF537 EZ-KIT Lite debug software
  - USB driver files
  - Example programs
  - ADSP-BF537 *EZ-KIT Lite Evaluation System Manual* (this document)
- Universal 7V DC power supply
- 7-foot Ethernet crossover cable
- 7-foot Ethernet Patch cable
- 6-foot 3.5 mm male-to-male audio cable
- 3.5 mm headphones
- 10-foot USB 2.0 cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The ADSP-BF537 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, switches, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.

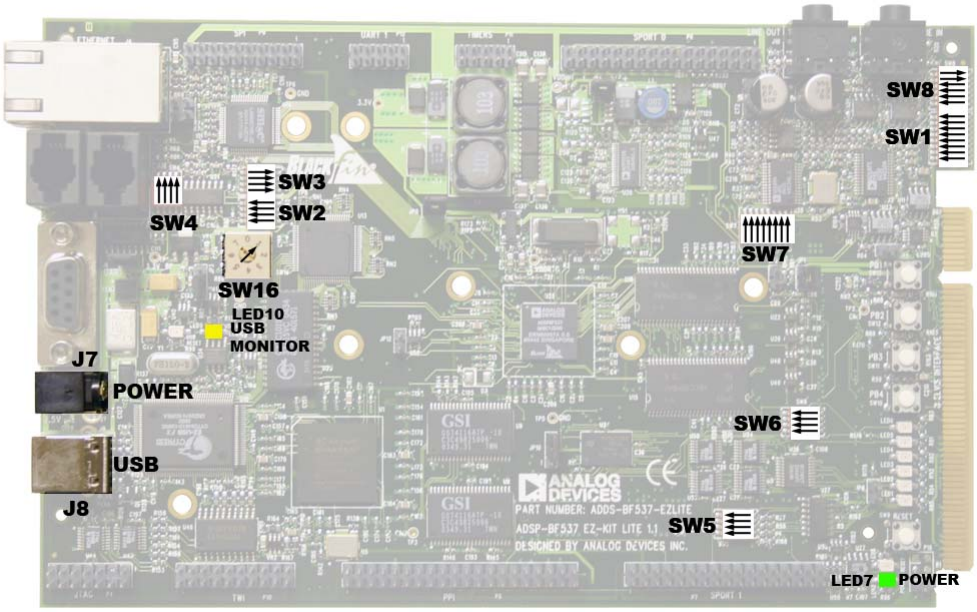

Figure 1-1. EZ-KIT Lite Hardware Setup

Installation and Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

1. Verify that the yellow USB monitor LED (`LED10`, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. From the **Start** menu, navigate to the VisualDSP++ environment via the **Programs** menu.
   If you are running VisualDSP++ for the first time, the **New Session** dialog box appears on the screen (skip the rest of the procedure and go to step 3).
   If you have run VisualDSP++ previously, the last opened session appears on the screen.
   To switch to another session, via the **Session List** dialog box, hold down the **Ctrl** key while starting VisualDSP++ (go to step 5).
3. In **Debug target**, select **Blackfin Emulators/EZ-KIT Lites**.
   In **Platform**, select the appropriate EZ-KIT Lite via a debug agent (**ADSP-BF537 EZ-KIT Lite via Debug Agent**).
   In **Session name**, type a new name or accept the default.
4. Click **OK** to return to the **Session List**.
5. Highlight the session and click **Activate**.

Evaluation License Restrictions

The ADSP-BF537 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF537 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 20 KB of internal memory for code space with no restrictions for data space.

The EZ-KIT Lite hardware must be connected and powered up to use VisualDSP++ with a valid evaluation or permanent license.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

Memory Map

The ADSP-BF537 processor has internal SRAM that can be used for instruction or data storage. The configuration of internal SRAM is detailed in the *ADSP-BF537 Blackfin Processor Hardware Reference*.

The ADSP-BF537 EZ-KIT Lite board includes two types of external memory, SDRAM and flash.

The size of the SDRAM is 64 Mbytes (32M x 16-bit). The processor's memory select pin, `~SMS0`, is configured for the SDRAM.

The size of the flash memory is 4 Mbytes (2M x 16-bits). The processor's asynchronous memory select pins `~AMS3-0` are configured for the flash.

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map

Start Address		End Address	Content
External Memory	0x0000 0000	0x03FF FFFF	SDRAM Bank 0 (SDRAM). See "SDRAM Interface" on page 1-8.
	0x2000 0000	0x200F FFFF	ASYNC Memory Bank 0. See "Flash Memory" on page 1-9.
	0x2010 0000	0x201F FFFF	ASYNC Memory Bank 1. See "Flash Memory" on page 1-9.
	0x2020 0000	0x202F FFFF	ASYNC Memory Bank 2. See "Flash Memory" on page 1-9.
	0x2030 0000	0x203F FFFF	ASYNK Memory Bank 3. See "Flash Memory" on page 1-9.
	0x203F 0000		MAC Address
	All other locations		Not used
Internal Memory	0xFF80 0000	0xFF80 3FFF	Data Bank A SRAM 16 KB
	0xFF80 4000	0xFF80 7FFF	Data Bank A SRAM/CACHE 16 KB
	0xFF90 0000	0xFF90 7FFF	Data Bank B SRAM 16 KB
	0xFF90 4000	0xFF90 7FFF	Data Bank B SRAM/CACHE 16 KB
	0xFFA0 0000	0xFFA0 7FFF	Instruction Bank A SRAM 32 KB
	0xFFA1 0000	0xFFA1 3FFF	Instruction Bank B SRAM 16 KB
	0xFFA0 8000	0xFFA0 BFFF	Instruction SRAM/CACHE 16 KB
	0xFFB0 0000	0xFFB0 0FFF	Scratch Pad SRAM 4 KB
	0xFFC0 0000	0xFFDF FFFF	System MMRs 2 MB
	0xFFE0 0000	0xFFFF FFFF	Core MMRs 2 MB
	All other locations		Reserved

SDRAM Interface

The three SDRAM control registers must be initialized in order to use the MT48LC32M8A2 32M x 16 bits (64 MB) SDRAM memory. When you are in a VisualDSP++ session and connected to the EZ-KIT Lite board, the SDRAM registers are configured automatically through the debugger each time the processor is reset. The values in Table 1-2 are used whenever Bank 0 is accessed through the debugger (for example, when viewing memory windows or loading a program). The numbers were derived for maximum flexibility and work for a system clock frequency between 54 MHz and 133 MHz.

Table 1-2. EZ-KIT Lite Session SDRAM Default Settings[1]

Register	Value	Function
EBIU_SDGCTL	0x0091998D	Calculated with SCLK = 133 MHz 16-bit data path External buffering timing disabled t_{WR} = 2 SCLK cycles t_{RCD} = 3 SCLK cycles t_{RP} = 3 SCLK cycles t_{RAS} = 6 SCLK cycles pre-fetch disabled CAS latency = 3 SCLK cycles SCLK1 disabled
EBIU_SDBCTL	0x00000025	Bank 0 enabled Bank 0 size = 64 MB Bank 0 column address width = 10 bits
EBIU_SDRRC	0x000003A0	Calculated with SCLK = 54 MHz RDIV = 416 clock cycles

1 54 MHz <= SCLK <= 133 MHz.

The EBIU_SDGCTL register can only be re-written within the user code by first placing the chip in self-refresh (see the *ADSP-BF537 Blackfin Processor Hardware Reference*). Clearing the appropriate checkbox on the **Target**

Options dialog box, which is accessible through the **Settings** pull-down menu, disables automatic and allows manual configuration. For more information, see "Target Options" on page 1-16.

Automatic configuration of SDRAM is not optimized for any SCLK frequency. Table 1-3 shows the optimized configuration for the SDRAM registers using a 120 MHz and 133 MHz SCLK. Only the EBIU_SDRRC register needs to be modified in the user code to achieve maximum performance.

Table 1-3. SDRAM Optimum Settings

Register	SCLK = 133 MHz (CCLK = 400 MHz)	SCLK = 120 MHz (CCLK = 600 MHz)
EBIU_SDGCTL	0x0091 998D	0x0091 998D
EBIU_SDBCTL	0x0000 0025	0x0000 0025
EBIU_SDRRC	0x0000 0408	0x0000 03A0

An example program is included in the EZ-KIT installation directory to demonstrate how to set up the SDRAM interface.

Flash Memory

The flash interface of the ADSP-BF537 EZ-KIT Lite contains a 4 MB (2M x 16-bits) ST Micro M29W320DB device. The size of the flash memory is controlled by the flash address range switch, SW6 (see "Flash Enable Switch (SW6)" on page 2-11). The default for the SW6 switch is all positions ON, which allows the user to have access to the full 4 MB of the flash memory. If any of the ~AMS signals need to be connected to the board by plugging into the expansion interface, the signal can be disconnected from the flash by turning the appropriate position of the SW6 switch to OFF. Each ~AMS signal accounts for 1 MB of flash memory. The amount of available flash memory decreases as ~AMS signals are being turned OFF.

The last sector in the flash memory (0x1F8000–0x1FFFFF) is reserved for the Media Access Control (MAC) address. Each board has a unique MAC address. The sector is protected and is not erased even when the entire flash erase command is issued. The memory sector can be changed only by changing the JP10 jumper from pins 1–2 to pins 2–3. Refer to the flash memory data sheet for information on protected sectors.

Example code is provided in the EZ-KIT Lite installation directory to demonstrate how to program the flash memory.

Table 1-4 shows a sample value for the asynchronous memory configuration register.

Table 1-4. Asynchronous Memory Control Register Setting Example

Register	Value	Function
EBIU_AMBCTL0	0x7BB07BB0	Timing control for Banks 1 and 0

CAN Interface

The Controller Area Network (CAN) interface contains a Philips TJA1041 high-speed CAN transceiver. The PF14 programmable flag connects to the enable control input (EN). The PF15 programmable flag connects to the standby control input (~STB). The PF13 programmable flag connects to the error and power-on indication output (ERR). The PJ4 connects to the receive data output (RXD), and PJ5 connected to the transmit data input (TXD).

The CAN interface can be disconnected from the processor by turning positions 1 though 4 of the SW2 switch to OFF. When in the OFF position, these signals can be used elsewhere on the board. See “CAN Enable Switch (SW2)” on page 2-9 for more information.

The CAN interface contains two 4-position modular connectors.

Example programs are included in the EZ-KIT installation directory to demonstrate the CAN circuit operation.

Ethernet Interface

The ADSP-BF537 processor is able to directly connect to a network with the help of an embedded Fast Ethernet Medium Access Controller (MAC). The MAC supports both 10-BaseT (10 Mbits/sec) and 100-BaseT (100 Mbits/sec) operations. The 10/100 Ethernet MAC peripheral of the ADSP-BF537 processor is fully compliant with the IEEE 802.3-2002 standard and provides programmable features designed to minimize supervision, bus utilization, or message processing by the rest of the processor system.

The Ethernet interface contains a SMSC LAN83C185 device. The LAN83C185 is a low-power highly-integrated analog interface IC for high-performance embedded Ethernet applications.

The Ethernet connector is a RJ45 connector with built-in magnetics and LEDs.

802.3af Power-over-Ethernet (PoE) is supported when the EZ-KIT Lite connects to a Blackfin USB-LAN EZ-Extender.

Example programs are included in the EZ-KIT installation directory to demonstrate the Ethernet circuit operation.

ELVIS Interface

The ADSP-BF537 EZ-KIT Lite board contains the National Instruments Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) interface. The interface features the DC voltage and current measurement modules, oscilloscope and bode analyzer modules, function generator, arbitrary waveform generator, and digital IO.

The ELVIS interface is a LabVIEW-based design and prototype environment for university science and engineering laboratories. The ELVIS interface consists of LabVIEW-based virtual instruments, a multifunction data acquisition (DAQ) device, and a custom-designed bench-top workstation and prototype board. This combination provides a ready-to-use suite of instruments found in most educational laboratories. Because the interface is based on LabVIEW and provides complete data acquisition and prototyping capabilities, the system is ideal for academic coursework that range from lower-division classes to advanced project-based curriculums.

For more information on ELVIS and example demonstration programs, visit National Instruments Web site at www.ni.com.

Audio Interface

The audio circuit provides one channel of stereo input and one channel of stereo output via 3.5 mm stereo jacks. The SPORT0 interface of the processor is linked with the stereo audio data input and output pins of the audio circuit. The audio circuit consists of an AD1871 analog-to-digital converter (ADC) and an AD1854 digital-to-analog converter (DAC).

The processor is responsible for generating the frame sync and bit clocks because the audio interface of the EZ-KIT Lite operates in slave mode. The audio interface samples data at a 48 kHz sample rate. The serial data interface operates in Two Wire Interface mode and connects to SPORT0 of the processor.

The audio interface can be disconnected from SPORT0 by turning positions 1 and 5 of the SW7 switch OFF. When in the OFF position, the SPORT0 signals can be used on the SPORT0 connector (P6) or the expansion interface (see "Audio Enable Switch (SW7)" on page 2-12 for more information).

Example programs are included in the EZ-KIT installation directory to demonstrate the audio circuit operation.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and six LEDs for general-purpose IO.

The six LEDs, labeled `LED1` through `LED6`, are accessed via the `PF11-PF6` processor pins. For information on how to program the pins, refer to the *ADSP-BF537 Blackfin Processor Hardware Reference*.

The four general-purpose push button are labeled `SW10` through `SW13`. A status of each individual button can be read through programmable flag (PF) inputs, `PF2` through `PF5`. A PF reads "`1`" when a corresponding switch is being pressed-on. When the switch is released, the PF reads "`0`". A connection between the push button and PF input is established through the `SW5` DIP switch. See "Push Button Enable Switch (SW5)" on page 2-11 for details.

An example program is included in the EZ-KIT installation directory to demonstrate the functionality of the LEDs and push buttons.

Example Programs

Example programs are provided with the ADSP-BF537 EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in the `…\Blackfin\EZ-KITs\ADSP-BF537\Examples` subdirectory of the VisualDSP++ installation directory. Please refer to the readme file provided with each example for more information.

Background Telemetry Channel

The ADSP-BF537 USB debug agent supports the Background Telemetry Channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

The BTC allows the user to view a variable as it is updated or changed, all while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check out our latest line of processor emulators on the web at `www.analog.com`. For more information about the Background Telemetry Channel, see the *VisualDSP++ User's Guide* or online Help.

VisualDSP++ Interface

This section provides information on the following parts of the VisualDSP++ graphical user interface:

- "Trace Window" on page 1-14
- "Target Options" on page 1-16
- "Restricted Software Breakpoints" on page 1-18

Trace Window

Choosing the **Trace** command from the **View–>Debug Windows** menu opens the **Trace** window (Figure 1-2).

The trace buffer stores a history of the last 16 changes in program flow taken by the program sequencer. View the history to recreate the program sequencer's most recent path.

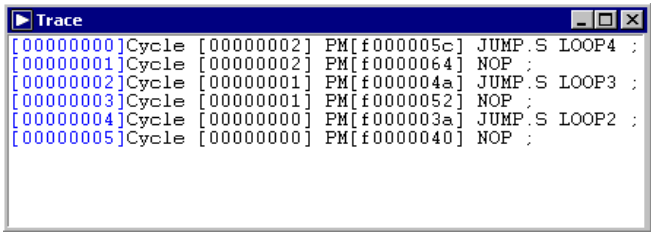

Figure 1-2. Trace Window

The trace buffer does not track changes in flow caused by zero-overhead loops or while in the reset service routine.

To use the trace buffer, ensure your program leaves the reset service routine.

Enabling Trace Buffer

To view trace history in the **Trace** window, first, enable the trace buffer (choose **Enable Trace** from the **Tools–>Trace** menu). On each halt, the **Trace** window is updated with the changes that occurred since the last halt. Reading the trace buffer destroys the trace buffer's contents and discards the information previously stored before the last run.

Reading Trace Buffer Data

The first column between the square brackets (in blue) indicates the line number in the **Trace** window.

The second column between square brackets, which comes in vertical pairs, shows the trace number. For each discontinuity, the first (top position) is the source trace, and the second (bottom position) is the destination trace. The third column in between square brackets shows the addresses of the instructions. Each address is followed by the assembly instruction.

The trace grows upward. In Figure 1-2, trace 0 occurred before trace 1, which occurred before trace 2, and so on.

Target Options

Choosing **Target Options** from the **Settings** menu opens the **Target Options** dialog box (Figure 1-3). Use target options to control certain aspects of the processor on the ADSP-BF537 EZ-KIT Lite evaluation system.

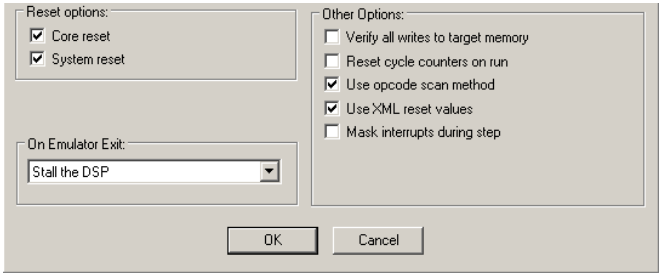

Figure 1-3. Target Options Dialog Box

Reset Options

Reset options control how the processor behaves when a reset occurs. The reset options are described in Table 1-5.

Table 1-5. Reset Options

Option	Description
Core reset	Resets the core when the debugger executes a reset.
System reset	Resets the peripherals when the debugger executes a reset.

On Emulator Exit

This target option controls processor behavior when VisualDSP++ relinquishes processor control (for example, when exiting VisualDSP++). The option is described in Table 1-6.

Table 1-6. On Emulator Exit Target Options

Option	Description
On Emulator Exit	Determines the state the processor is left in when the emulator relinquishes control of the processor: **Reset DSP and Run** causes the processor to reset and begin execution from its reset vector location. **Run from current PC** causes the processor to begin running from its current location. **Stall the DSP** resets the processor and then writes a `JUMP 0` to the first location in internal memory so the processor is stuck in a tight loop after exiting.

Other Options

Table 1-7 describes other available target options.

Table 1-7. Miscellaneous Target Options

Option	Description
Verify all writes to target memory	Validates all memory writes to the processor. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files, since VisualDSP++ does not perform the extra reads that are required to verify each write.
Reset cycles counter on run	Resets the cycle count registers to zero before a **Run** command is issued. Select this option to count the number of cycles executed between breakpoints in a program.

Table 1-7. Miscellaneous Target Options (Cont'd)

Option	Description
Use opcode scan method	Enables the debugger to use a highly-optimized JTAG scan method; provides extremely fast communication between the EZ-KIT Lite and the processor. In certain circumstances, causes JTAG scan failures. Typically, JTAG scan failures occur when this option is combined with debugging situations that hold off or stall the core (such as debugging, loading, or viewing external memory). Clearing this option uses a less optimized JTAG scan method.
Use XML reset values	Uses a section in the processor-specific .XML file located in the installation's system folder. The file defines registers that are reset to certain values; the values are read at startup and subsequently used to set the registers when a reset is performed through VisualDSP++.
Mask interrupts during step	Disables interrupts while single stepping through code.

Restricted Software Breakpoints

The EZ-KIT Lite development system restricts breakpoint placement when certain conditions are met. That is, under some conditions, breakpoints cannot be placed effectively. Such conditions depend on bus architecture, pipeline depth, and ordering of the EZ-KIT Lite and its target processor.

2 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF537 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the ADSP-BF537 EZ-KIT Lite board and explains how the board components interface with the processor.
- "Jumper and Switch Settings" on page 2-9
  Shows the location and describes the function of the configuration jumpers and switches.
- "LEDs and Push Buttons" on page 2-19
  Shows the location and describes the function of the LEDs and push buttons.
- "Connectors" on page 2-22
  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

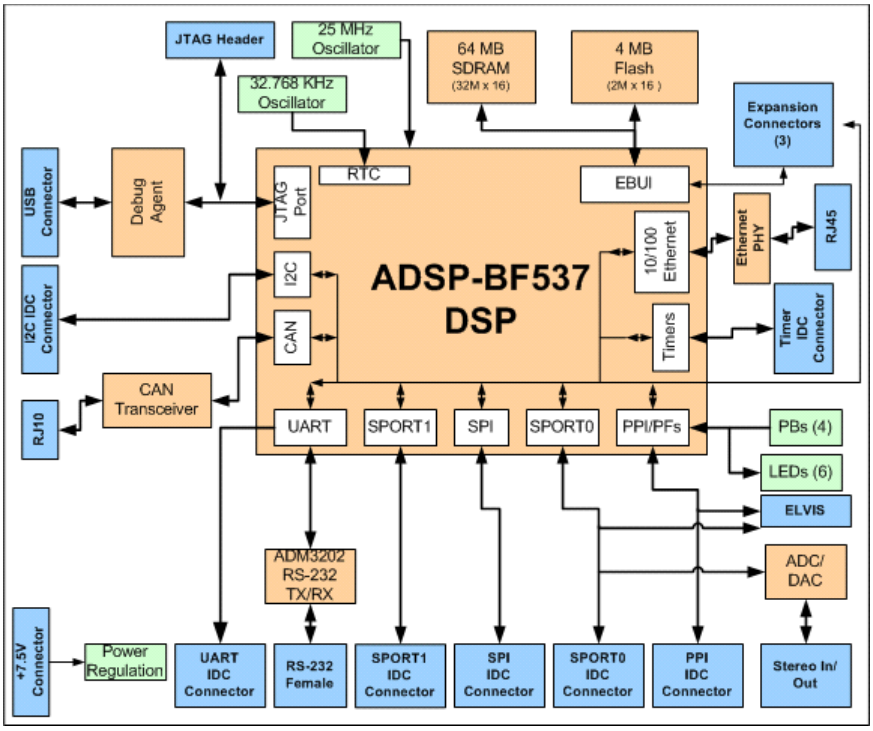

Figure 2-1. System Architecture

The EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF537 Blackfin processor. The processor has IO voltage of 3.3V. The core voltage of the processor is supplied by the internal voltage regulator.

The core voltage and the core clock rate can be set on the fly by the processor. The input clock is 25 MHz. A 32.768 kHz crystal supplies the Real Time Clock (RTC) inputs of the processor. The default boot mode for the processor is flash boot. See "Boot Mode Select Switch (SW16)" on page 2-13 for information about changing the default boot mode.

External Bus Interface Unit

The External Bus Interface Unit (EBIU) connects external memory to the ADSP-BF537 processor. The unit includes a 16-bit wide data bus, an address bus, and a control bus. On the EZ-KIT Lite, the EBIU connects to the SDRAM, flash, and expansion interfaces.

64 Mbytes (32M x 16 bits) of SDRAM connect to the synchronous memory select 0 pin (~SMS0). Refer to "SDRAM Interface" on page 1-8 for information about configuring the SDRAM. Note that SDRAM clock is the processor's Clock Out (CLK OUT), which must not exceed 133 MHz.

The flash memory device connects to the asynchronous memory select signals, ~AMS3 through ~AMS0. The device provides a total of 4 Mbytes of flash memory. The processor can use this memory for both booting and storing information during normal operation. Refer to "Flash Memory" on page 1-9 for details.

All of the address, data, and control signals are available externally via the expansion interface (J1-3). The pinout of these connectors can be found in Appendix B, "Schematics" on page B-1.

SPORT0 Audio Interface

The SPORT0 interface connects to the audio circuit, the SPORT0 connector (P6), and the expansion interface. The audio circuit uses the primary data transmit and receive pins to input and output data from the audio input and outputs.

The pinout of the SPORT connector and the expansion interface connectors can be found in Appendix B, "Schematics" on page B-1.

SPI Interface

The processor's Serial Peripheral Interconnect (SPI) interface is connected to the SPI connector (P9) and the expansion interface.

Programmable Flags (PFs)

The processor has 48 general-purpose input/output (GPIO) signals spread across three ports (PF, PG and PH). The pins have multiple functions, depending on the setup of the processor. Table 2-1 shows how the programmable flag pins are used on the EZ-KIT Lite.

Table 2-1. Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF0	GPIO/DMAR0	UART0 Transmit
PF1	GPIO/DMAR1	UART0 Receive
PF2	UART1_TX/TMR7	Push button (SW13). See "Programmable Flag Push Buttons (SW13–10)" on page 2-20.
PF3	UART1_RX/TMR6/TACI6	Push button (SW12). See "Programmable Flag Push Buttons (SW13–10)" on page 2-20.
PF4	TMR5/SPI_SSEL6	Push button (SW11). See "Programmable Flag Push Buttons (SW13–10)" on page 2-20.
PF5	TMR4/SPI_SSEL5	Push button (SW10). See "Programmable Flag Push Buttons (SW13–10)" on page 2-20.

Table 2-1. Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF6	TMR3/SPI_SSEL4	LED (LED1). See "LEDs and Push Buttons" on page 1-13 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PF7	TMR2/PPI_FS3	LED (LED2). See "LEDs and Push Buttons" on page 1-13 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PF8	TMR1/PPI_FS2	LED (LED3). See "LEDs and Push Buttons" on page 1-13 and "Push Button Enable Switch (SW5)" on page 2-11 for information on how to disable the push button.
PF9	TMR0/PPI_FS1	LED (LED4). See "LEDs and Push Buttons" on page 1-13 and "ELVIS Processor Core Current Measurement Jumpers (JP1 and JP7)" on page 2-16 for information on how to disable the push button.
PF10	SPI_SSEL1	LED (LED5). See "LEDs and Push Buttons" on page 1-13 and "ELVIS Processor Core Current Measurement Jumpers (JP1 and JP7)" on page 2-16 for information on how to disable the push button.
PF11	SPI_MOSI	LED (LED6). See "LEDs and Push Buttons" on page 1-13 and "ELVIS Processor Core Current Measurement Jumpers (JP1 and JP7)" on page 2-16 for information on how to disable the push button.
PF12	SPI_MISO	Audio Reset
PF13	SPI_SCK	CAN ERR
PF14	SPI_SS/TACLK0	CAN EN
PF15	PPI4_CLK/TMRCLK	CAN STB
PG0	PPI_D0	ELVIS_TRIGGER
PG1	PPI_D1	ELVIS_PF1

Table 2-1. Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG2	PPI_D2	ELVIS_PF2
PG3	PPI_D3	ELVIS_PF5
PG4	PPI_D4	ELVIS_PF6
PG5	PPI_D5	ELVIS_PF7
PG6	PPI_D6	UART0_CTS
PG7	PPI_D7	UART0_RTS
PG8	PPI_D8/DR1SEC	Not used
PG9	PPI_D9/DT1SEC	Not used
PG10	PPI_D10/RSCLK1	Not used
PG11	PPI_D11/RFS1	Not used
PG12	PPI_D12/DR1PRI	Not used
PG13	PPI_D13/TSCLK1	Not used
PG14	PPI_D14/TFS1	No used
PG15	PPI_D15/DT1PRI	USB_IRQ used for USB bus power
PH0	ETXD0	ETXD used for Ethernet interface
PH1	ETXD1	ETXD1 used for Ethernet interface
PH2	ETXD2	ETXD2 used for Ethernet interface
PH3	ETXD3	ETXD3 used for Ethernet interface
PH4	ETXEN	ETXEN used for Ethernet interface
PH5	MII_TXCLK/RMII_REF_CLK	MII_TXCLK used for Ethernet interface
PH6	MII_PHYINT/RMII_MDINT	Not used
PH7	COL	COL used for Ethernet interface
PH8	ERXD0	ERXD0 used for Ethernet interface
PH9	ERXD1	ERXD1 used for Ethernet interface

Table 2-1. Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PH10	ERXD2	ERXD2 used for Ethernet interface
PH11	ERXD3	ERXD3 used for Ethernet interface
PH12	ERXDV/TACLK5	ERXDV used for Ethernet interface
PH13	ERXCLK/TACLK6	ERXCLK used for Ethernet interface
PH14	ERXER/TACLK7	ERXER used for Ethernet interface
PH15	MII_CRS/RMII_CRS_DV	MII_CRS used for Ethernet interface

UART Port

The processor's Universal Asynchronous Receiver/Transmitter (UART) port connects to the ADM3202 RS232 line driver as well as to the expansion interface. The RS232 line driver connects to the DB9 female connector, providing an interface to a PC or other serial device.

Expansion Interface

The expansion interface consists of three 90-pin connectors. Table 2-2 shows the interfaces each connector provides. For the exact pinout of these connectors, refer to Appendix B, "Schematics" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical or Customer Support.

Analog Devices offers many EZ-Extender products that plug on to the expansion interface. For more information on these products, visit the Analog Devices Web site at www.analog.com.

Table 2-2. Expansion Interface Connectors

Connector	Interfaces
J1	5V, G ND, Address, Data, PPI
J2	3.3V, GND, SPI, NMI, TMR2–0, SPORT0, SPORT1, PF15–0, EBUI control signals
J3	5V, 3.3V, GND, UART, Flash IO, Reset, Video control signals

Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the regulator used. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a 6-pin interface. The JTAG emulation port of the processor connects also to the USB debugging interface. When an emulator connects to the board at P4, the USB debugging interface is disabled. See "JTAG Connector (P4)" on page 2-25 for more information about the connector.

To learn more about available emulators, contact Analog Devices (see "Processor Product Information").

Jumper and Switch Settings

This section describes the operation of the jumpers and switches. The jumpers and switch locations are shown in Figure 2-2.

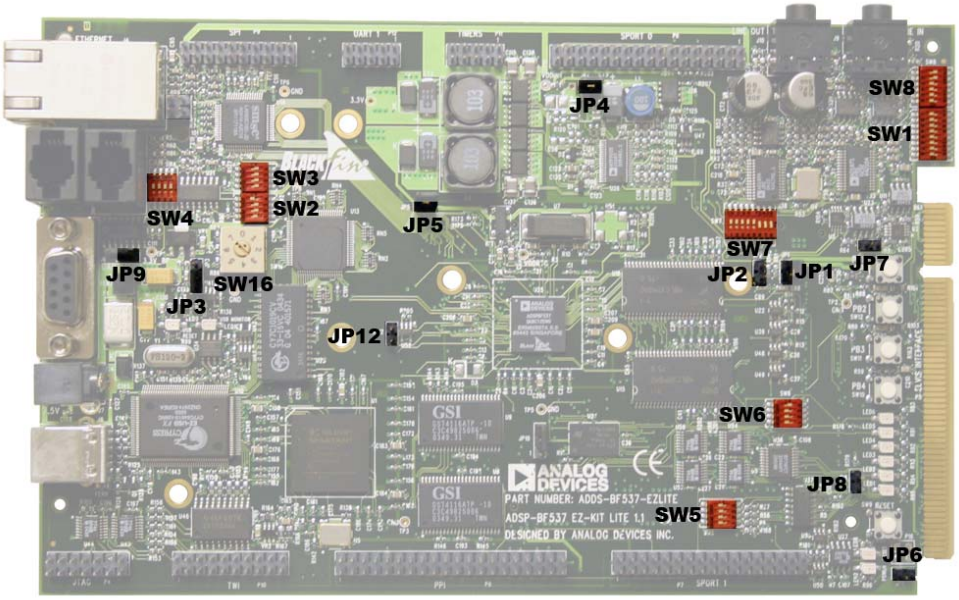

Figure 2-2. Jumper and Switch Locations

CAN Enable Switch (SW2)

The Controller Area Network (CAN) enable switch (SW2) disconnects the CAN signals from the GPIO pins of the processor. When the SW2 switch is in the OFF position, the associated GPIO signal (see Table 2-3) can be used on the expansion interface.

Table 2-3. CAN Enable Switch (SW2)

CAN Signal	SW2 Switch Position (Default)	Processor Signal
ENABLE	1 (ON)	PF14
STANDBY	2 (ON)	PF15
ERROR	3 (ON)	PF13
RECEIVE DATA	4 (ON)	PJ4

Ethernet Mode Select Switch (SW3)

The Ethernet mode select switch (SW3) controls the configuration of the 10/100 digital block in the LAN83C185 PHY device (see Table 2-4).

Table 2-4. Ethernet Mode Select Switch (SW3)

SW3 Switch Position			Ethernet Mode
3	2	1	
ON	ON	ON	10Base-T Half Duplex. Auto-negotiation disabled.
ON	ON	OFF	10Base-T Full Duplex. Auto-negotiation disabled.
ON	OFF	ON	100Base-T Half Duplex. Auto-negotiation disabled.
ON	OFF	OFF	100Base-T Full Duplex. Auto-negotiation disabled.
OFF	ON	ON	100Base-T Half Duplex. Auto-negotiation enabled.
OFF	ON	OFF	Repeater mode. Auto-negotiation enabled.
OFF	OFF	ON	Power Down mode
OFF	**OFF**	**OFF**	**All capable. Auto-negotiation enabled. (Default)**

UART Enable Switch (SW4)

The UART enable switch (SW4) disconnects UART signals from the GPIO pins of the processor. When the switch is in the OFF position, the associated GPIO signal (see Table 2-5) can be used on the expansion interface.

Table 2-5. UART Enable Switch (SW4)

EZ-KIT Lite Signal	SW4 Switch Position (Default)	Processor Signal
TX	1 (ON)	PF0
CTS	2 (ON)	PG6
RX	3 (ON)	PPF1
RTS	4 (OFF)	PG7

Push Button Enable Switch (SW5)

The push button enable switch (SW5) disconnects the associated with the push button circuit drivers from the GPIO pins of the processor. When the SW5 switch is in the OFF position, the associated GPIO signal (see Table 2-6) can be used on the expansion interface.

Table 2-6. Push Button Enable Switch (SW5)

Push Button	SW5 Switch Position (Default)	Processor Signal
PB1 (SW13)	1 (ON)	PF2
PB2 (SW12)	2 (ON)	PF3
PB3 (SW11)	3 (ON)	PF4
PB4 (SW10)	4 (ON)	PF5

Flash Enable Switch (SW6)

The flash enable switch (SW6) disconnects ~AMS signals from flash memory, allowing other devices to utilize the signals via the expansion interface. For each switch listed in Table 2-7 that is turned OFF, the size of available flash memory is reduced by 1 MB.

Table 2-7. Flash Enable Switch (SW6)

Processor Signal	SW6 Switch Position (Default)
~AMS0	1 (ON)
~AMS1	2 (ON)
~AMS2	3 (ON)
~AMS3	4 (ON)

Audio Enable Switch (SW7)

The audio enable switch (SW7) disconnects the audio signals from the processor (positions 1–5) and determines how the clock for the audio circuit is generated and connected (position 6–8). Position 8 determines if the ADC is in master or slave mode. When in master mode (position 8 is ON), the ADC generates the clock. When in slave mode (position 8 is OFF), the processor generates the clock. Positions 6 and 7 connect the transmit and receive clocks together (see Table 2-8).

Table 2-8. Audio Enable Switch (SW7)

EZ-KIT Lite Signal	SW7 Switch Position (Default)	Processor Signal
DROPRI	1 (ON)	PJ8
RSCLK0	2 (ON)	PJ6
RFS0	3 (ON)	PJ7
TSCLK0	4 (ON)	PG9
TFS0	5 (ON)	PJ10
Clock Loopback	6 (ON)	
FS Loopback	7 (ON)	
ADC Master/Slave	8 (ON)	

Boot Mode Select Switch (SW16)

The rotary switch (SW16) determines the boot mode of the processor. Table 2-9 shows the available boot mode settings. By default, the ADSP-BF537 processor boots from on-board flash memory.

Table 2-9. Boot Mode Select Switch (SW16)

SW16 Position	Processor Boot Mode
0	Execute from 16-bit external memory
1	**Boot from 16-bit flash memory. (Default)**
2	Reserved
3	Boot from SPI memory
4	Boot from SPI host
5	Boot from Serial TWI Memory
6	Boot from TWI host
7	Boot from UART host

3V Power Selection Jumper (JP3)

The 3V power selection jumper (JP3) selects the power source for the 3-volt parts. In a standard mode of operation, the parts are powered by the on-board switching regulator circuit (ADP3025) via an external power supply. When a Blackfin USB-LAN EZ-Extender connects to the EZ-KIT Lite, power can be derived from the USB bus power or Power-over-Ethernet (802.3af). In this case, the board can operate without an external power supply. The jumper settings are shown in Table 2-10.

Core Voltage Selection Jumper (JP4)

The core voltage selection jumper (JP4) is not used in the current design. The jumper settings shown in Table 2-11 must not be changed.

Table 2-10. 3V Power Selection Jumper (JP3)

JP3 Position	Mode
1 & 2	**3V parts powered from on-board switching regulator. (Default)**
2 & 3	3V parts powered from an external power supply: USB-bus power or Power-over-Ethernet

Table 2-11. Core Voltage Selection Jumper (JP4)

JP4 Position	Mode
1 and 2	Not used
2 and 3	**Default setting**

Expansion Interface Voltage Selection Jumper (JP5)

The expansion interface voltage selection jumper (JP5) selects the power source for the 5-volt signal on the expansion interface. In a standard mode of operation, the signal is powered by the on-board switching regulator circuit (ADP3025) via an external power supply. When a Blackfin USB-LAN EZ-Extender connects to the board, power can be derived from the USB bus power or Power-over-Ethernet (802.3af). In this case, the board can operate without an external power supply. The jumper setting is shown in Table 2-12.

Table 2-12. Expansion Interface Voltage Selection Jumper (JP5)

JP5 Setting	Mode
ON	**5V signal powered from on-board switching regulator. (Default)**
OFF	5V signal powered from external power supply: USB-bus power or Power-over-Ethernet

UART Loop Jumper (JP9)

The UART loop jumper (JP9) is for looping the transmit and receive signals. The default is in the OFF position.

ELVIS Oscilloscope Configuration Switch (SW1)

The oscilloscope configuration switch (SW1) determines which audio circuit signals connect to channels A and B of the oscilloscope. The switch is used only when the board connects to the Educational Laboratory Virtual Instrumentation Suite (ELVIS) interface (see "ELVIS Interface" on page 1-11). Each channel must have only one signal selected at a time (see Table 2-13).

Table 2-13. Oscilloscope Configuration Switch (SW1)

Channel	SW1 Switch Position (Default)	Audio Circuit Signal
A	1 (OFF)	AMP_LEFT_IN
A	2 (OFF)	AMP_RIGHT_IN
A	3 (OFF)	LEFT_OUT
A	4 (OFF)	RIGHT_OUT
B	5 (OFF	AMP_LEFT_IN
B	6 (OFF)	AMP_RIGHT_IN
B	7 (OFF)	LEFT_OUT
B	8 (OFF)	RIGHT_OUT

ELVIS Function Generator Configuration Switch (SW8)

The function generator configuration switch (SW8) controls which signals connect to the left and right input signals of the audio interface. The SW8 switch is used only when the board connects to the ELVIS interface (see "ELVIS Interface" on page 1-11). Each channel must have only one signal selected at a time, as described in Table 2-14.

Table 2-14. Function Generator Configuration Switch (SW8)

Channel	SW8 Switch Position (Default)	Audio Signal
AMP_LEFT_IN	1 (ON)	LEFT_IN
AMP_RIGHT_IN	2 (ON)	RIGHT_IN
AMP_LEFT_IN	3 (OFF)	DAC0
AMP_RIGHT_IN	4 (OFF)	DAC1
AMP_LEFT_IN	5 (OFF)	FUNCT_OUT
AMP_RIGHT_IN	6 (OFF)	FUNCT_OUT

ELVIS Processor Core Current Measurement Jumpers (JP1 and JP7)

The JP1 and JP7 jumpers select the method for the core current measurement of the processor. The feature is supported only when the circuit connects to an ELVIS station or to a NI DAQ card (see "ELVIS Interface" on page 1-11). When JP1 and JP7 connect to neither system, the circuit must be bypassed. The jumper settings are shown in Table 2-15.

Table 2-15. Processor Core Measurement Jumpers (JP1 and JP7)

JP1 Setting	JP7 Setting	Mode
OFF	OFF	ELVIS current measurement
OFF	ON	DAQ current measurement
ON	**OFF**	**Bypass shunt circuit. (Default)**
ON	ON	Not used

ELVIS IO Current Measurement Jumper (JP2)

The processor IO current measurement jumpers (JP2) controls the method by which IO current is measured. The feature is supported only when the circuit connects to an NI DAQ card (see "ELVIS Interface" on page 1-11). When is not connected to a DAQ system, the circuit must be bypassed. The jumper settings are shown in Table 2-16.

Table 2-16. IO current Measurement Jumper (JP2)

JP2 Setting	Mode
OFF	DAQ current measurement
ON	**BYPASS shunt circuit. (Default)**

ELVIS Voltage Selection Jumper (JP6)

The ELVIS voltage selection jumper (JP6) is used to select the power source for the EZ-KIT Lite. In a standard mode of operation, the board receives its power from an external power supply. When JP6 is installed, the board is powered from an ELVIS interface and no external power supply is required. The jumper setting is shown in Table 2-17.

The external power supply must be disconnected from the board when JP6 is installed. In this case, the power supply may cause damage to the EZ-KIT Lite board and ELVIS unit.

Table 2-17. ELVIS Voltage Selection Jumper (JP6)

JP6 Setting	Mode
OFF	**Powered from an external power supply. (Default)**
ON	Powered from ELVIS

ELVIS Select Jumper (JP8)

The ELVIS select jumper (JP8) configures the EZ-KIT Lite's connection to an ELVIS station (see "ELVIS Interface" on page 1-11). When JP8 is installed, the connections to the push buttons and LED are re-directed to the ELVIS station, instead of the processor. The jumper setting is shown in Table 2-18.

Table 2-18. ELVIS Select Jumper (JP8)

JP8 Setting	Mode
OFF	**Not connected to ELVIS. (Default)**
ON	Connected to ELVIS

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 2-3 shows the locations of the LEDs and push buttons.

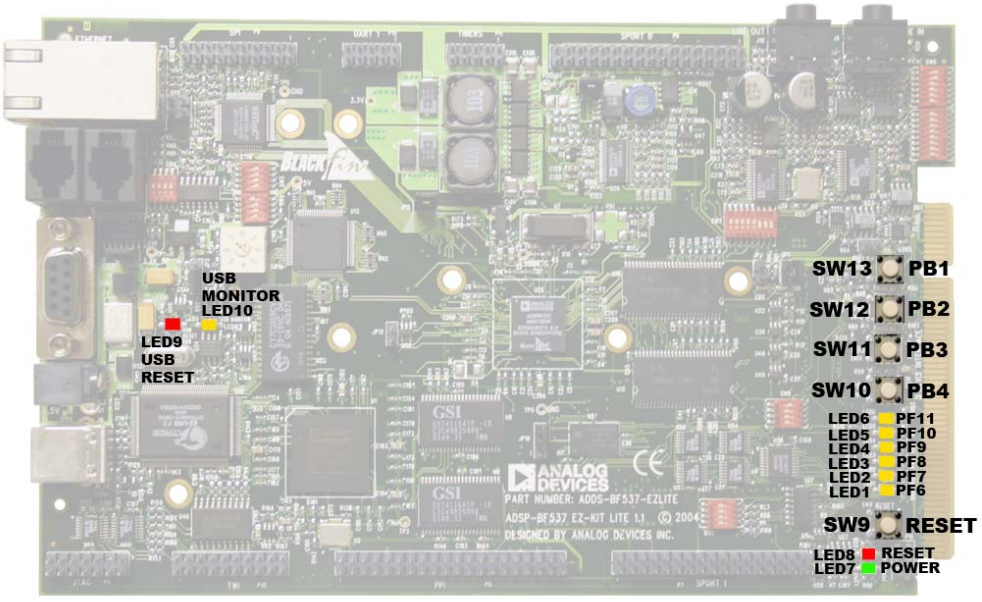

Figure 2-3. LED and Push Button Locations

Reset Push Button (SW9)

The RESET push button resets all of the ICs on the board. One exception is the USB interface chip. The chip is not being reset when the push button is pressed after the USB cable has been plugged in and communication has been correctly initialized with the PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.

Programmable Flag Push Buttons (SW13–10)

Four push buttons, SW13-10, are provided for general-purpose user input. The buttons connect to PF5-2 programmable flag pins of the processor. The push buttons are active HIGH and, when pressed, send a High (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-13 for more information on how to use the PFs when programming the processor. The push button enable switch (SW5) is capable of disconnecting the push buttons from the PF (refer to "Push Button Enable Switch (SW5)" on page 2-11 for more information). The programmable flag signals and their corresponding switches are shown in Table 2-19.

Table 2-19. Programmable Flag Switches

Processor Programmable Flag Pin	Push Button Reference Designator
PF2	SW13
PF3	SW12
PF4	SW11
PF5	SW10

Power LED (LED7)

When LED7 is lit (green), it indicates that power is being properly supplied to the board.

Reset LEDs (LED8 and LED9)

When LED8 is lit, it indicates that the master reset of all the major ICs is active. When LED9 is lit, the USB interface chip is being reset. The USB chips reset only on power-up, or if USB communication has not been initialized.

User LEDs (LED1–6)

Six LEDs connect to six general-purpose IO pins of the processor (see Table 2-20)). The LEDs are active HIGH and are lit by writing a "1" to the correct PF signal. Refer to "LEDs and Push Buttons" on page 1-13 for more information about how to use the flash when programming the LEDs.

Table 2-20. User LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED1	PF6
LED2	PF7
LED3	PF8
LED4	PF9
LED5	PF10
LED6	PF11

USB Monitor LED (LED10)

The USB Monitor LED (LED10) indicates that USB communication has been initialized successfully, and you can connect to the processor using a VisualDSP++ EZ-KIT Lite session. This should take approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see the *VisualDSP++ Installation Quick Reference card*).

When VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Connectors

This section describes the connector functionality and provides information about mating connectors. The locations of the connectors are shown in Figure 2-4 on page 2-22.

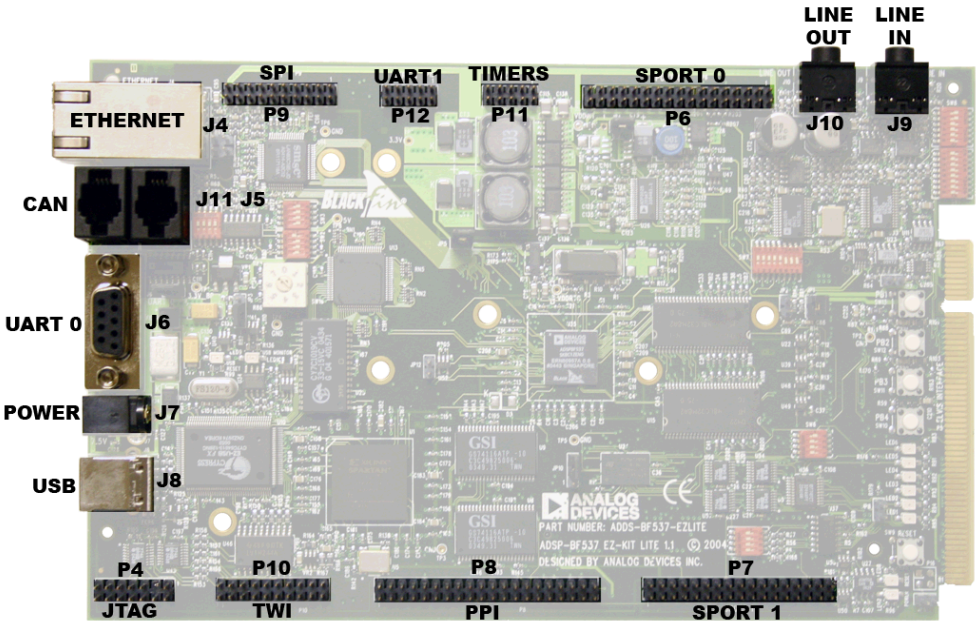

Figure 2-4. Connector Locations

Audio Connectors (J9 and J10)

Part Description	Manufacturer	Part Number
3.5 mm stereo jack	A/D Electronics	ST323-5
Mating Cable (shipped with EZ-KIT Lite)		
3.5 mm stereo interconnect cable	Random	0A3-01106
3.5 mm headphones	Koss	UR5

CAN Connectors (J5 and J11)

Part Description	Manufacturer	Part Number
Modular Jack	AMP	558872-1
Mating Cable		
4 conductor modular jack cable	L-COM	TSP3044

Ethernet Connector (J4)

Part Description	Manufacturer	Part Number
Ethernet Jack	Pulse	JK0-0025
Mating Cable (shipped with EZ-KIT Lite)		
Cat 5E patch cable	Random	PC10/100T-007
Cat 5E crossover cable	Random	PC10/100TC-007

RS232 Connector (J6)

Part Description	Manufacturer	Part Number
DB9, Female, Vertical Mount	Digi-Key	191-009-213-571-ND
Mating Cable		
2m Female to female cable	Digi-Key	AE1020-ND

Power Connector (J7)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm Power Jack	SWITCHCRAFT	RAPC712
Mating Power Supply (shipped with EZ-KIT Lite)		
7V Power Supply	CUI Inc.	DMS070214-P6P-SZ

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-21 shows the power supply specifications.

Table 2-21. Power Supply Specification

Terminal	Connection
Center pin	+7 VDC@2.14 amps
Outer Ring	GND

Expansion Interface Connectors (J1–3)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see "Expansion Interface" on page 2-7. For the availability and pricing of the J1, J12, and J3 connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90 Position 0.05" Spacing, SMT	Samtec	SFC-145-T2-F-D-A
Mating Connector		
90 Position 0.05" Spacing (Through Hole)	Samtec	TFM-145-x1 Series
90 Position 0.05" Spacing (Surface Mount)	Samtec	TFM-145-x2 Series
90 Position 0.05" Spacing (Low Cost)	Samtec	TFC-145 Series

JTAG Connector (P4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

SPORT0 Connector (P6)

The pinout for the P6 connector can be found in Appendix B, “Schematics” on page B-1.

Part Description	Manufacturer	Part Number
IDC Header	Digi-Key	S2012-17-ND
Mating Connector		
IDC socket	Digi-Key	S4217-ND

SPORT1 Connector (P7)

The pinout for the P7 connector can be found in Appendix B, “Schematics” on page B-1.

Part Description	Manufacturer	Part Number
IDC Header	Digi-Key	S2012-17-ND
Mating Connector		
IDC socket	Digi-Key	S4217-ND

PPI Connector (P8)

The pinout for the P8 connector can be found in Appendix B, “Schematics” on page B-1.

Part Description	Manufacturer	Part Number
IDC Header	Digi-Key	S2012-20-ND
Mating Connector		
IDC socket	Digi-Key	S4220-ND

SPI Connector (P9)

The pinout for the P9 connector can be found in Appendix B, "Schematics" on page B-1.

Part Description	Manufacturer	Part Number
IDC Header	Digi-Key	S2012-10-ND
Mating Connector		
IDC socket	Digi-Key	S4210-ND

Two-Wire Interface Connector (P10)

The pinout for the P10 connector can be found in Appendix B, "Schematics" on page B-1.

Part Description	Manufacturer	Part Number
IDC Header	Digi-Key	S2012-10-ND
Mating Connector		
IDC socket	Digi-Key	S4210-ND

TIMERS Connector (P11)

The pinout for the P11 connector can be found in Appendix B, "Schematics" on page B-1.

Part Description	Manufacturer	Part Number
IDC Header	Digi-Key	S2012-05-ND
Mating Connector		
IDC socket	Digi-Key	S4205-ND

UART1 Connector (P12)

The pinout for the P12 connector can be found in Appendix B, "Schematics" on page B-1.

Part Description	Manufacturer	Part Number
IDC Header	Digi-Key	S2012-05-ND
Mating Connector		
IDC socket	Digi-Key	S4205-ND

A BILL OF MATERIALS

The bill of materials corresponds to the board schematics on page B-1. Please check the latest schematics on the Analog Devices website, http://www.analog.com/Processors/Processors/DevelopmentTools/technicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals.

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
1	1	3.3V-OCTAL-BUFFER	U46	TI	SN74LVT244BDW
2	1	10MHZ OSCILLATOR	U5	RALTRON	C04310-10.00
3	1	HEX-INVER-SCHMITT-TRIGGER	U37	TI	74LVC14AD
4	1	3.3V-OCTAL-BUFFER	U36	IDT	IDT74FCT3244APY
5	1	USB-TX/RX MICROCONTROL-LER	U10	CYPRESS	CY7C64603-128NC
6	1	NPN TRANSISTOR 200MA	Q1	FAIRCHILD	MMBT4401
7	1	ADJ 200MA REGULATOR	VR2	ANALOG DEVICES	ADP3331ART
8	1	25 MHZ CRYSTAL	U7	EPSON	MA-505 25.000M-C2
9	1	128K X 8 SRAM	U25	CYPRESS	CY7C1019BV33-12VC
10	1	12 MHZ CRYSTAL	Y1	DIG01	300-6027-ND
11	5	SINGLE-2-INPUT-NAND	U39-43	TI	SN74AHC1G00DBVR
12	1	12.288 MHZ OSCILLATOR	U4	DIG01	SG-8002CA-PCC-ND
13	2	256Kx16 SRAM	U8-9	GSI TECHNOL-OGY	GS74116ATP-10
14	1	P-MOSFET	U28	FAIRCHILD SEMI	NDS8434A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
15	1	32.768 CRYSTAL	U6	EPSON	MC-156 32.768KA-A2
16	1	XILINX-SPARTANIIE	U1	XILINX	XC2S150E-7FT256C
17	1	SINGLE-2 INPUT OR GATE	U52	TI	SN74LVC1G32DBVR
18	6	SINGLE-2-INPUT-AND-GATE	U22,U47-50,U58	TI	SN74LVC1G08DBVR
19	2	8M X 8 SDRAM	U15-16	MICRON	MT48LC32M8A2TG-75
20	1	CAN-TRANSCEIVER	U21	PHILIPS	TJA1041T
21	1	Ethernet-PHY	U14	SMSC	LAN83C185-JD
22	4	POWER-MOSFET	U17-20	VISHAY	SI4820DY-T1
23	1	24LC32	U34	ATMEL	24LC32
24	1	DSM2150F5V	U13	ST MICRO	DSM2150F5V
25	1	M29W320DB	U24	ST MICRO	M29W320DB70ZA6
26	1	VOLTAGE-SUPERVISOR	U27	ANALOG DEVICES	ADM708SAR
27	1	3.3V-1.0AMP REGULATOR	VR1	ANALOG DEVICES	ADP3338AKC-3.3
28	3	DUAL AUDIO OP AMP	U29-31	NATIONAL SEMI	LMV722M

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
29	1	STERO-DAC	U38	ANALOG DEVICES	AD1854JRS
30	1	STERO-ADC	U33	ANALOG DEVICES	AD1871YRS
31	1	RS232-TXRX	U32	ANALOG DEVICES	ADM3202ARN
32	2	Instrumentation-amp	U2-3	ANALOG DEVICES	AD623ARM-REEL
33	2	OP-amp	U11,U23	ANALOG DEVICES	AD820AR
34	1	DSP	U35	ANALOG DEVICES	ADSP-BF537SKBC1ENG
35	1	REGULAOR	U26	ANALOG DEVICES	ADP3025JRU-REEL
36	1	POWER JACK	J7	SWITCHCRAFT	SC1152-ND12
37	1	USB CONNECTOR	J8	MILL-MAX	897-30-004-90-0000
38	5	PUSH BUTTON SWITCH	SW9-13	PANASONIC	EVQ-PAD04M
39	3	SMT SOCKET	J1, J2, J3	SAMTEC	SFC-145-T2-F-D-A
40	2	DIP SWITCH	SW1, SW7	C&K	CKN1365-ND

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
41	1	DIP SWITCH	SW8	DIG01	CKN1364-ND
42	5	DIP SWITCH	SW2-6	DIG01	CKN1363-ND
43	1	POE-Builtin-magnetics	J4	PULSE ENG.	JK0-0025
44	1	Rotary-Switch	SW16	GRAYHILL	94HAB08
45	1	DB9 CONNECTOR	J6	NORCOMP INC	191-009-213-571
46	2	MODULAR CONNECTOR	J5, J11	AMP	558872-1
47	7	LED	LED1-6,10	PANASONIC	LN1461C-TR
48	2	10uF 16V 10% C	CT7 AND CT8	SPRAGUE	293D106X9016C2T
49	3	100 100MW 5% 805	R100-101,R103	AVX	CR21-101J-T
50	7	FERRITE BEAD	FER2-6,FER9	MURATA	BLM11A601SPT
51	1	SILICON RECTIFIER	D4	VISHAY	S2A/52
52	1	68uF 6.3V 20% D	CT5	PANASONIC	ECS-TOJD686R
53	1	340K 1/8W 1% 805	R166	DALE	CRCW0805-3403FT
54	1	698K 1/8W 1% 805	R167	DALE	CRCW0805-6983FT
55	2	68uF 25V 20% CAP003	CT1-2	PANASONIC	EEV-FC1E680P

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
56	1	332K 1/10W 1% 805	R164	PHILIPS	9C08052A3323FKRT/R
57	1	10uH 47 +/-20 IND001	L1	DIG01	445-1202-2-ND
58	2	270 1/10W 5% 805	R99,R136	PHYCOMP	9C08052A2700JLHFT
59	5	10K 31MW 5% RNET8	RN1-5	CTS	746X101103J
60	1	190 100MHZ 5A FER002	FER7	MURATA	DLW5BSN191SQ2
61	1	SCHOTTKY DIODE	D5	ZETEX	ZHCS1000
62	2	0.47UF 16V 10% 805	C199-200	AVX	0805YC474KAT2A
63	5	1UF 10V 10% 805	C134,C210, C220-222	AVX	0805ZC105KAT2A
64	19	10UF 6.3V 10% 805	C158,C176,C182-184, C206-209, C212-219	AVX	080560106KAT2A
65	43	0.1UF 10V 10% 402	C55-57,C59-60, C111-114,C139-140, C146-149,C152-157, C168-175,C185-198	AVX	0402ZD104KAT2A
66	83	0.01UF 16V 10% 402	C1-25,C30-46,C96-105, C107-110,C141-145, C159-167,C177-181, C202-205,C211, C225, C226, C227	AVX	0402YC103KAT2A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
67	59	10K 1/16W 5% 402	R2,R5,R7-9,R12-16, R24-25,R72-74,R78-80, R82,R84-90,R97, R126-130,R139-147, R162,R169, R170-172,R174, R176-178,R179, R181-186,R205	DALE	CRCW0402103JRT7
68	1	4.7k 1/16w 5% 402	R4	PANASONIC	ERJ-2GEJ472X
69	3	0 1/16W 5% 402	R3,R163,R207	PANASONIC	ERJ-2GE0R00X
70	20	22 1/16W 5% 402	R187-R202,R122-123, R137-138	PANASONIC	ERJ-2GEJ220X
71	2	33 1/16W 5% 402	R1, R54	PANASONIC	ERJ-2GEJ330X
72	4	18PF 50VDC 5% 805	C26-29	PANASONIC	ECJ-2VC1H180J
73	2	1000PF 50V 5% 402	C127-128	AVX	04025C102JAT2A
74	1	34.8K 1/10W 1% 805	R113	YAGEO	9C08052A3482FKHFT
75	2	1.5K 1/10W 5% 603	R206, R124	DIGIKEY	P1.5KCFCT-ND
76	1	0.022UF 50V 5% 805	C95	AVX	08055C223JAT2A
77	12	0.1UF 16V 10% 603	C64,C72-74,C87-89, C123-125,C130,C133	AVX	0603YC104KAT2A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
78	5	0.01UF 16V 10% 0603	C50-51,C62-63,C93	KEMET	C0603C103K4RAC
79	4	10UF 25V +80/-20% 1210	C115,C136-138	PANASONIC	ECJ-4YF1E106Z
80	1	4.7UF 25V 205 0805	C122	PANASONIC	ECJ-2FB1E475M
81	2	68PF 50V 5% 0603	C116-117	PANASONIC	ECJ-1VC1H680J
82	4	330PF 50V 5% 0603	C79,C84,C118,C121	AVX	06035A331JAT2A
83	1	150PF 50V 5% 0603	C120	AVX	06035A151JAT2A
84	1	4.7UF 6.3V 20% 0603	C135	PANASONIC	ECJ-1VB0J475M
85	1	470PF 50V 5% 0603	C119	PANASONIC	ECJ-1VC1H471J
86	1	22000PF 16V 10% 0603	C132	PANASONIC	ECJ-1VB1C223K
87	1	68000PF 25V +80/-20% 0603	C131	PANASONIC	ECJ-1VF1E683Z
88	2	33000PF 25V 10% 0603	C126,C129	AVX	06033C333KAT2A
89	2	220UF 6.3V 20% D2E	CT3-4	SANYO	10TPE220ML
90	2	1A 10BQ040 SMB	D8-9	IR	10BQ040
91	2	10UH 17 20% IND005	L2-3	COILCRAFT	MSS1278-103MXB

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
92	6	10K 1/10W 5% 0603	R37,R53,R105, R156-158	VISHAY	CRCW0603103JRT1
93	2	4.7K 1/10W 5% 0603	R155,R161	VISHAY	CRCW0603472JRT1
94	2	10M 1/10W 5% 0603	R10-11	VISHAY	CRCW0603106JRT1
95	2	100K 1/10W 5% 0603	R20,R26	VISHAY	CRCW0603104JRT1
96	10	330 1/10W 5% 0603	R75-76,R83,R91-96,R98	VISHAY	CRCW0603331JRT1
97	1	1M 1/10W 5% 0603	R135	VISHAY	CRCW0603105JRT1
98	12	0 1/10W 5% 0603	R27,R115,R117-118, R149-154,R165,R168	PHYCOMP	9C06031A0R00JLHFT
99	4	49.9 1/16W 1% 0603	R67-68,R70-71	VISHAY	CRCW060349R9FRT1
100	8	10 1/10W 5% 0603	R6,R55-57,R59,R62, R69,R111	DALE	CRCW0603100JRT1
101	1	130K 1/16W 1% 0603	R107	VISHAY	CRCW06031303FRT1
102	1	4.7 1/10W 5% 0603	R119	PHYCOMP	9C06031A4R70JLHFT
103	4	10K 1/16W 1% 0603	R64,R102,R106,R110	PHYCOMP	9C06031A1002FKHFT
104	1	75K 1/16W 1% 0603	R108	DALE	CRCW06037502FRT1
105	1	6.2K 1/10W 1% 0603	R109	DIGI-KEY	311-6.20KHTR-ND

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
106	3	200K 1/16W 1% 0603	R112,R114,R116	VISHAY	CRCW06032003FRT1
107	1	25.5K 1/16W 1% 0603	R104	YAGEO	9C06031A2552FKHFT
108	1	1K 1/10W 5% 0603	R125	YAGEO	9C06031A1001JLHFT
109	2	6.8NF 16V 10% 0603	C91-92	DIG01	311-1084-2-ND
110	1	4.7NF 16V 10% 0603	C90	DIG01	311-1083-2-ND
111	4	237 1/10W 1% 0603	R23,R29,R31,R33	DIGI-KEY	311-237HTR-ND
112	2	750K 1/10W 1% 0603	R30,R32	DIGI-KEY	311-750KHTR-ND
113	3	11K 1/10W 1% 0603	R39-40,R60	DIGI-KEY	311-11KHTR-ND
114	4	5.49K 1/10W 1% 0603	R42-43,R46-47	DIGI-KEY	311-5.49KHTR-ND
115	3	3.32K 1/10W 1% 0603	R44,R48,R132	DIGI-KEY	311-3.32KHTR-ND
116	2	1.65K 1/10W 1% 0603	R45,R49	DIGI-KEY	311-1.65KHTR-ND
117	2	49.9K 1/10W 1% 0603	R38,R41	DIGI-KEY	311-49.9KHTR-ND
118	2	604 1/10W 1% 0603	R50-51	DIGI-KEY	311-604HTR-ND
119	2	90.9K 1/10W 1% 0603	R58,R63	DIGI-KEY	311-90KHTR-ND
120	2	0.1 1/10W 1% 0603	R61,R148	YAGEO	ERJ-3RSFR10V

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
121	2	10K 1/10W 1% 0603	R159-160	DIGI-KEY	311-10.0KHTR-ND
122	8	5.76K 1/10W 1% 0603	R17-19,R21-22,R28, R34-35	DIGI-KEY	311-5.76KHTR-ND
123	4	120PF 50V 5% 0603	C47-49,C71	PANASONIC	ECJ-1VC1H121J
124	12	100PF 50V 5% 0603	C52-54,C61,C65,C68, C75,C77,C81,C85,C94, C106	PANASONIC	ECJ-1VC1H101J
125	4	0.001UF 50V 5% 0603	C66-67,C69-70	PANASONIC	ECJ-1VC1H102J
126	2	33PF 50V 5% 0603	C150-151	PANASONIC	ECJ-1VC1H300J
127	2	2.21K 1/10W 1% 0603	R133-134	DIGI-KEY	311-2.21KHTR-ND
128	1	12.4K 1/10W 1% 0603	R77	DIGI-KEY	311-12.4KHTR-ND
129	2	62.0 1/10W 1% 0603	R65-66	DIGI-KEY	311-62.0HTR-ND
130	2	220PF 50V 5% 0603	C82,C86	PANASONIC	ECJ-1VC1H221J
131	2	680pF 50V 5% 0603	C80,C83	PANASONIC	ECJ-1VC1H681J
132	2	2200pF 50V 5% 0603	C76,C78	PANASONIC	ECJ-1VB1H222K
133	2	2.74K 1/10W 1% 0603	R36,R52	DIGI-KEY	311-2.74KHTR-ND
134	2	DIODE	D1 & D2	DIODES INC	MMBD4148W

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
135	2	LED	LED8-9	PANASONIC	LN1261C
136	1	LED	LED7	PANASONIC	LN1361C
137	6	QUICKSWITCH-257	U44-45,U54-57	ANALOG DEVICES	ADG774ABRQ
138	8	IDC 2X1	JP1-2, JP5-9, JP12	BERG	54101-T08-02
139	2	IDC 3X1	JP3,JP10	BERG	54101-T08-03
140	2	IDC 5X2	P11-12	BERG	54102-T08-05
141	1	IDC 7X2	P4	BERG	54102-T08-07
142	2	IDC 10X2	P9-10	BERG	54102-T08-10
143	2	IDC 17X2	P6-7	BERG	54102-T08-17
144	1	IDC 20X2	P8	BERG	54102-T08-20
145	1	FUSE	F1	RAYCHEM CORP.	SMD250-2
146	2	AUDIO CONNECTOR	J9, J10	AD ELECTRON-ICS	ST-323-5
147	2	1.2K 1/16W 1% 402	R173, R175	DIGIKEY	P1.2KJTR-ND

ADSP-BF537 EZ-KIT LITE SCHEMATIC

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Approvals	Date
Drawn	
Checked	
Engineering	

Title	ADSP-BF537 EZ-KIT LITE TITLE		
Size C	Board No. A0188-2004		Rev 1.1
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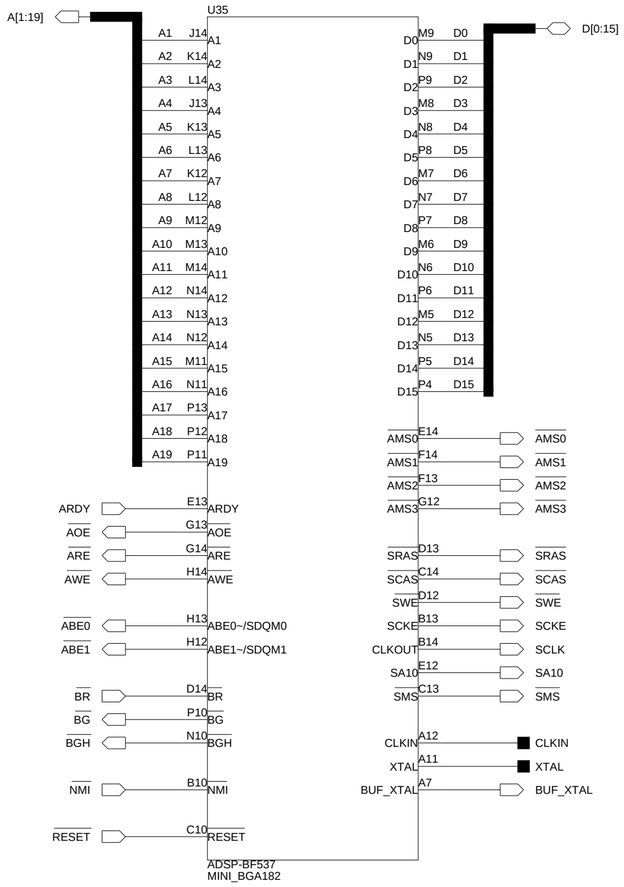
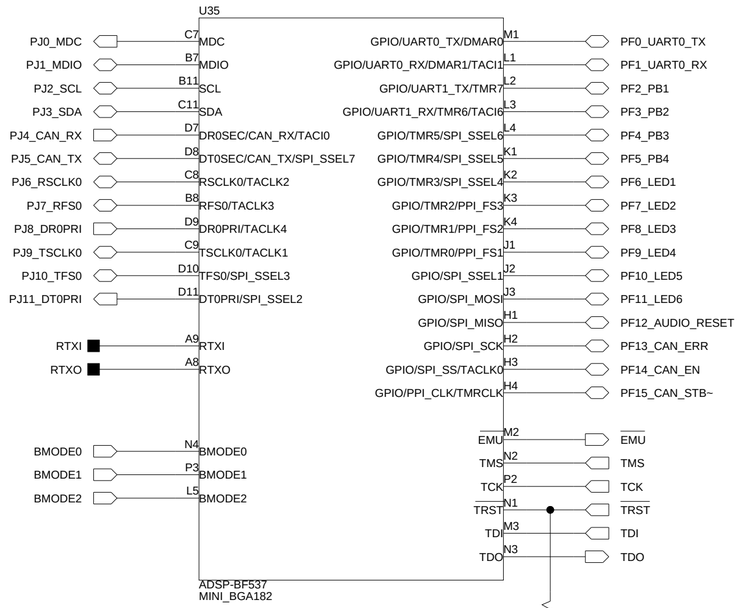
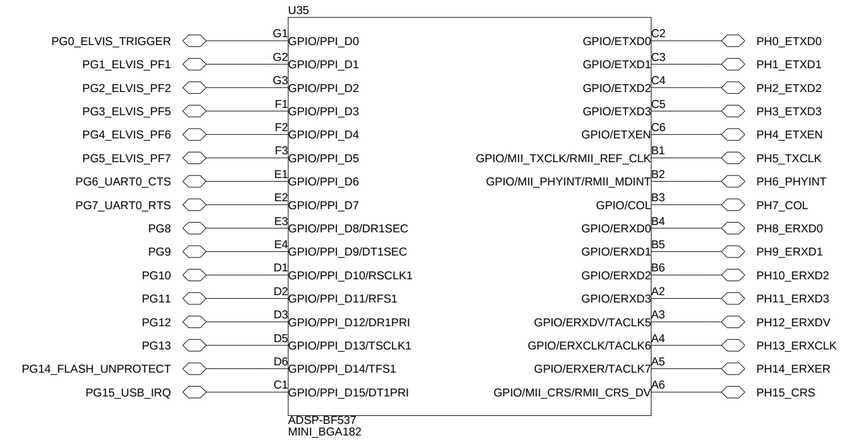
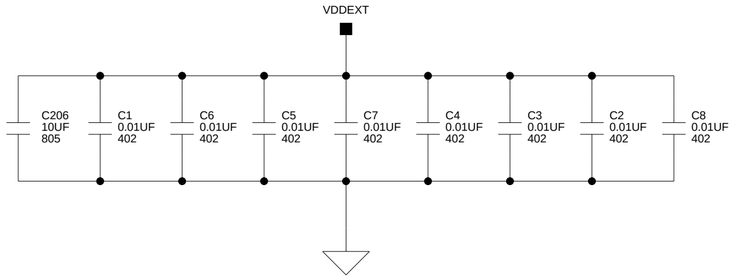


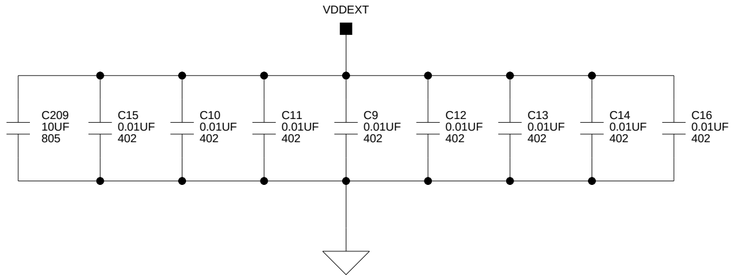


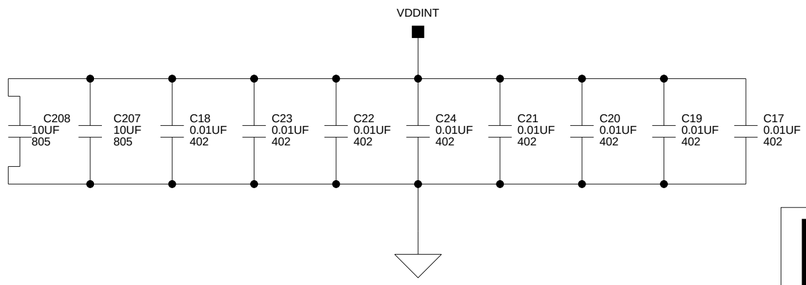


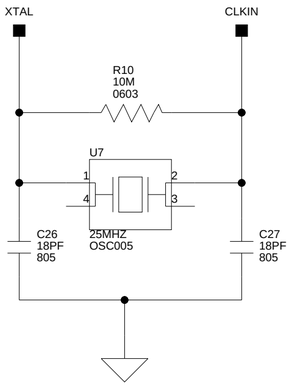
R4
4.7K
402

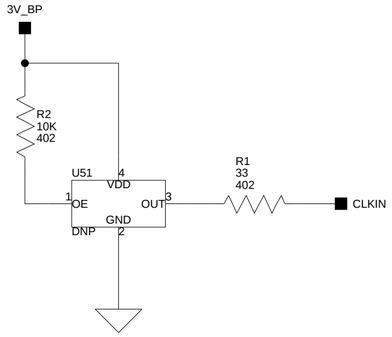
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com

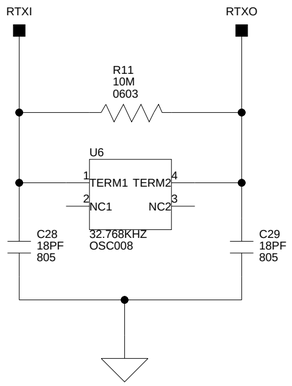












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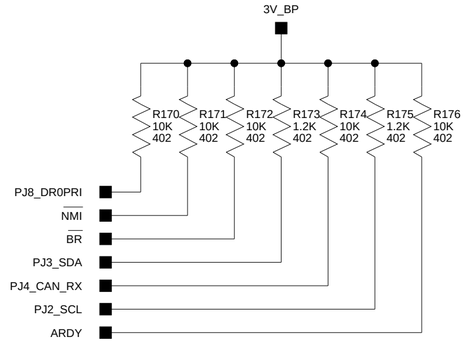

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Title	ADSP-BF537 EZ-KIT LITE SDRAM AND FLASH		
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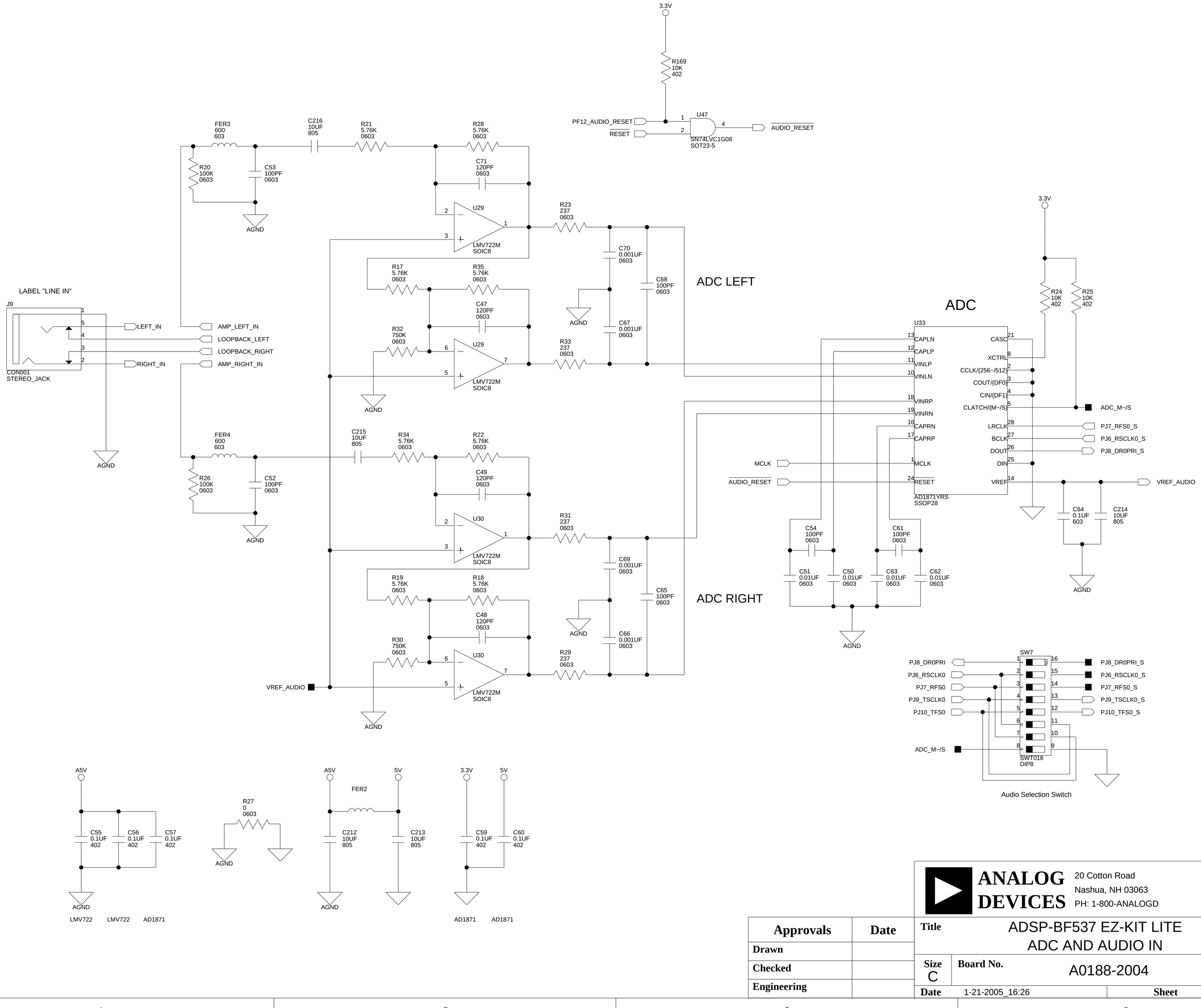

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Title	ADSP-BF537 EZ-KIT LITE DAC AND AUDIO OUT	
Size: C	Board No.: A0188-2004	Rev: 1.1
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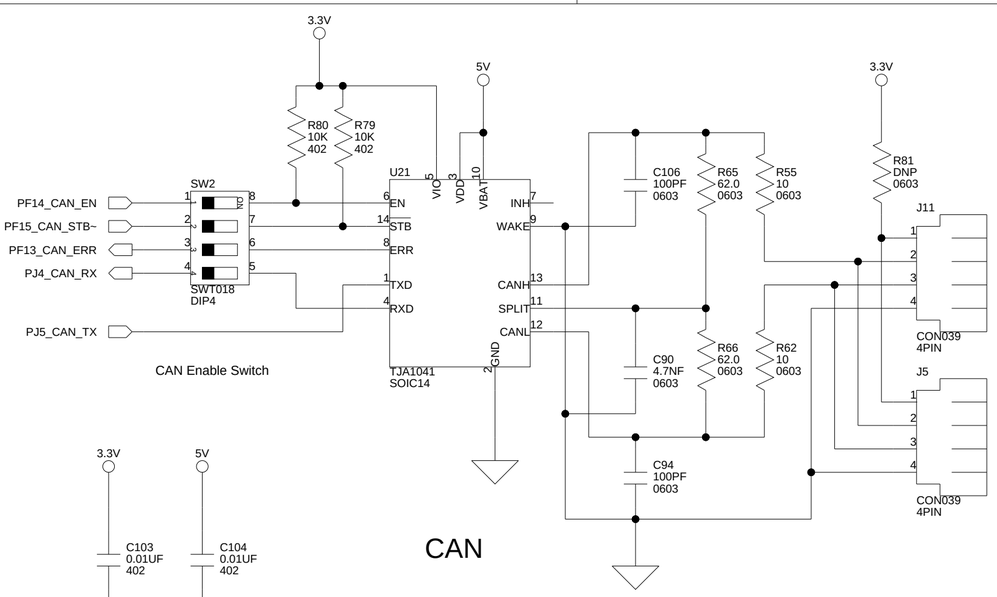

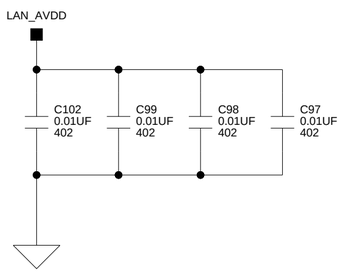

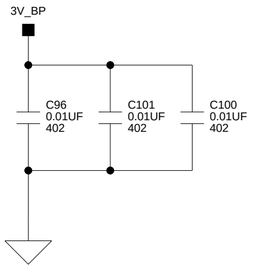

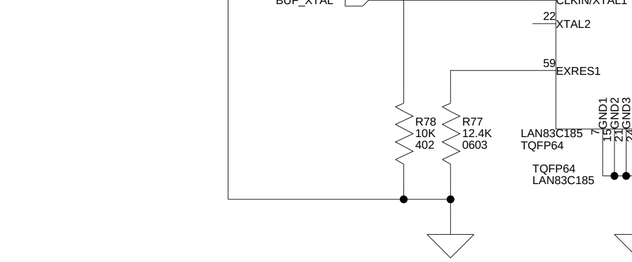

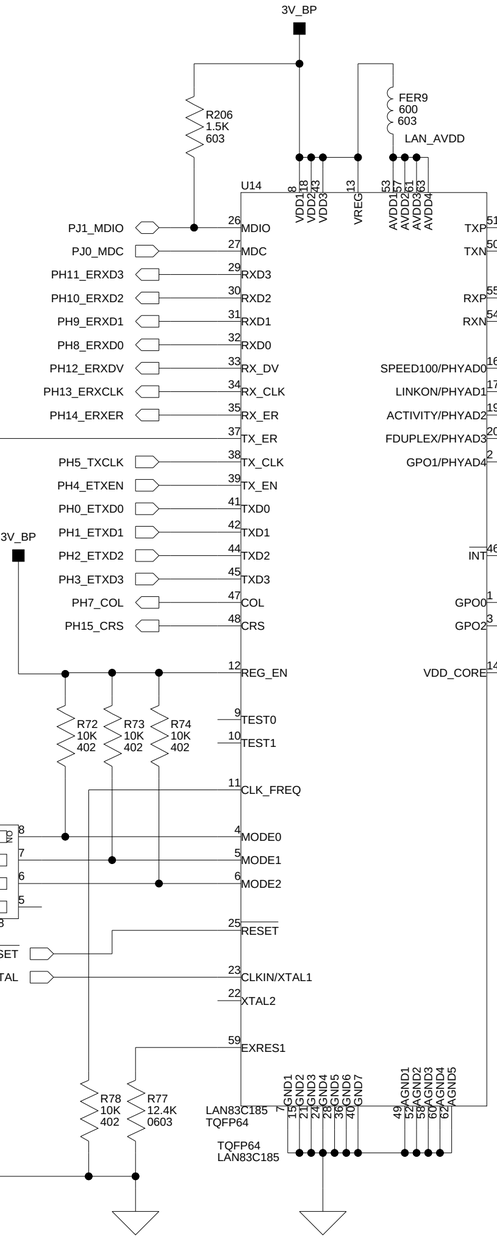

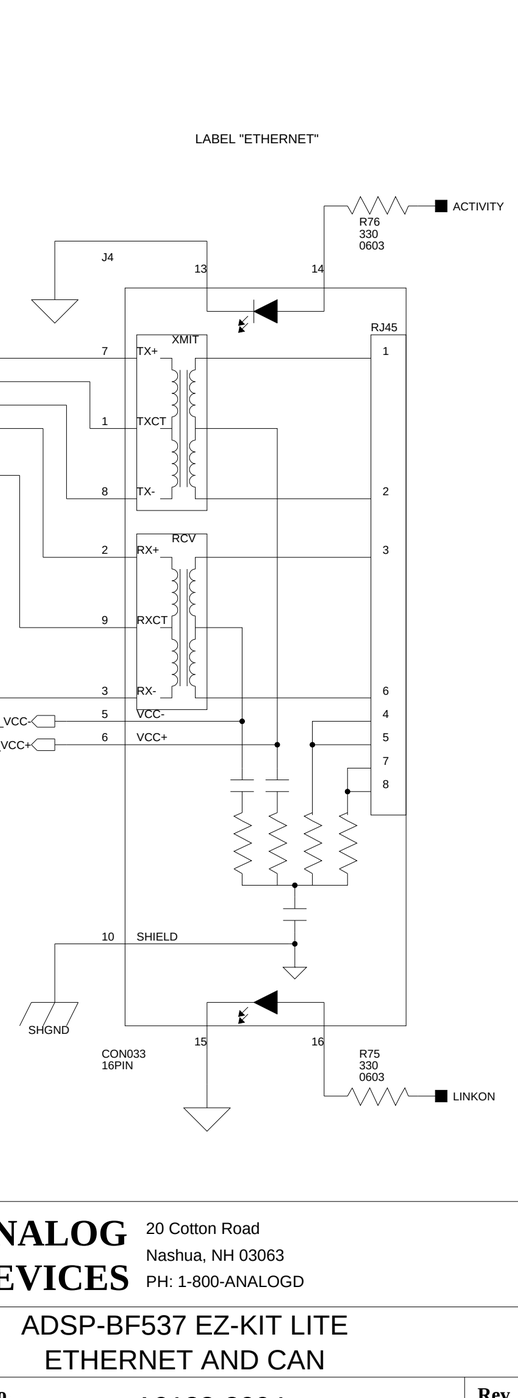

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Title	ADSP-BF537 EZ-KIT LITE ETHERNET AND CAN		
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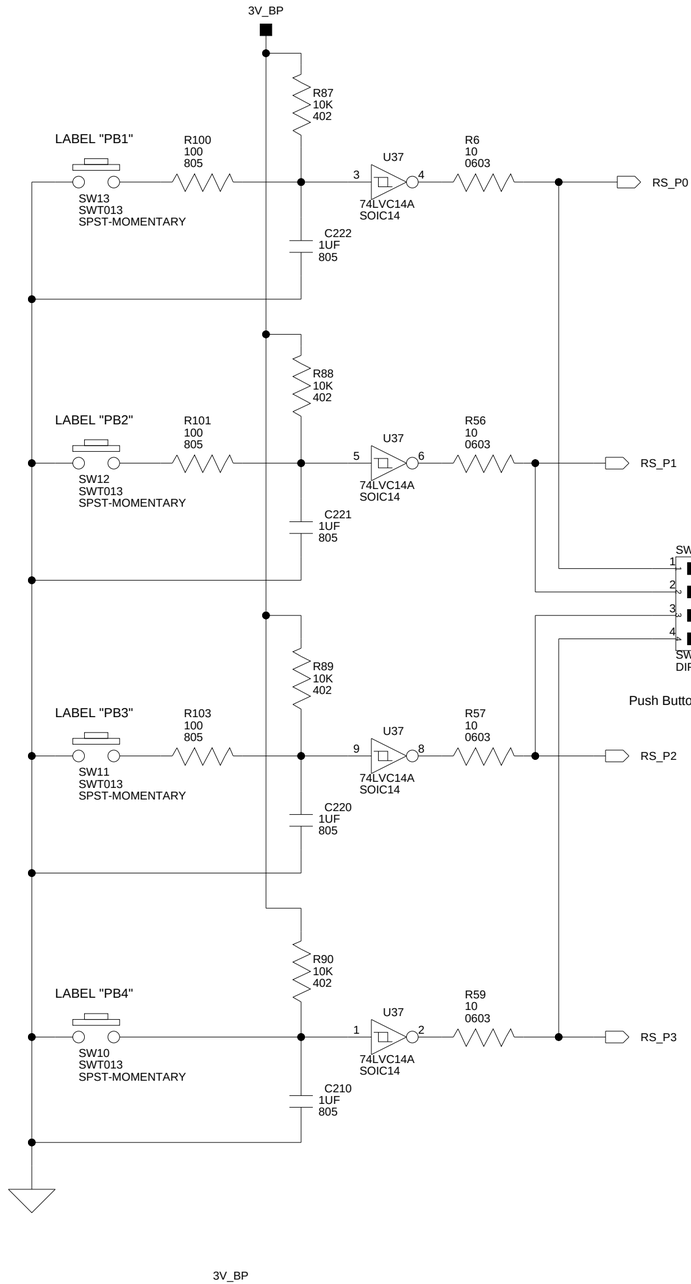
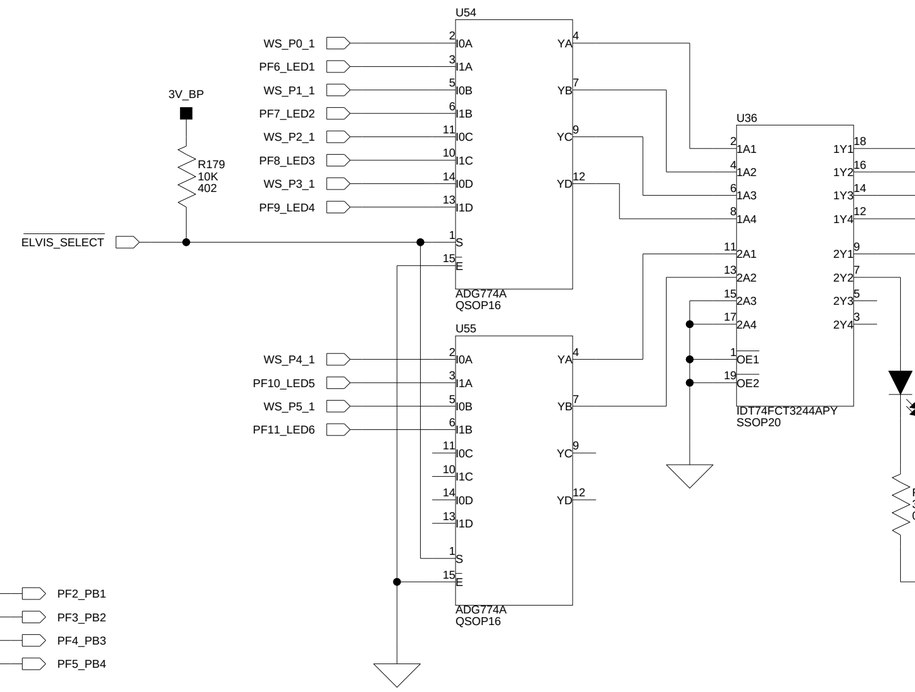
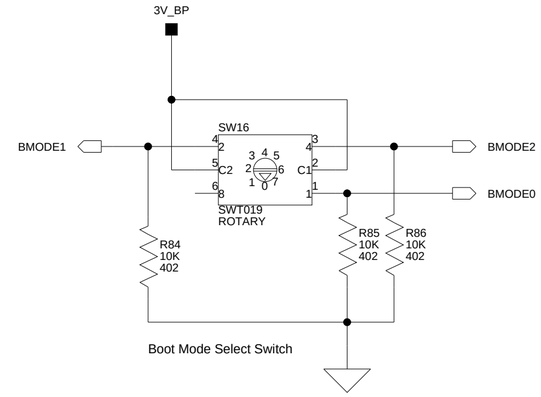


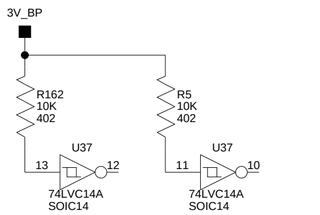
Push Button Enable Switch

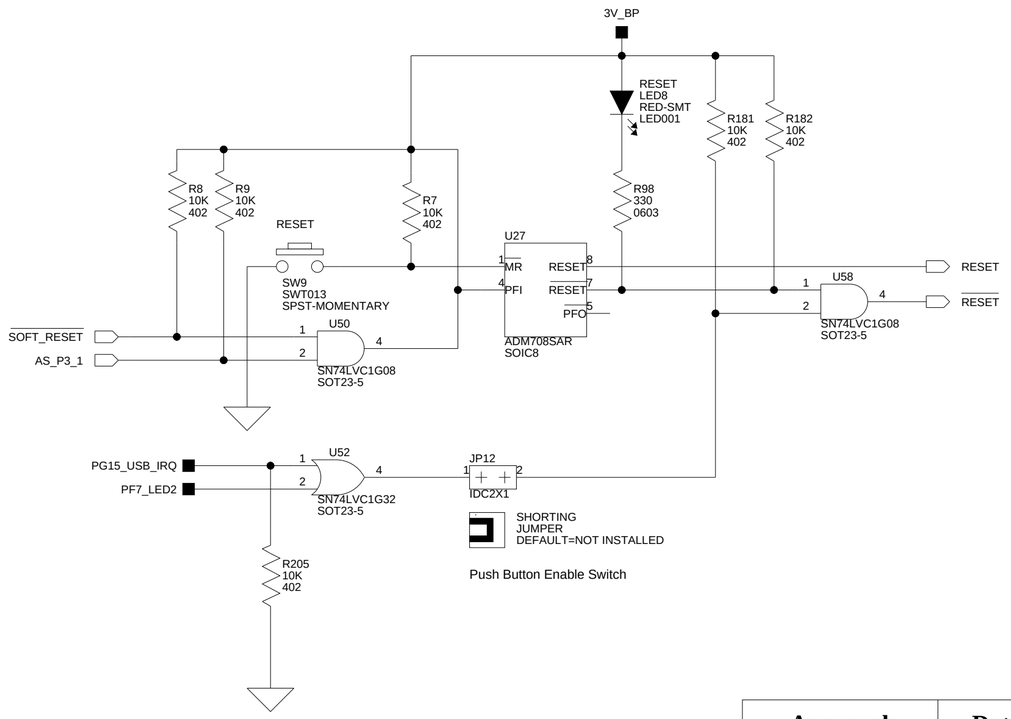




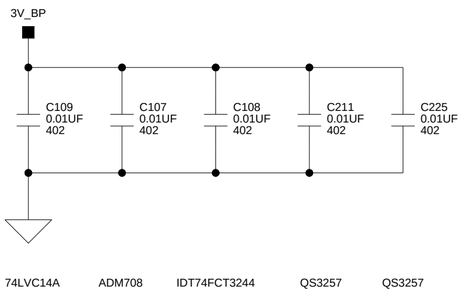
Boot Mode Select Switch

POSITION	BOOT MODE
0	EXECUTE FROM 16-BIT EXTERNAL MEMORY
1	BOOT FROM 16-BIT MEMORY
2	RESERVED
3	BOOT FROM SPI MEMORY
4	BOOT FROM SPI HOST
5	BOOT FROM SERIAL TWI MEMORY
6	BOOT FROM TWI HOST
7	BOOT FROM UART HOST





Push Button Enable Switch



74LVC14A ADM708 IDT74FCT3244 QS3257 QS3257

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Title	ADSP-BF537 EZ-KIT LITE PUSH BUTTONS, LEDS AND BOOT MODE	
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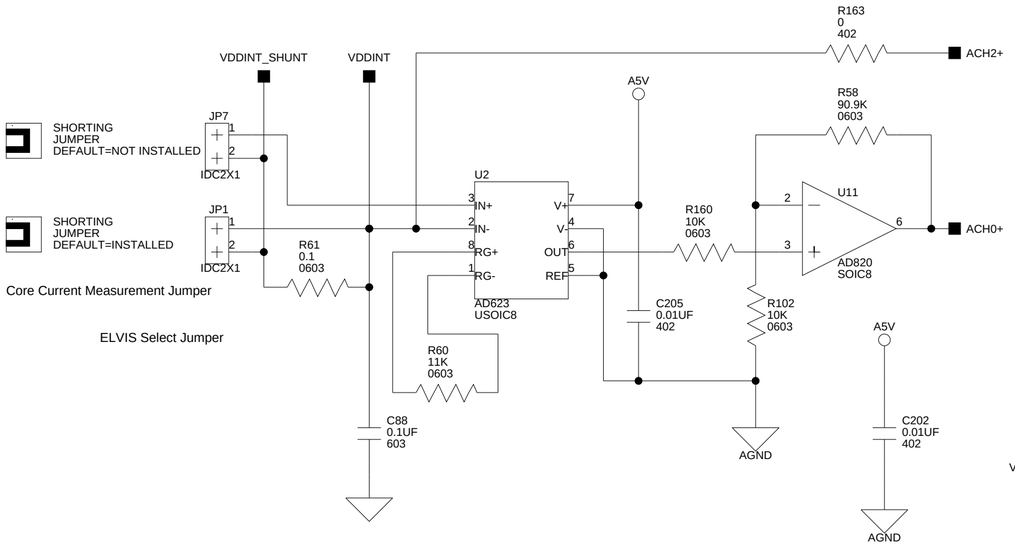
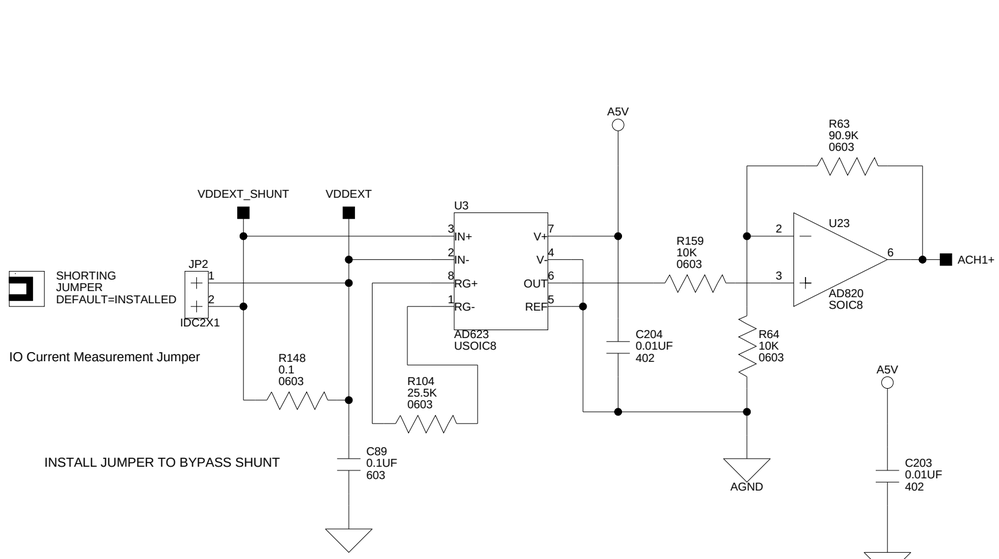
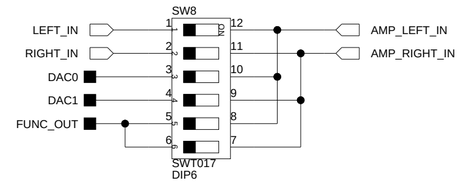


DSP CORE VOLTAGE & CURRENT

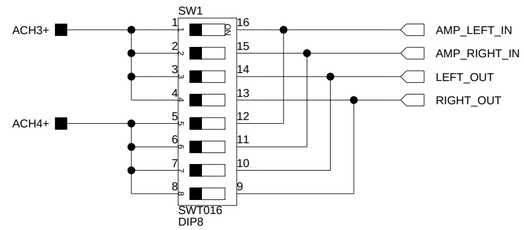
JP1	JP7	MODE
OFF	OFF	ELVIS DMM CURRENT MEASUREMENT
OFF	ON	DAQ DMM CURRENT MEASUREMENT
ON	OFF	BYPASS SHUNT CIRCUITS
ON	ON	NOT USED



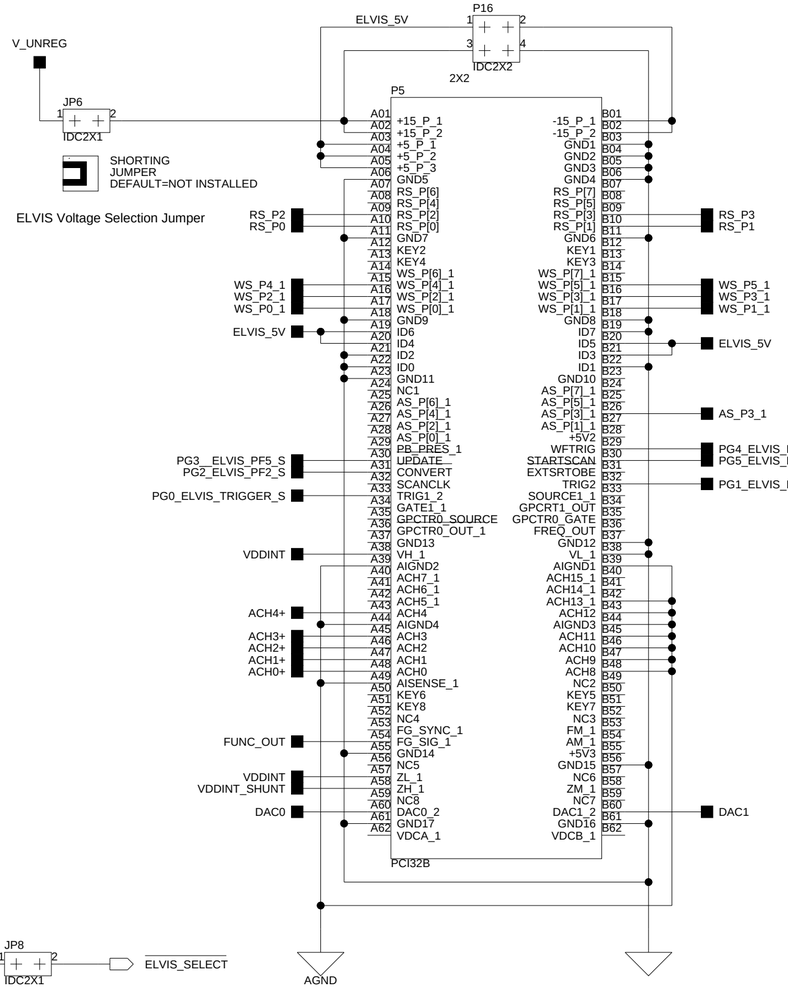
DSP IO CURRENT



Function Generator Switch



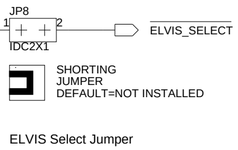
Oscilloscope Select Switch



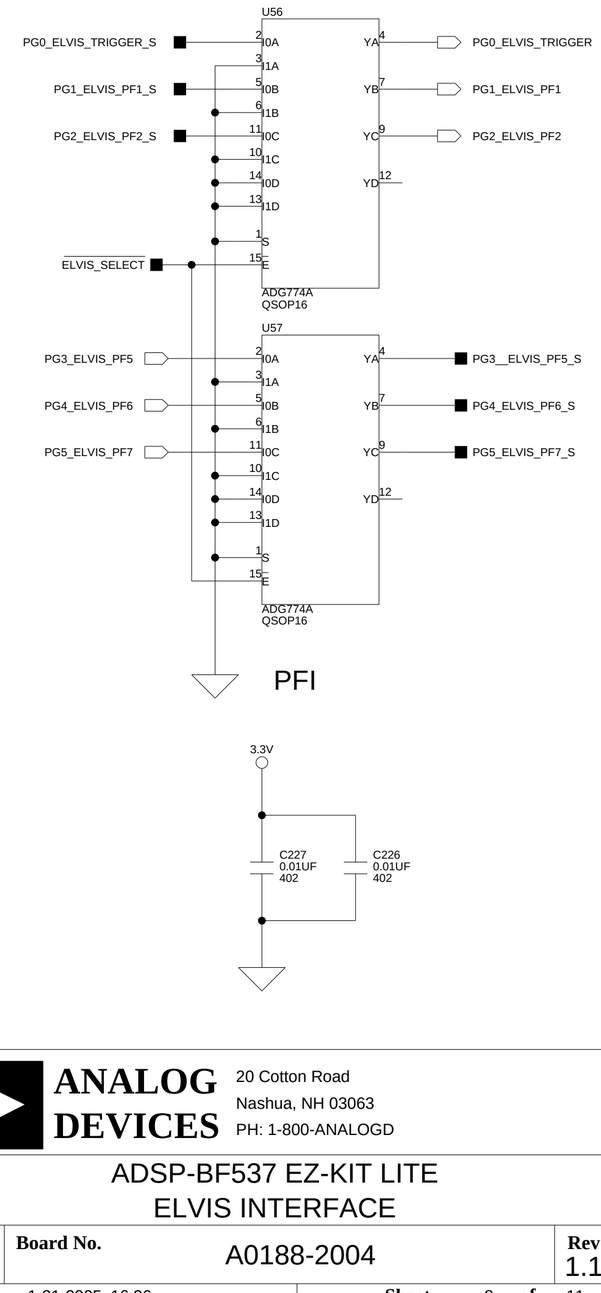
ELVIS Voltage Selection Jumper

ELVIS CONNECTOR

NI ELVIS ID 30 (0001 1110)



ELVIS Select Jumper



PFI

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Title	ADSP-BF537 EZ-KIT LITE ELVIS INTERFACE	
Size C	Board No. A0188-2004	Rev 1.1
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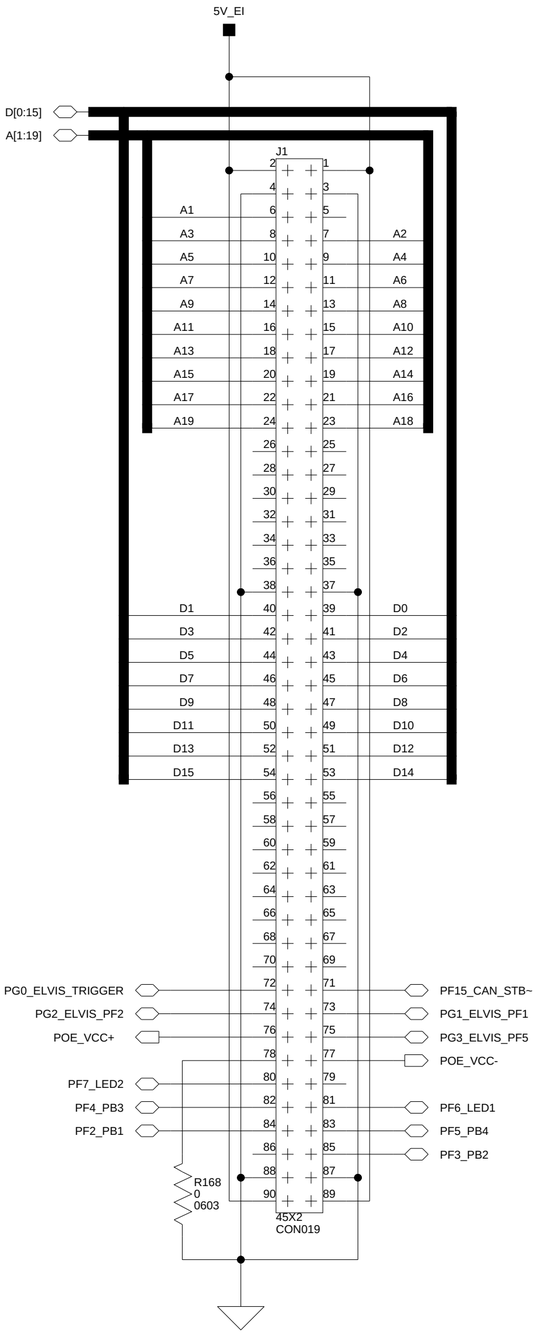
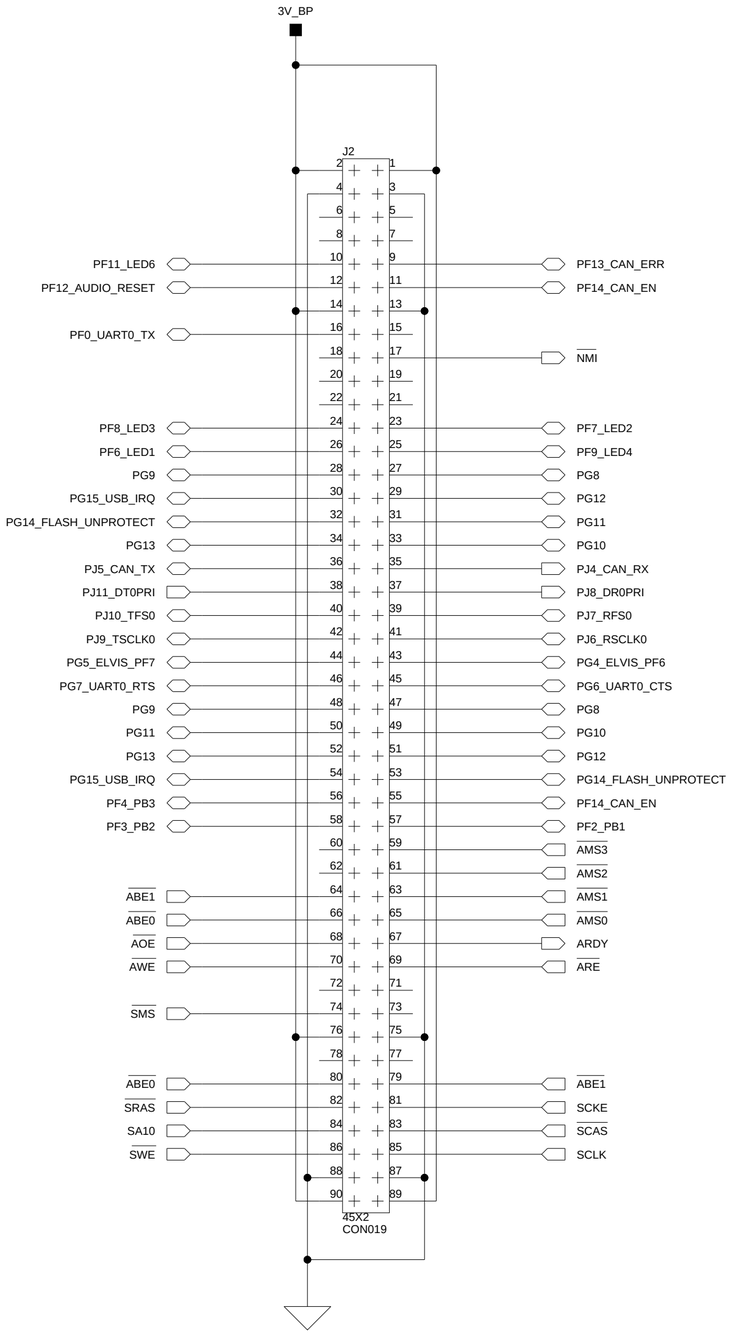
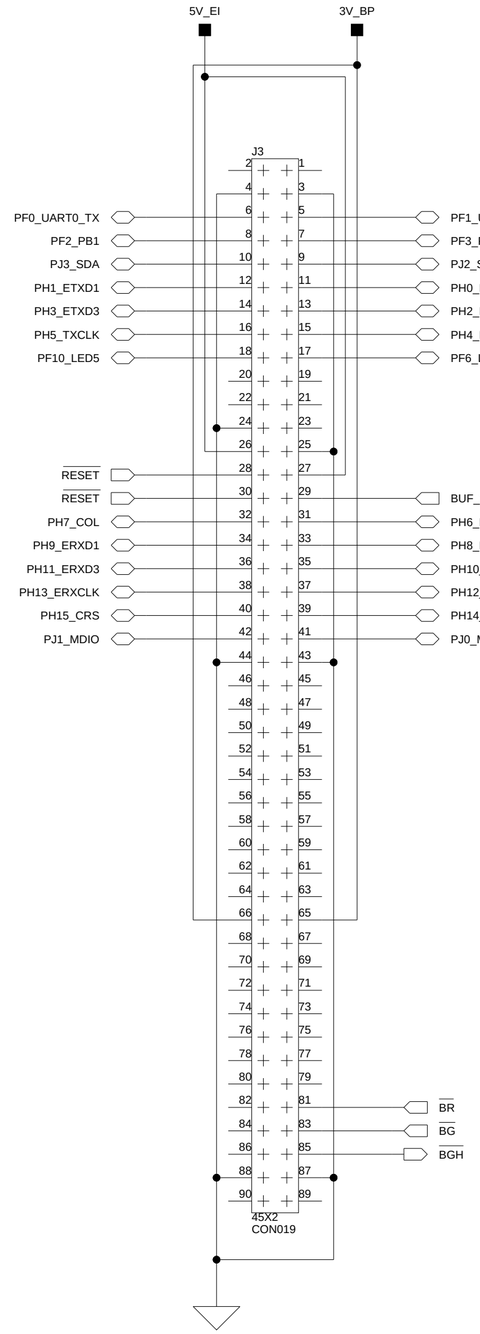
EXPANSION INTERFACE (TYPE B)

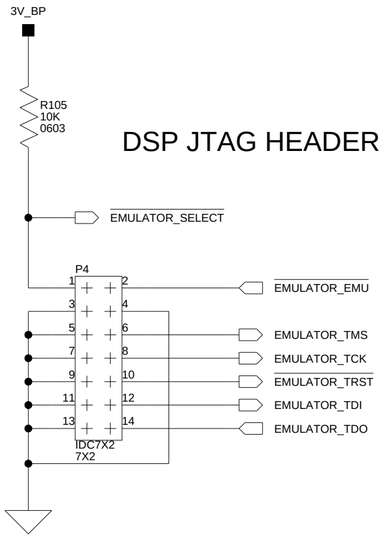






All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com



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Title	ADSP-BF537 EZ-KIT LITE EXPANSION INTERFACE		
Size C	Board No. A0188-2004		Rev 1.1
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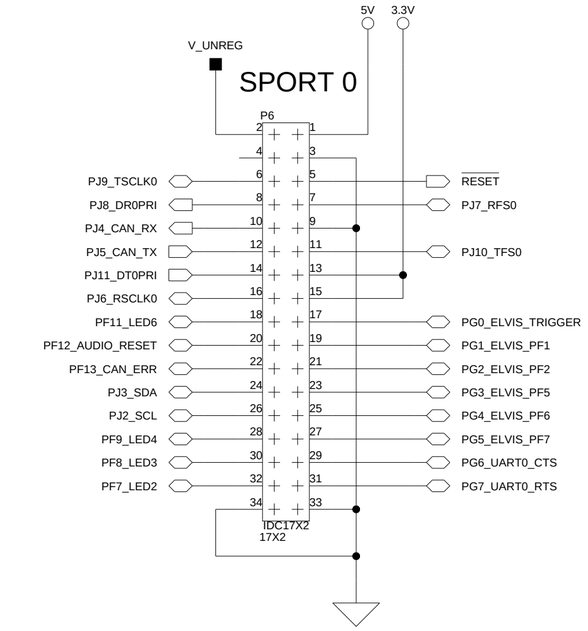

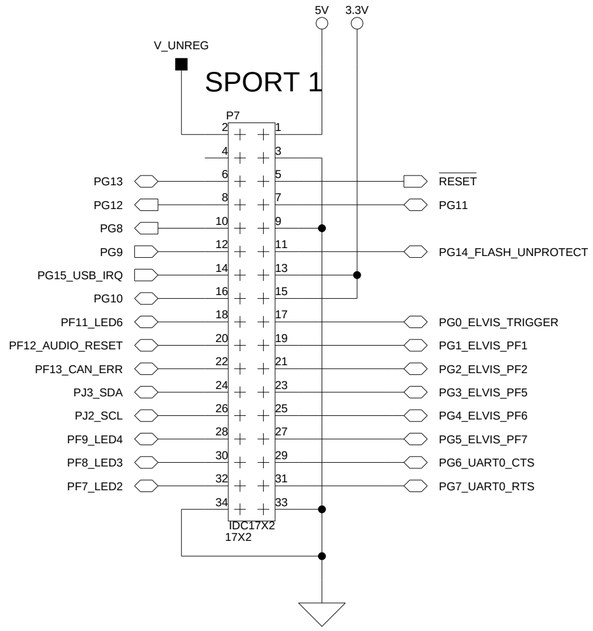

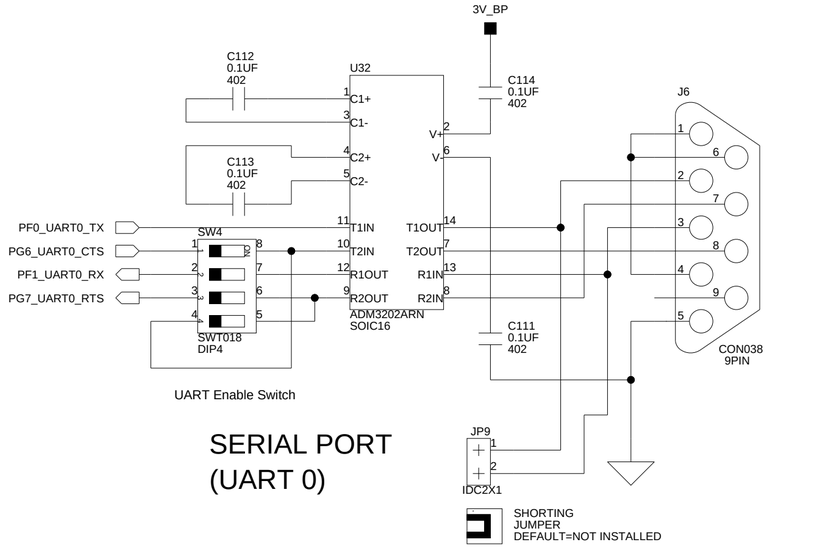

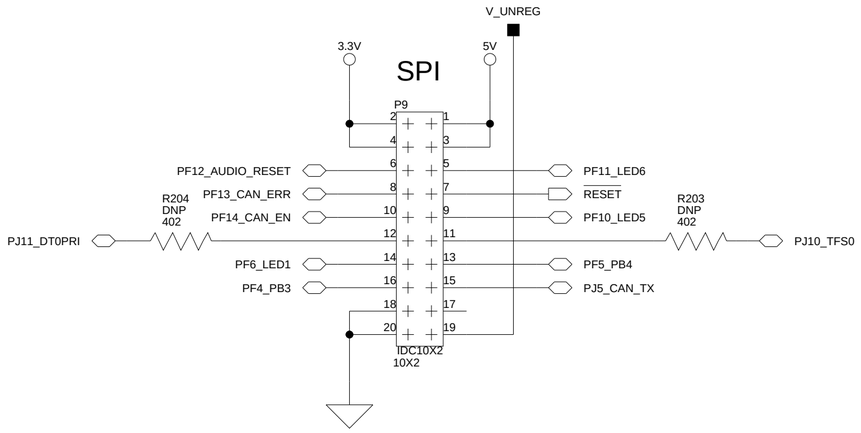

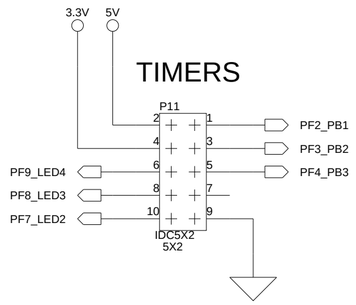

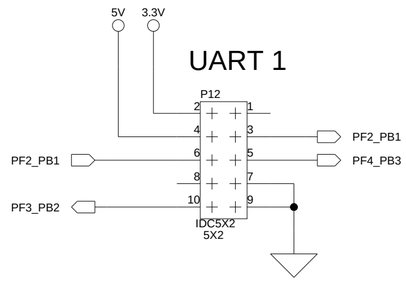

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Title: ADSP-BF537 EZ-KIT LITE STAMP CONNECTORS

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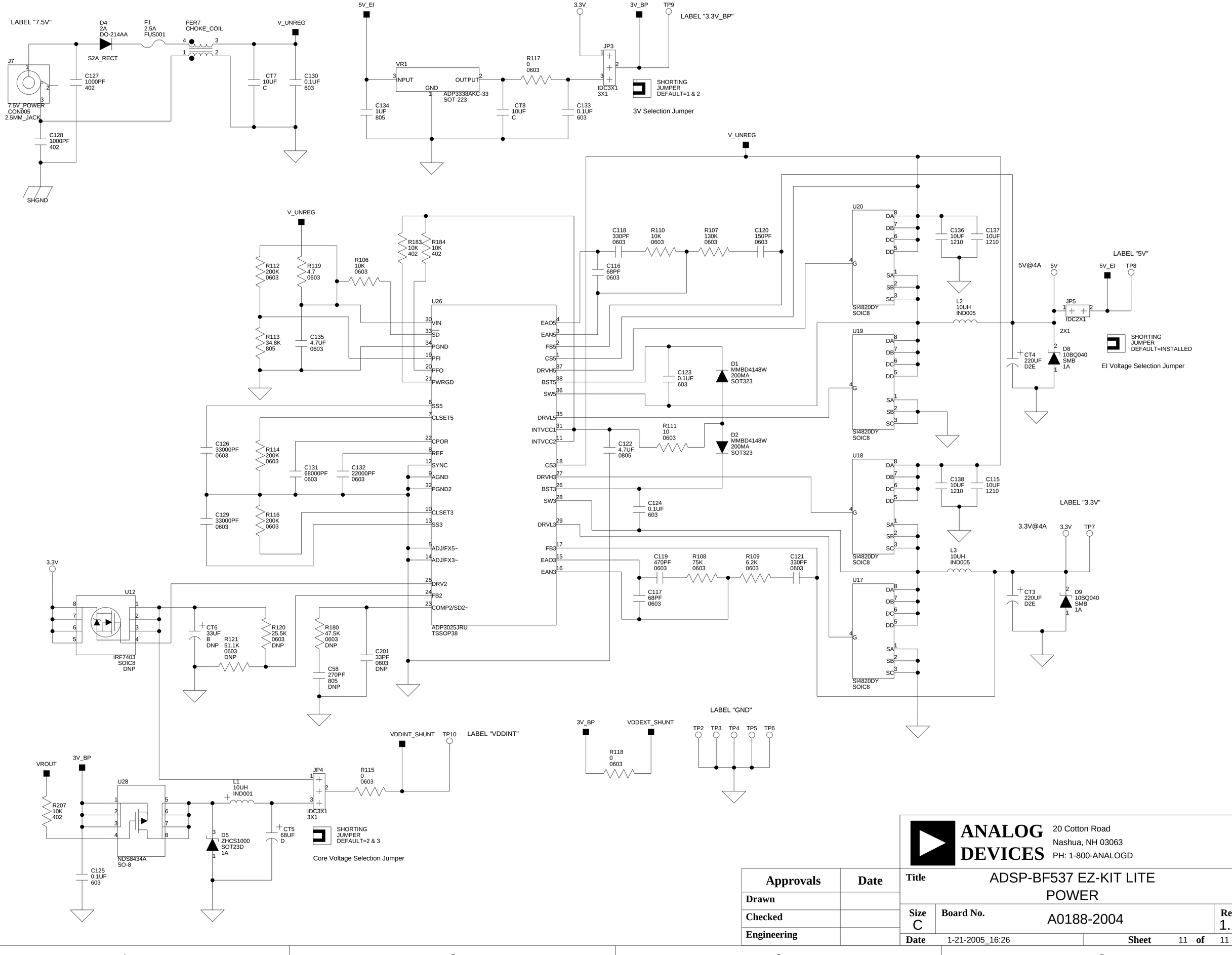

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Title	ADSP-BF537 EZ-KIT LITE POWER	
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