ADSP-TS201S EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
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ANALOG DEVICES

Copyright Information

Printed in the USA.

Limited Warranty

The EZ-KIT Lite evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The ADSP-TS201S EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The ADSP-TS201S EZ-KIT Lite evaluation system had been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

CONTENTS

PREFACE

PREFACE

Thank you for purchasing the ADSP-TS201S EZ-KIT Lite®, Analog Devices (ADI) evaluation system for TigerSHARC® floating-point embedded processors.

The TigerSHARC processor is a Static Super Scalar (SSS) architecture targeted at software-defined radio applications. In these wireless infrastructure applications, the TigerSHARC processor is replacing field-programmable gate arrays (FPGAs) in the Chip Rate processing applications for third generation cellular. The performance, flexibility, multiprocessing and IO capabilities of the TigerSHARC processor makes it superior to FPGA implementations.

The evaluation board is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-TS201S TigerSHARC processor. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-TS201S assembly
- Load, run, step-in, step-out, step-over, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-TS201S processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-TS201S processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to `http://www.analog.com/processors/tools/`.

The ADSP-TS201S EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The ADSP-TS201S EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-TS201S EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 128K words of internal memory for code space with no restrictions for data space.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

The board features:

- Two Analog Devices ADSP-TS201S processors
  - 500 MHz Core Clock Speed
  - Configurable Core Clock Mode
- Analog Devices AD1871 96 kHz Analog-to-Digital Converter
  - Line-In 3.5 mm Stereo Jack

- Analog Devices AD1854 96 kHz Digital-to-Analog Converter
  - Line-Out 3.5 mm Stereo Jack
- SDRAM Memory
  - 32 MB (4 MB x 64)
- Flash Memory
  - 512K Main Flash Memory
- USB Debugging Interface
- Interface Connectors
  - 14-Pin Emulator Connector for JTAG Interface
  - LVDS Link Ports via RJ-45 Connectors
  - Expansion Interface Connectors (not populated)
- General-Purpose IO
  - 4 Push Button FLAGS (two for each processor)
  - 2 Push Button Interrupts (one for each processor)
  - 4 LED FLAG Outputs (two for each processor)
- Analog Devices ADP3331, ADP3336, and ADP3339 for Voltage Regulation

The EZ-KIT Lite board contains two external memories: flash memory and SDRAM. The flash memory can be used to store user-specific boot code. By configuring the boot mode switch (`SW2`) and programming the flash memory, the board can run as a stand-alone unit. The SDRAM is shared by both processors and can be used to store data external to the processors. For more information, see "Memory Map" on page 1-6.

The EZ-KIT Lite board contains an audio interface, facilitating creation of audio signal processing applications.

Additionally, the EZ-KIT Lite board provides expansion connectors, allowing you to connect to the processor's external port (EP).

Purpose of This Manual

The *ADSP-TS201S EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes the operation and configuration of the board components and provides guidelines for running your own code on the ADSP-TS201S EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

The product software installation is detailed in the

Intended Audience

The primary audience of this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-TS201 TigerSHARC Processor Hardware Reference* and the *ADSP-TS201 TigerSHARC Processor Programming Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user's or getting started guides. For the locations of these documents, see "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "Using EZ-KIT Lite" on page 1-1
  Provides information on the EZ-KIT Lite from a programmer's perspective and outlines the board's memory map.
- Chapter 2, "EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the hardware aspects of the EZ-KIT Lite.
- Appendix A, "Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "Schematics" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.

This appendix is not part of the online Help. The online Help viewers should go to the PDF version of the ADSP-TS201S EZ-KIT Lite Evaluation System Manual located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics. Alternatively, the schematics can be found on the Analog Devices Web site, `www.analog.com/processors`.

What's New in This Manual

This revision of the *ADSP-TS201S EZ-KIT Lite Evaluation System Manual* provides an updated listing of related documents and updated licensing information.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the Embedded Processing and DSP products Web site at
  `http://www.analog.com/processors/technicalSupport`
- E-mail tools questions to
  `dsptools.support@analog.com`
- E-mail processor questions to
  `dsp.support@analog.com`
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:

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Norwood, MA 02062-9106
USA
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Supported Processors

The ADSP-TS201S EZ-KIT Lite evaluation system supports the Analog Devices ADSP-TS201S TigerSHARC embedded processors.

Product Information

You can obtain product information from the Analog Devices website, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at www.analog.com. Our website provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and embedded processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and processors, visit our Web site at www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
  `dsp.support@analog.com`
- Fax questions or requests for information to
  1-781-461-3010 (North America)
  +49 (89) 76 903-557 (Europe)
- Access the FTP Web site at
  `ftp ftp.analog.com` or `ftp 137.71.23.21`
  `ftp://ftp.analog.com`

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-TS201S Embedded Processor Datasheet	General functional description, pinout, and timing
ADSP-TS201 TigerSHARC Processor Hardware Reference	Description of internal processor architecture and all register functions
ADSP-TS201 TigerSHARC Processor Programming Reference	Description of all allowed processor assembly instructions

Table 2. Related VisualDSP++ Publications

Title	Description
VisualDSP++ User's Guide	Description of VisualDSP++ features and usage
VisualDSP++ Assembler and Preprocessor Manual	Description of the assembler function and commands

Table 2. Related VisualDSP++ Publications (Cont'd)

Title	Description
VisualDSP++ C/C++ Complier and Library Manual for TigerSHARC Processors	Description of the complier function and commands for TigerSHARC processors
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands
VisualDSP++ Loader Manual	Description of the loader/splitter function and commands

All documentation is available online. Most documentation is available in printed form.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

`http://www.analog.com/processors/resources/technicalLibrary`

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary `.PDF` files of most manuals are provided in the `Docs` folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
.CHM	Help system files and manuals in Help format
.HTM or .HTML	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the .HTML files requires a browser, such as Internet Explorer 4.0 (or higher).
.PDF	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the .PDF files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows® Explorer, or the Analog Devices Web site.

Accessing Documentation From VisualDSP++

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and navigate to the VisualDSP++ documentation via the **Start** menu.

To view ADSP-TS201S EZ-KIT Lite Help, which is part of the VisualDSP++ Help system, use the **Contents** or **Search** tab of the Help window.

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (.CHM) are located in the Help folder, and .PDF files are located in the Docs folder of your VisualDSP++ installation CD-ROM. The Docs folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-TS201S EZ-KIT Lite evaluation system.

Accessing Documentation From Web

Download manuals at the following Web site:
`http://www.analog.com/processors/resources/technicalLibrary/manuals`.

Select a processor family and book title. Download archive (`.ZIP`) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call **1-603-883-2430**. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto `http://www.analog.com/salesdir/continent.asp`.

Hardware Tools Manuals

To purchase EZ-KIT Lite and In-Circuit Emulator (ICE) manuals, call **1-603-883-2430**. The manuals may be ordered by title or by product number located on the back cover of each manual.

Processor Manuals

Hardware reference and instruction set reference manuals may be ordered through the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**), or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.

Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**); they also can be downloaded from the Web site.

To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 USING EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-TS201S EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "Programmable FLAG Pins" on page 1-9
  Describes the function and use of the programmable FLAG pins on the EZ-KIT Lite evaluation system.
- "Interrupt Pins" on page 1-10
  Describes the function and use of the interrupt pins on the EZ-KIT Lite evaluation system.
- "Audio Interface" on page 1-11
  Describes how to use and configure the audio interface.
- "Processor Link Ports" on page 1-11
  Describes how to use and configure the link ports.
- "Example Programs" on page 1-12
  Provides information about the example programs included in the ADSP-TS201S EZ-KIT Lite evaluation system.
- "Flash Programmer Utility" on page 1-13
  Provides information on the Flash Programmer utility included with VisualDSP++.

For detailed information about programming the ADSP-TS201S TigerSHARC processor, see the documents referred to as "Related Documents".

Package Contents

Your ADSP-TS201S EZ-KIT Lite package contains the following items.

- ADSP-TS201S EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*
- ADSP-TS201S *EZ-KIT Lite Evaluation System Manual* (this document)

- CD containing:
  - VisualDSP++ software
  - ADSP-TS201 EZ-KIT Lite debug software
  - USB driver files
  - Example programs
- Universal 7.5V DC power supply
- USB 2.0 cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-TS201S EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, DIP

switches, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration) before using the board.

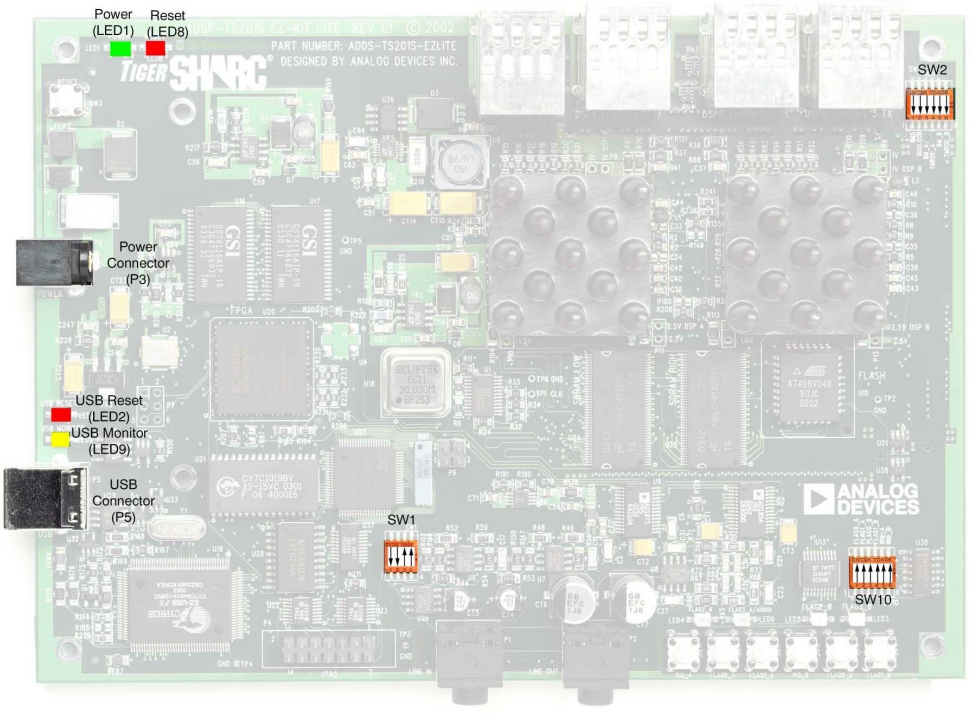


Figure 1-1. EZ-KIT Lite Hardware Setup

Installation and Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

To set up an EZ-KIT Lite session in VisualDSP++:

1. Verify that the yellow USB monitor LED (LED9, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. From the **Start** menu, navigate to the VisualDSP++ environment via the **Programs** menu.
   If you are running VisualDSP++ for the first time, the **New Session** dialog box appears on the screen (skip the rest of the procedure and go to step 3).
   If you have run VisualDSP++ previously, the last opened session appears on the screen.
   To switch to another session, via the **Session List** dialog box, hold down the **Ctrl** key while starting VisualDSP++ (go to step 5).
3. In Debug Target, choose **TigerSHARC Emulators/EZ-KIT Lites**.
   In **Platform**, select **ADSP-TS201 EZ-KIT Lite via Debug Agent**.
   In **Session name**, type a new name or accept the default.
4. Click **OK** to return to the **Session List**.
5. Highlight the session and click **Activate**.

Evaluation License Restrictions

The ADSP-TS201S EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-TS201S EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 128K words of internal memory for code space with no restrictions for data space.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

Memory Map

The ADSP-TS201S processor has 24 Mbits of internal memory that can be used for program storage or data storage. The configuration of internal memory is detailed in the *ADSP-TS201 TigerSHARC Processor Hardware Reference*.

The ADSP-TS201S EZ-KIT Lite board contains 512K x 8-bit of external flash memory. The memory is divided into eight uniform 64 Kb sections. This memory connects to the processor's ~BMS and ~MS0 pins. The flash memory can be accessed in boot memory space as well as the external memory bank zero space.

The board also contains 4M x 64-bit of external SDRAM memory. This memory connects to the processor's SDRAM interface.

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map

	Start Address	End Address	Content
Internal Memory	0x0000 0000	0x 0001 FFFF	Internal Memory 0
	0x0004 0000	0x0005 FFFF	Internal Memory 2
	0x0008 0000	0x0009 FFFF	Internal Memory 4
	0x000C 0000	0x000D FFFF	Internal Memory 6
	0x0010 0000	0x0011 FFFF	Internal Memory 8
	0x0014 0000	0x0015 FFFF	Internal Memory 10
	0x001E 0000	0x001E 03FF	Internal Registers
	0x001F 0000	0x001F 03FF	SOC Registers
	0x0C00 0000	0x0FFF FFFF	Broadcast
	0x1000 0000	0x13FF FFFF	Processor ID 0
	0x1400 0000	0x17FF FFFF	Processor ID 1
External Memory	0x3000 0000	0x37FF FFFF	External Memory Space Bank 0 (MS0); MS0 includes flash memory which ends at 0x3007 FFFF.
	0x3800 0000	0x39FF FFFF	External Memory Space Bank 1
	0x4000 0000	0x43FF FFFF	External Memory Space (MSSD0); MSSD0 includes SDRAM which ends at 0x407F FFFF.
	0x8000 0000	0xFFFF FFFF	Host

SDRAM Interface

The SDRAM on the EZ-KIT Lite evaluation board is 32 MB. To access SDRAM, the SYSCON and SDRCON registers must be configured properly. The SDRAM default values are:

- SYSCON = 0x00189067
- SDRCON = 0x00005983

For the supplied memory, the SDRCON register should be configured as follows:

- SDRAM enable, CAS latency of two cycles
- pipe depth of zero, page boundary of 256 words
- refresh rate of every 3700 cycles, precharge to RAS of two cycles
- RAS to precharge of five cycles
- init sequence is MRS cycle follows refresh

The SYSCON and SDRCON registers define bus control configuration. They can be written once only after reset and cannot be changed during system operation.

In emulation space, the SYSCON and the SDRCON registers can be written to as many times as needed. The USB debug monitor operates in emulation space and allows "always writable" mode for these registers.

Flash Memory

The AT49BV040 chip provides a total of 512K x 8-bits of external flash memory, arranged into eight uniform 64 Kb memory blocks. The block addresses are shown in Table 1-2.

Table 1-2. Flash Memory Map

Start Address	End Address	Content
0x3000 0000	0x3000 FFFF	Uniform Block 0
0x3001 0000	0x3001 FFFF	Uniform Block 1
0x3002 0000	0x3002 FFFF	Uniform Block 2
0x3003 0000	0x3003 FFFF	Uniform Block 3

Table 1-2. Flash Memory Map (Cont'd)

Start Address	End Address	Content
0x3004 0000	0x3004 FFFF	Uniform Block 4
0x3005 0000	0x3005 FFFF	Uniform Block 5
0x3006 0000	0x3006 FFFF	Uniform Block 6
0x3007 0000	0x3007 FFFF	Uniform Block 7

To program the flash memory with your boot code, you must first create a loader file from your processor code. You set up the loader in VisualDSP++ depending on how you plan to boot the flash. For information on creating a loader file, refer to VisualDSP++ online help and the *VisualDSP++ Loader Manual*.

Next, the loader file must be programmed into the flash memory. This can be done using the VisualDSP++ Flash Programmer utility (see "Flash Programmer Utility" on page 1-13).

Programmable FLAG Pins

Each ADSP-TS201S processor has four programmable FLAG pins. Two FLAG pins from each processor (FLAG0 and FLAG1) allow interaction with the running program through the use of a switch (SW6-9). The FLAG2 and FLAG3 pins from each processor are connected to LEDs (LED3-6).

After the processor is reset, the programmable FLAGs are configured as inputs. The direction of each programmable FLAG is configured in the FLAGREG register. If the FLAG is configured for an output, the value to be output is set in the FLAGREG register. If the FLAG is configured for an input, the value on the FLAG pin is read from the SQSTAT register. Programmable FLAGs are summarized in Table 1-3. For more information on how to configure the programmable FLAG pins, see the *ADSP-TS201S TigerSHARC Processor Hardware Reference*.

Table 1-3. Programmable FLAG Pin Summary

FLAG	Connected To	Use
FLAG0_A	SW9	The FLAG0 and FLAG1 pins are connected to the push buttons to supply feedback for program execution. For instance, you can write user input to trigger a routine when the push button is pressed.
FLAG1_A	SW8	
FLAG0_B	SW6	
FLAG1_B	SW7	
FLAG2_A	LED4	The FLAG2 and FLAG3 pins are connected to the LEDs to supply feedback during program execution.
FLAG3_A	LED6	
FLAG2_B	LED5	
FLAG3_B	LED3	

Interrupt Pins

The ADSP-TS201S processor includes four interrupt pins (IRQ3-0) for interaction with the running program. One external interrupt from each processor is directly accessible through push button switches SW4 and SW5 on the EZ-KIT Lite board. Interrupts are summarized in Table 1-4. For more information on configuring the interrupt pins, see the *ADSP-TS201S TigerSHARC Processor Hardware Reference*.

Table 1-4. Interrupt Pin Summary

Interrupt	Connected To	Use
IRQ0_A	SW4	The IRQ0 interrupt is connected to push buttons to supply feedback for program execution. For instance, you can write your code to perform a different function when an interrupt is detected.
IRQ0_B	SW5	

Audio Interface

The audio interface of the EZ-KIT Lite board allows you to interface with the board's analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The audio interface consists of two main ICs: AD1871 and AD1854.

The AD1871 is a stereo audio ADC intended for digital audio applications requiring high-performance analog-to-digital conversion. The AD1871 provides 97 dB THD+N and 107 dB dynamic range.

The AD1854 is a high-performance, single-chip stereo, audio DAC delivering 113 dB dynamic range and 112 dB SNR at a 48 kHz sample rate.

Because the ADSP-TS201S processor does not have any SPORTs, an Xilinx field-programmable gate array (FPGA) generates the audio interface control signals between the processor and the audio circuit. Setting the FLAG3 signal of processor A "high" enables the audio interface inside of the FPGA. Once the audio interface has been enabled, the audio data can be transferred to and from the processor by generating a DMAR0 cycle. The audio data interfaces with the processor via the lowest 24 bits of the data bus (D23-0).

Refer to the audio example program included in the EZ-KIT Lite's installation directory for more information on how to use the audio interface. Refer to "Audio (P1–2)" on page 2-20 for information about the audio connectors.

Processor Link Ports

The link ports on the ADSP-TS201S processor use LVDS signaling to communicate with each another. Each processor has a TX (transmit) port and RX (receive) port for each of its link ports. The RJ-45 connectors, J4 and J5, are the TX and RX for processor A. Similarly, J6 and J7 are TX and RX for processor B. The TX and RX of one processor's link ports

should be respectively connected to RX and TX of another processor's link port. In this manner, the TX of one processor connects to the RX of the other processor.

The link ports should be connected using a standard CAT 5E networking cable. The length of the cable may affect the maximum frequency at which the data can be transferred. Refer to the ADSP-TS201S *Embedded Processor Datasheet* for more information.

There are four link ports on each of the processors on the EZ-KIT Lite. `Link Port0` of both processors connects to the field-programmable gate array (FPGA) at `U20`. `Link Port1` of both processors connects to `J3` of the expansion interface. `Link Port2` of each of the processors connects to each other. Finally, `Link Port3` connects to the RJ-45 connectors (`J4-J7`).

The `LOCLKIN_P` of both processor A and processor B are pulled up internally in the FPGA. Similarly, `LOCLKININ_N` of both processor A and processor B are pulled down internally in the FPGA. Finally, `R12` and `R28` are not populated. All of this is done to avoid noise affecting the EZ-KIT Lite operation.

To suppress noise from the expansion interface, a similar pull-up or pull-down scheme has been used on `Link Port1`. The board's `R240` and `R239` are used to pull up `L1CLKIN_P` of both processors. Similarly, `R242` and `R241` are used to pull down `L1CLKIN_N` of both processors. Finally, `R14` and `R30` are not populated to avoid a short between 2.5V power and `GND`. The link ports can be reactivated by removing the pull up and pull downs and adding a 100 Ohm resistor on `R14` and `R30`.

Example Programs

Example programs are provided with the ADSP-TS201S EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in the

`\…\TS\EZ-KITs\ADSP-TS201\Examples` subdirectory of the VisualDSP++ installation directory. Please refer to the readme file provided with each example program for more information.

When running the examples, do not change these bits:
`BGEN` or `NMOD` (bits 8 or 9) in the `SQCTL` register.
The change can disable communications with the host.

Flash Programmer Utility

The ADSP-TS201S EZ-KIT Lite evaluation system includes a Flash Programmer utility. The utility allows you to program the flash memory on the EZ-KIT Lite. The Flash Programmer is installed with VisualDSP++. Once the utility is installed, it is accessible from the **Tools** pull-down menu.

For more information on the Flash Programmer utility, refer to the online Help.

2 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-TS201S EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the ADSP-TS201S processor and explains how the board components interface with the EZ-KIT Lite.
- "Switch Settings" on page 2-5
  Shows the location and describes the function of each configuration DIP switch.
- "Configuration Resistors" on page 2-10
  Shows the location and describes the function of each configuration resistor.
- "LEDs and Push Buttons" on page 2-16
  Shows the location and describes the function of the LEDs and push buttons.
- "Connectors" on page 2-19
  Shows the location of and gives the part number for all of the connectors on the board. In addition, provides the manufacturer and part number information for the mating parts.
- "Specifications" on page 2-22
  Describes the power connector.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

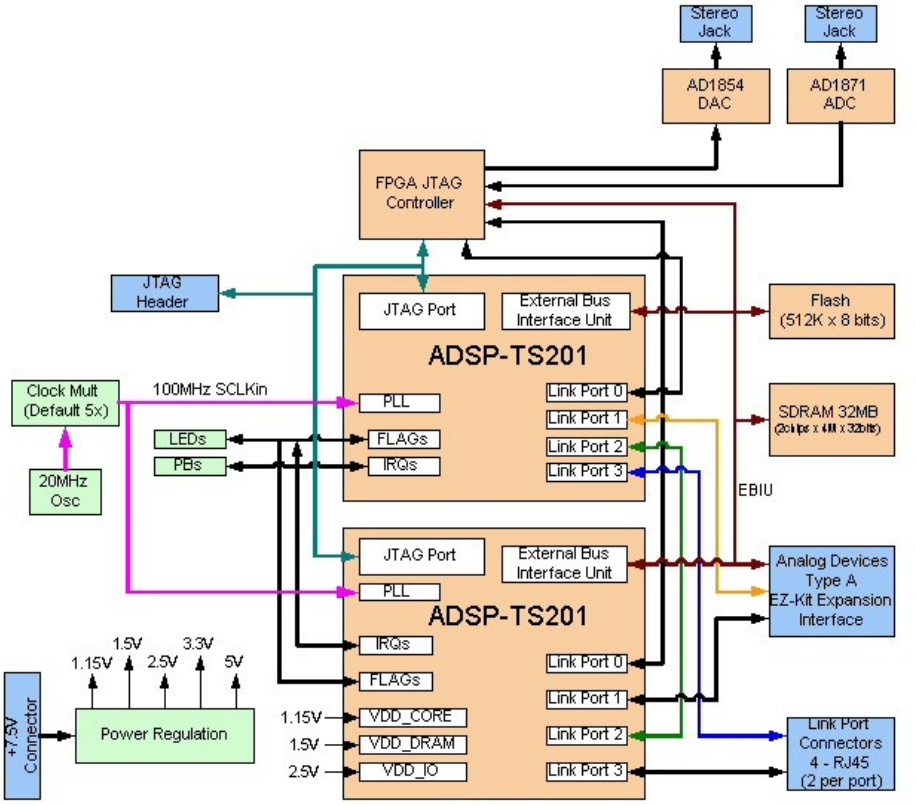


Figure 2-1. System Architecture

The EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-TS201S TigerSHARC processor. The processor is powered by three separate regulators for the core, the internal DRAM, and the IO.

The processor core voltage is set to 1.15V. The internal DRAM is powered by an external 1.5V regulator. Finally, the external interface (IO) operates at 2.5V but can accept up to 3.3V levels.

A 20 MHz SMT oscillator in conjunction with a clock generator set to 5x supply the input clock to the processors. The speed at which the core operates is determined by pull-up and pull-down resistors on both the clock generator (U1) and the SCLKRAT[2:0] bit of each of the processors. For more information, see "Clock Mode Settings" on page 2-12. By default, the processor core runs at 500 MHz (20 MHz x 5 (U1) x 5 (sclkrat) =500 MHz).

External Port

The external port (EP) connects to a 512K x 8-bit flash memory. The flash memory connects to the boot memory select pin (~BMS) and memory bank zero pin (~MS0), allowing the memory to be used to boot the processor as well as to store information during normal operation. Refer to "Flash Memory" on page 1-8 for information about the flash memory locations.

The EP also connects to a 4M x 64-bit SDRAM. Refer to "SDRAM Interface" on page 1-7 for information on how to configure the SDRAM registers.

Expansion Interface

The expansion interface consists of three connectors. The following table shows the interfaces each connector provides. For the exact pinout of these connectors, refer to Appendix B, "Schematics".

Table 2-1. Expansion Interface Connectors

Connector	Interfaces
J1	5V, GND, Address, Data
J2	2.5V, GND, SDRAM control signals, FLAGs, IRQs, TIMERs, Data
J3	GND, Reset, DMA, Memory Control, CLKOUT, Link Ports signals

When you use the expansion interface, limits to the current and to the interface speed must be taken into consideration. The maximum current limit depends on the capabilities of the regulator. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory, as well as the special function registers through a 14-pin header. See "JTAG (P4)" on page 2-21 for more information about the JTAG connector. To learn more about available emulators, contact Analog Devices as described in "Product Information" on page -xv.

For more information about designing JTAG into a custom board or to learn more about the JTAG interface, please refer to *EE-68* found at Analog Devices website.

Switch Settings

This section describes the function of the DIP switches SW1, SW2, and SW10. The location of the switches and their respective default settings are shown in Figure 2-2.

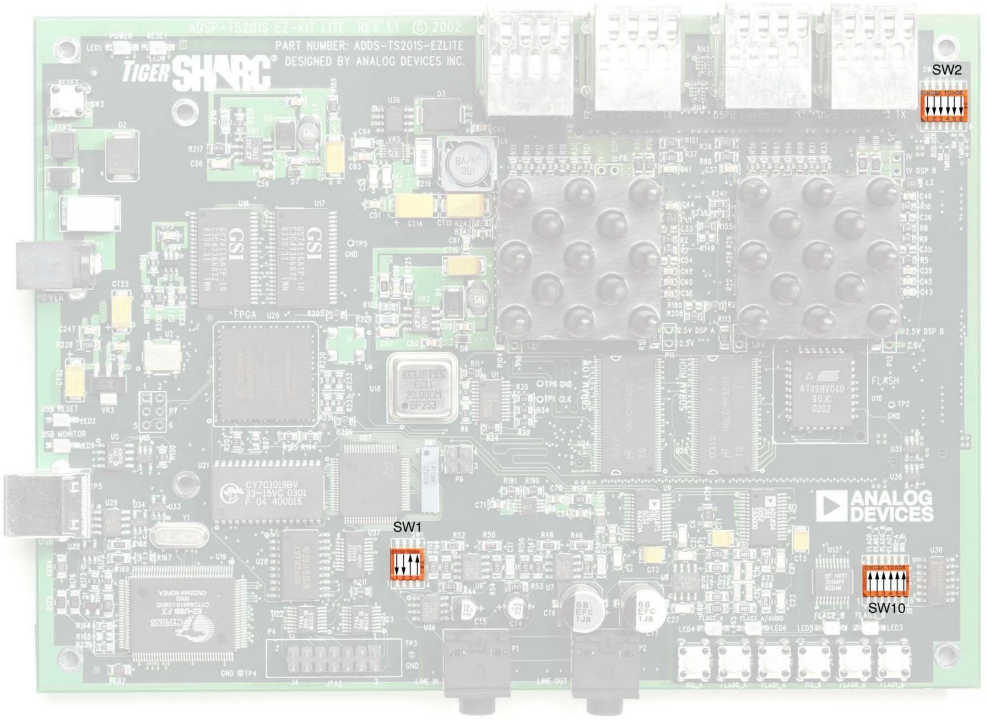


Figure 2-2. Switch Locations

Audio Amplification Selection (SW1)

The SW1 switch determines the amplification of right and left signals connected to the Line-IN connector P1. A non-powered electret microphone can be used by simply varying the switch setting to the values shown in Table 2-2. An amplification gain of a factor of 10 can be achieved by setting the switch into electret microphone use.

Table 2-2. Audio Amplification Selection (SW1)

Position 1	Position 2	Position 3	Position 4	Audio Amplification Mode
OFF[1]	OFF	ON	ON	No amplification
ON	ON	OFF	OFF	For electret microphone use

1 Default settings

Processor Mode Selections (SW2)

The SW2 switch configures several processor strap pins, which set the processor's operating modes after power up or hard reset:

- "Processor Boot Strap Settings"
- "SYSCON/SDRCON Mode Settings"
- "Interrupt Enable Settings"
- "Link Port Width Settings"

The switch settings should not be changed while power is applied to the board. Many of the strap pin settings may be re-configured in software after the processor is powered up. Refer to the *ADSP-TS201S Embedded Processor Datasheet* for more information.

Processor Boot Strap Settings

Position 1 of the SW2 switch determines how the processor boots. Table 2-3 shows the available boot mode settings. Refer to the *ADSP-TS201S Embedded Processor Datasheet* for more information.

Table 2-3. Processor Boot Strap Settings (SW2 Position 1)

Position 1	Boot Mode
OFF[1]	**EPROM Boot**
ON	External Boot or Link Port Boot

1 Default settings

SYSCON/SDRCON Mode Settings

Position 2 of the SW2 switch determines how the processor handles writes to the SYSCON and SDRCON registers. Table 2-4 shows the setting for the type of write. Refer to the *ADSP-TS201S Embedded Processor Datasheet* for more information.

Table 2-4. SYSCON/SRDCON Mode Settings (SW2 Position 2)

Position 2	SYSCON/SDRCON Mode
OFF[1]	**SYSCON/SDRCON one-time writable**
ON	SYSCON/SDRCON always writable

1 Default settings

In emulation space, the SYSCON and SDRCON registers can be written to as many times as needed. The USB debug monitor operates in emulation space and allows “always writable” mode for these registers.

Interrupt Enable Settings

Positions 3 and 5 of the SW2 switch determine how each of the processor handles interrupts. Table 2-5 and Table 2-6 show the settings for the interrupt modes. Refer to the *ADSP-TS201S Embedded Processor Datasheet* for more information.

Table 2-5. Interrupt Enable Settings (SW2 Position 3)

Position 3	Interrupt Enable Mode for Processor A (U11)
OFF[1]	**Disable interrupts, level-sensitive mode**
ON	Enable interrupts, edge-sensitive mode

1 Default settings

Table 2-6. Interrupt Enable Settings (SW2 Position 5)

Position 5	Interrupt Enable Mode for Processor B (U12)
OFF[1]	**Disable interrupts, level-sensitive mode**
ON	Enable interrupts, edge-sensitive mode

1 Default settings

Link Port Width Settings

Positions 4 and 6 of the SW2 switch determine the link port data width. Table 2-7 and Table 2-8 show the settings for the two types of link ports data widths. Refer to the *ADSP-TS201S Embedded Processor Datasheet* for more information.

Table 2-7. Link Port Width Settings (SW2 Position 4)

Position 4	Link Port Data Width for Processor A (U11)
OFF[1]	**1-Bit link port data width**
ON	4-Bit link port data width

1 Default settings

Table 2-8. Link Port Width Settings (SW2 Position 6)

Position 6	Link Port Data Width for Processor B (U12)
OFF[1]	**1-Bit link port data width**
ON	4-Bit link port data width

1 Default settings

FLAGs and IRQs Switch Settings (SW10)

The SW10 switch determines the source of the FLAG and IRQ signals connected to each of the prospective processors. The source can be modified so that the nets can be driven by either a push button switch or an external source via the Expansion Header. Refer to "Programmable FLAG Push Buttons (SW6–9)" and "Interrupt Push Buttons (SW4–5)" on page 2-18 for information on FLAGs, IRQs, and the associated push buttons. Table 2-9 shows the setting for the interrupt modes.

Table 2-9. FLAGs and IRQs Switch Settings (SW10)

DSP A		DSP B		DSP A	DSP B	Use With
Position 1 (FLAG0)	**Position 2 (FLAG1)**	**Position 3 (FLAG0)**	**Position 4 (FLAG1)**	**Position 5 (IRQ0)**	**Position 6 (IRQ0)**	
OFF	OFF	OFF	OFF	OFF	OFF	External source
ON[1]	ON	ON	ON	ON	ON	On-board push button switch

1 Default settings

Configuration Resistors

This section describes the function of the two TigerSHARC processors' configuration resistors. The location of the configuration resistors and their respective default settings are shown in Figure 2-3.

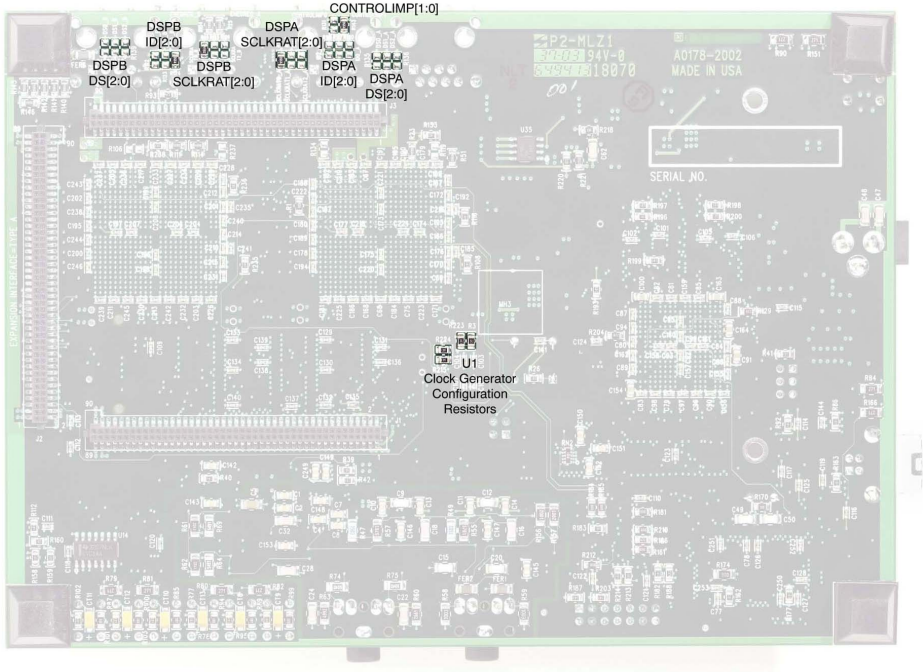


Figure 2-3. Resistor Locations (Bottom View of Board)

Processor ID Settings

The two ADSP-TS201S processors on the EZ-KIT Lite are factory-configured to set the processor A to an ID value of zero and processor B to an ID value of one. This means that in the cluster processor A is the master.

Although it is not recommended, the ID value of each processor can be varied by placing 500 Ohm resistors in the appropriate position. Table 2-10 and Table 2-11 show the available ID settings.

The EZ-KIT Lite must have a processor with the processor ID set to zero (0) on the board. ID0 must be present in order to allow initialization of SDRAM external memory. Internal pull-up or pull-downs on certain pins, such as memory interface and bus arbitration, are enabled only when the ID=(000). Refer to the *ADSP-TS201S TigerSHARC Processor Hardware Reference* for more information.

Table 2-10. Processor A ID Pins Configuration

R115 (Net: ID2_A)	R117 (Net: ID1_A)	R120 (Net: ID0_A)	ID[2:0] Value
Not populated[1]	**Not populated**	**Not populated**	0
Not populated	Not populated	Populated	1
Not populated	Populated	Not populated	2
Not populated	Populated	Populated	3
Populated	Not populated	Not populated	4
Populated	Not populated	Populated	5
Populated	Populated	Not populated	6
Populated	Populated	Populated	7

1 Default settings

Table 2-11. Processor B ID Pins Configuration

R122 (Net: ID2_B)	R123 (Net: ID1_B)	R124 (Net: ID0_B)	ID[2:0] Value
Not populated	Not populated	Not populated	0
Not populated[1]	**Not populated**	**Populated**	1
Not populated	Populated	Not populated	2

Table 2-11. Processor B ID Pins Configuration (Cont'd)

R122 (Net: ID2_B)	R123 (Net: ID1_B)	R124 (Net: ID0_B)	ID[2:0] Value
Not populated	Populated	Populated	3
Populated	Not populated	Not populated	4
Populated	Not populated	Populated	5
Populated	Populated	Not populated	6
Populated	Populated	Populated	7

1 Default settings

Clock Mode Settings

The resistors on the clock generator (U1) and the resistors on the SCLKRAT pins[2:0] of each of the processors determine the frequency at which the two processor operate. The frequency supplied to CLKIN of the processor may also be changed by replacing the 20 MHz oscillator (U18) shipped with the board with a different oscillator. Ensure that the selected clock mode and frequency do not exceed the minimum and maximum specifications of the ADSP-TS201S processor as noted in the datasheet.

The final frequency at which the processors operate is determined by the following equation:

```
(Freq of U18)*(Mult Factor of U1)*(Mult Factor of SCLKRAT pins) =
Final Oper Freq
```

The default frequency factory setting is 20 MHz*5*5 = 500 MHz.

Table 2-12 through Table 2-14 show the resistor settings for the clock generator and the SCLKRAT pins. For more information on the clock modes, see the *ADSP-TS201S Embedded Processor Datasheet*.

The Processor A and Processor B SCLK ratios must be of the same value.

Table 2-12. Clock Generator (U1) Settings

R215	R224	R3	R223	Multiplication Factor
Not populated	Populated	Not populated	Populated	2
Not populated	Populated	Populated	Populated	3
Not populated	Populated	Populated	Not populated	4
Populated	Populated	Not populated	Populated	4.25
Populated[1]	**Populated**	**Populated**	**Populated**	5
Populated	Populated	Populated	Not populated	6
Populated	Not populated	Not populated	Populated	6.25
Populated	Not populated	Populated	Populated	8
Populated	Not populated	Populated	Not populated	Reserved (Test mode)

1 Default settings

Table 2-13. SCLK Ratio Settings for Processor A

R128 (SCLKRAT2)	R127 (SCLKRAT1)	R133 (SCLKRAT0)	Multiplication Factor
Not populated	Not populated	Not populated	4
Not populated[1]	**Not populated**	**Populated**	5
Not populated	Populated	Not populated	6
Not populated	Populated	Populated	7
Populated	Not populated	Not populated	8
Populated	Not populated	Populated	10
Populated	Populated	Not populated	12
Populated	Populated	Populated	Reserved

1 Default settings

Table 2-14. SCLK Ratio Settings for Processor B

R126 (SCLKRAT2)	R125 (SCLKRAT1)	R45 (SCLKRAT0)	Multiplication Factor
Not populated	Not populated	Not populated	4
Not populated[1]	**Not populated**	**Populated**	5
Not populated	Populated	Not populated	6
Not populated	Populated	Populated	7
Populated	Not populated	Not populated	8
Populated	Not populated	Populated	10
Populated	Populated	Not populated	12
Populated	Populated	Populated	Reserved

1 Default settings

Control Impedance Selection

The CONTROLIMP1 and CONTROLIMP0 resistors set the impedance and driver mode of the processors, as described in Table 2-15. The resistors are used together with the drive strength pins to determine the actual impedance and drive strength. Refer to the *ADSP-TS201S Embedded Processor Datasheet* for more information.

Table 2-15. Control Impedance Selection

R143 (CONTROLIMP1)	R131 (CONTROLIMP0)	Driver Mode
Populated[1]	**Not populated**	**Normal**
Populated	Populated	Pulse mode
Not populated	Not populated	A/D mode
Not populated	Populated	Pulse mode, A/D mode

1 Default settings

Drive Strength Selection

The DS[2:0] pins of each processor determine the digital drive strength, as described in Table 2-16 and Table 2-17. Refer to the *ADSP-TS201S Embedded Processor Datasheet* for more information.

Table 2-16. Drive Strength Setting for Processor A

R136 (DS2)	R132 (DS1)	R135 (DS0)	Drive Strength	Output Impedance
Populated	Not populated	Populated	11.1%	26Ω
Populated	Not populated	Not populated	23.8%	32Ω
Populated	Populated	Populated	36.5%	40Ω
Populated	Populated	Not populated	49.2%	50Ω
Not populated	Not populated	Populated	61.9%	62Ω
Not populated[1]	**Not populated**	**Not populated**	**74.6%**	**70Ω**
Not populated	Populated	Populated	87.3%	96Ω
Not populated	Populated	Not populated	100%	120Ω

1 Default settings

Table 2-17. Drive Strength Setting for Processor B

R138 (DS2)	R139 (DS1)	R137 (DS0)	Drive Strength	Output Impedance
Populated	Not populated	Populated	11.1%	26Ω
Populated	Not populated	Not populated	23.8%	32Ω
Populated	Populated	Populated	36.5%	40Ω
Populated	Populated	Not populated	49.2%	52Ω
Not populated	Not populated	Populated	61.9%	62Ω
Not populated[1]	**Not populated**	**Not populated**	**74.6%**	**70Ω**
Not populated	Populated	Populated	87.3%	96Ω
Not populated	Populated	Not populated	100%	120Ω

1 Default settings

LEDs and Push Buttons

This section describes the function of the LEDs and push buttons. Figure 2-4 shows the locations of the LEDs and push buttons.

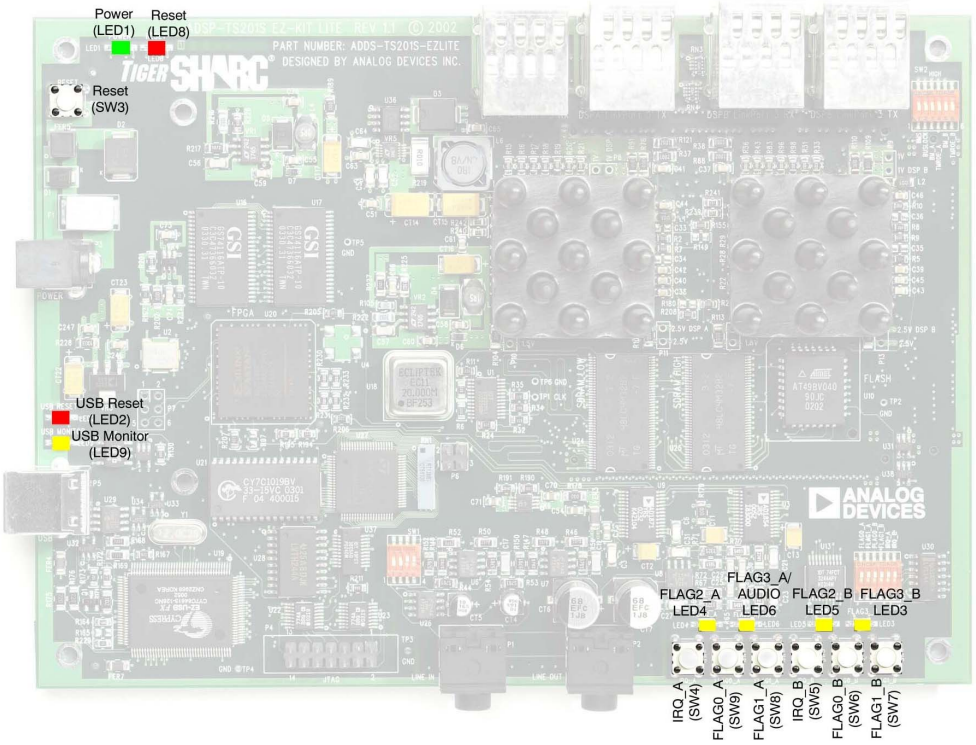


Figure 2-4. LED and Push Button Locations

Power LED (LED1)

The green LED, `LED1`, indicates that power is being properly supplied to the board.

Reset LEDs (LED2 and LED8)

When LED2 is lit, the USB interface is being reset. This interface is only reset when it is not configured. Once it has been configured, you must remove power to reset the USB interface.

When LED8 is lit, it indicates that the master reset of all the major ICs is active.

FLAG LEDs (LED3–6)

The FLAG LEDs connect to the processor's FLAG pins (FLAG2 and FLAG3). These LEDs are active "high" and are lit by an output of "1" from the processor. Refer to "Programmable FLAG Pins" on page 1-9 for information on how to utilize the FLAGs when programming the processor. Table 2-18 shows the FLAG signals and the corresponding LEDs.

Table 2-18. FLAG LEDs

FLAG Pin	LED Reference Designator	FLAG Pin	LED Reference Designator
FLAG2_A	LED4	FLAG2_B	LED5
FLAG3_A	LED6	FLAG3_B	LED3

USB Monitor LED (LED9)

The USB monitor LED indicates that USB communication has been initialized successfully, allowing you to connect to the processor using VisualDSP++. If LED9 is not lit, try resetting the board and/or reinstalling the USB driver (see "Installing EZ-KIT Lite USB Driver" on page 1-7).

When VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Programmable FLAG Push Buttons (SW6–9)

Four push buttons are provided for general-purpose user input. The SW6, SW7, SW8, and SW9 push buttons connect to the processor's programmable FLAG pins. The push buttons are active "high" and when pressed, send a high (1) to the processor. Refer to "Programmable FLAG Pins" on page 1-9 for more information on how to use the FLAGs. Table 2-19 shows the FLAG signals and the corresponding switches.

Table 2-19. FLAG Push Buttons

FLAG Pin	Push Button Reference Designator
FLAG0_A	SW9
FLAG1_A	SW8
FLAG0_B	SW6
FLAG1_B	SW7

Interrupt Push Buttons (SW4–5)

Two push buttons, SW4 and SW5, are provided for user interrupts. The push buttons connect to the processor's interrupt pins. The push buttons are active "low" and, when pressed, send a low (0) to the processor. Refer to "Interrupt Pins" on page 1-10 for more information on how to use the interrupts. Table 2-20 shows the interrupt signals and the corresponding switches.

Table 2-20. Interrupt Push Buttons

Interrupt Pin	Push Button Reference Designator
IRQ0_A	SW4
IRQ0_B	SW5

Reset Push Button (SW3)

The RESET push button, SW3, resets all the ICs on the board, except the USB interface after it has been configured.

Connectors

This section describes the connector functionality and provides information about mating connectors. The locations of the connectors are shown in Figure 2-5.

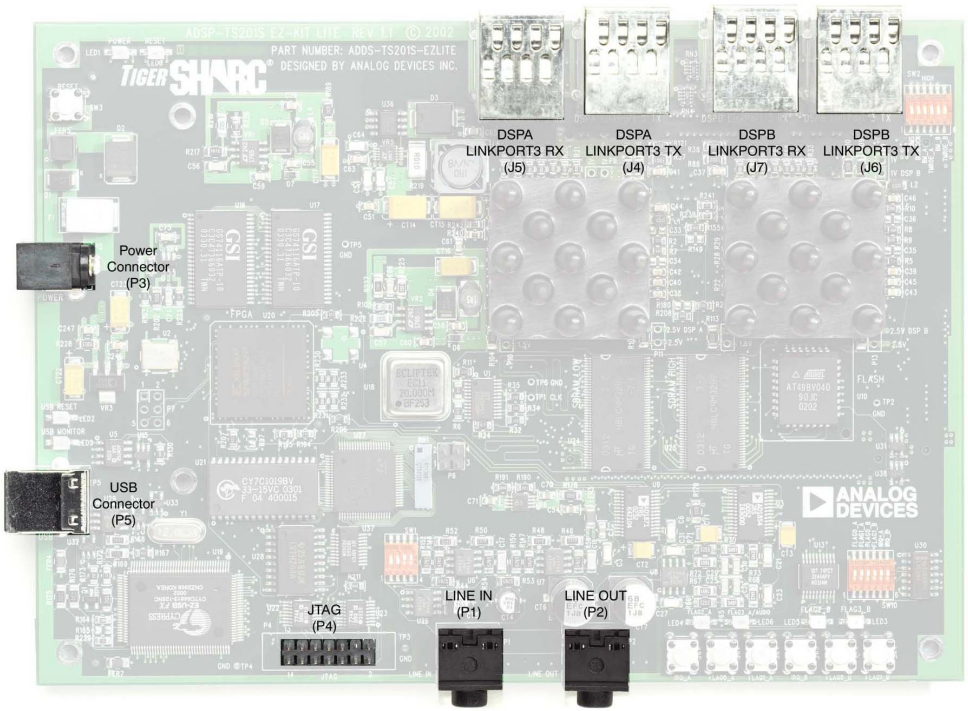


Figure 2-5. Connector Locations

Audio (P1–2)

There are two 3.5 mm stereo audio jacks.

Part Description	Manufacturer	Part Number
3.5 mm stereo jack	Shogyo	SJ-0359AM-5
Mating Connector		
3.5 mm stereo plug to 3.5 mm stereo cable	Radio Shack	L12-2397A

Power (P3)

The power connector provides all the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm Power Jack (P3)	SWITCHCRAFT	RAPC712
	Digi-Key	SC1152-ND
Mating Power Supply (shipped with the EZ-KIT Lite)		
7.5V Power Supply	GlobTek	TR9CC2000LCP-Y

JTAG (P4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. For more information about designing JTAG into a custom board or to learn more about the JTAG interface, please refer to *EE-68* found at Analog Devices website.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

USB (P5)

The USB connector is a standard Type B USB receptacle.

Part Description	Manufacturer	Part Number
Type B USB receptacle	Mill-Max	897-30-004-90-000
	Digi-Key	ED90003-ND
Mating Connector		
USB cable (provided with the kit)	Assman	AK672/2-3
	Digi-Key	AE1302-ND

Expansion Interface (J1–3)

Three board-to-board connectors provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see "Expansion Interface" on page 2-3.

Part Description	Manufacturer	Part Number
90 Position 0.05" Spacing	Samtec	SFC-145-T2-F-D-A
Mating Connector		
90 Position 0.05” Spacing (Through Hole)	Samtec	TFM-145-x1 Series
90 Position 0.05” Spacing (Surface Mount)	Samtec	TFM-145-x2 Series
90 Position 0.05” Spacing (Low Cost)	Samtec	TFC-145 Series

Link Ports (J4–7)

There are four RJ-45 connectors on the EZ-KIT Lite. Two connectors are used for Link Port 3 of Processor A and two are used for Link Port 3 of Processor B.

Part Description	Manufacturer	Part Number
8-Pin RJ-45 Connector	TYCO	1-1609214-1
Mating Cables		
BLK CAT 5E Cable (1 Foot)	E-FILLIATE	119-5136
Gray CAT 5E Cable (1 Meter)	Digi-Key	AE1233-ND

Specifications

This section provides the requirements for powering the board.

Power Supply

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-21 shows the power connector pinout.

Table 2-21. Power Connectors

Terminal	Connection
Center pin	+7.5 VDC@2amps
Outer Ring	GND

A BILL OF MATERIALS

The bill of materials corresponds to the board schematics on page B-1. Please check the latest schematics on the Analog Devices website, http://www.analog.com/Processors/Processors/DevelopmentTools/technicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals.

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
1	1	3.3V-OCTAL-BUFFER	U28	TI	SN74LVT244BDW
2	2	HEX-INVER-SCHMITT-TRIGGER	U14, U30	TI	74LVC14AD
3	1	3.3V-OCTAL-BUFFER	U13	IDT	IDT74FCT3244APY
4	1	ADJ 200MA REGULATOR	VR4	ANALOG DEVICES	ADP3331ART
5	3	SINGLE-2-INPUT-NAND	U15, U31, U38	TI	SN74AHC1G00DBVR
6	1	12.288MHz SMT OSCILLATOR	U2	DIGIKEY	SG-8002CA-PCC-ND
7	2	ADJUSTABLE-3A-SWITCH-REG	VR1–2	LINEAR TECH	LT1765ES8
8	1	P-CHANNEL-MOSFET	U35	FAIRCHILD SEMI	FDS6375
9	1	ADJ-7A-SWITCH-REG-CNTRLR	VR5	LINEAR TECH	LTC1773EMS
10	1	N-CHANNEL-MOSFET	U36	VISHAY	SI9804DY
11	2	4MX32-SDRAM-166MHZ	U24–25	MICRON	MT48LC4M32B2TG–7
12	1	3.3V CLK GENERATOR	U1	IDT	IDT5V928PGI
13	1	3.3V 1:5 CLK DRIVER	U37	IDT	IDT49FCT3805AQ
14	1	512K-X-8-BIT-FLASH-3.3V	U10	ATMEL	AT49BV040-90JC

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
15	2	1000pF 50V 5%	C47–48	AVX	12065A102JAT2A
16	4	2200pF 50V 5%	C22, C24, C56–57	AVX	12065A222JAT050
17	1	0.1uF 50V 20%	C5	AVX	12065E104MAT2A
18	1	VOLTAGE-SUPERVISOR	U5	ANALOG DEVICES	ADM708SAR
19	1	3.3V 1.5A REGULATOR	VR3	ANALOG DEVICES	ADP3339AKC-3.3-RL
20	4	DUAL AUDIO OP AMP	U6–8, U26	NATIONAL	LMV722M
21	1	STERO-DAC	U3	ANALOG DEVICES	AD1854JRS
22	1	STERO-DAC	U9	ANALOG DEVICES	AD1871YRS
23	1	ADJ 500MA REGULATOR	VR6	ANALOG DEVICES	ADP3336ARM-REEL
24	2	TigerSHARC ADSP-TS201S Processor	U11–12	ANALOG DEVICES	ADSP-TS201SABP-ENG
25	4	RUBBER FEET BLACK	MH1–2, MH4–5	MOUSER	517-SJ-5018BK
26	1	PWR 2.5MM_JACK	P3	SWITCH-CRAFT	SC1152-ND12

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
27	7	SPST-MOMENTARY 6MM	SW3–9	PANASONIC	EVQ-PAD04M
28	3	0.05 45X2 SMT	J1–3	SAMTEC	SFC-145-T2-F-D-A
29	2	DIP6	SW2, SW10	DIGIKEY	CKN1364-ND
30	4	RJ45 8PIN RIGHT ANGLE	J4–7	TYCO	1-1609214-1
31	1	4 PIN SMT SWITCH	SW1	DIGIKEY	CKN1363-ND
32	12	0.00 1/8W 5%	R76, R91, R104, R107, R109–110, R113, R118, R178–179, R189, R202	YAGEO	0.0ECT-ND
33	4	AMBER-SMT	LED3–6,	PANASONIC	LN1461C-TR
34	2	330pF 50V 5% NPO	C25, C30	AVX	08055A331JAT
35	4	0.01uF 100V 10% CERM	C1–2, C7–8	AVX	08051C103KAT2A
36	15	0.1uF 50V 10% CERM	C4, C51, C63, C66, C142–143, C145–149, C247–249	AVX	08055C104KAT
37	4	0.001uF 50V 5% NPO	C10–11, C13–14	AVX	08055A102JAT2A
38	2	10uF 16V 10% TANT	CT22–23	SPRAGUE	293D106X9016C2T

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
39	39	10K 100MW 5%	R3, R26, R39–42, R77, R86–87, R89, R92, R94, R100, R102, R108, R112, R116, R153, R158–160, R182–183, R187, R194, R195, R203, R213–215, R223–224, R235–236, R238–242	AVX	CR21-103J-T
40	4	4.7K 100MW 5%	R5, R93, R186, R188	AVX	CR21-4701F-T
41	1	10.7K 1/8W 1%	R217	DALE	CRCW1206-1072FRT1
42	1	10.5K 1/8W 1%	R227	BECKMAN	BCR1/81052FT
43	6	2.00K 1/8W 1%	R37–38,R88, R121, R156–157	DALE	CR32-2001F-T
44	2	49.9K 1/8W 1%	R60, R63	AVX	CR32-4992F-T
45	12	100pF 100V 5% NPO	C3, C6, C9, C12, C15, C20–21, C23, C27, C31, C52–53	AVX	12061A101JAT2A
46	3	10uF 16V 10% TANT	CT1–3	AVX	TAJB106K016R
47	1	3A SCHOT_RECT	D2	MICRO-SEMI	HSM350J

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
48	6	100 100MW 5%	R78, R85, R95, R99, R101, R103	AVX	CR21-101J-T
49	3	220pf 50V 10% NPO	C28, C32, C62	AVX	12061A221JAT2A
50	1	2A SILICON RECTIFIER	D1	GENERALSEMI	S2A
51	5	600 100MHZ 500MA FERRITE BEAD	FER1–3, FER6–7	DIGIKEY	240-1019-1-ND
52	4	237 1/8W 1%	R46, R48, R50, R52	AVX	CR32-2370F-T
53	2	750K 1/8W 1%	R47, R49	DALE-VISHAY	CRCW12067503FRT1
54	8	5.76K 1/8W 1%	R44,R53–57, R150, R152	PHYCOMP	9C12063A5761FKHFT
55	2	11.0K 1/8W 1%	R61–62	DALE	CRCW12061102FRT1
56	4	120PF 50V 5% NPO	C16–19	PHILLIPS	1206CG121J9B200
57	4	1UF 16V 10% X7R	C54, C70–72	MURATA	GRM40X7R105K016AL
58	1	47PF 100V 10%	C64	KEMET	C1206C470K1GACTU
60	1	340K 1/8W 1%	R192	DALE	CRCW0805-3403FT
61	1	698K 1/8W 1%	R201	DALE	CRCW0805-6983FT
62	2	680PF 50V 1% NPO	C26, C29	AVX	08055A681FAT2A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
63	2	2.74K 1/8W 1%	R68, R73	DALE	CRCW12062741FRT1
64	4	5.49K 1/8W 1%	R64–65, R69–70	PANASONIC	ERJ-8ENF5491V
65	2	3.32K 1/8W 1%	R66, R71	DALE	CRCW12063321FRT1
66	2	1.65K 1/8W 1%	R67, R72	PANASONIC	ERJ-8ENF1651V
67	2	10UF 16V 20% ELEC	CT4–5	DIG01	PCE3062TR-ND
68	2	68UF 25V 20% ELEC	CT6–7	PANASONIC	EEV-FC1E680P
69	2	2A SL22 SCHOTTKY	D4, D5	GENERAL SEMI	SL22
70	1	332K 1/10W 1%	R234	PHILIPS	9C08052A3323FKRT/R
71	18	0.00 100MW 5%	R1–2, R7–10, R130, R155, R161, R181, R184–185, R208–212, R226	VISHAY	CRCW0805 0.0 RT1
72	1	190 100MHZ 5A FERRITE BEAD	FER5	MURATA	DLW5BSN191SQ2
73	1	35.7K 1/10W 1%	R220	YAGEO	9C08052A3572FKHFT
74	2	10UH X 10%	L1–2	PANASONIC	ELJ-FC100KF

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
75	11	22 1/10W 5%	R4, R6, R11, R24, R32, R34–35,R129, R205–207	VISHAY/DALE	CRCW0805220JRT1
76	2	0.47UF 16V 10%	C73–74	AVX	0805YC474KAT2A
77	4	1UF 10V 10%	C37, C41, C44, C46	AVX	0805ZC105KAT2A
78	6	1000PF 10V 20%	C38–40, C42–43, C45	YAGEO	1206CG229C9B200
79	3	4.7UF 6.3V 10%	C61, C65, C76	AVX	08056D475KAT2A
80	53	0.1UF 10V 10%	C69, C75,C79–84, C155–162, C108,C110–115,C118, C120–122, C141, C144,C165–166, C182,C184–185, C187,C197–201, C221–225, C228–231, C237–239, C241	AVX	0402ZD104KAT2A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
81	46	0.01UF 16V 10%	C68,C85–90,C92–99, C103–104, 107, C109, C129–140,C167, C181,C183,C202–205, C216,C218–220,C227, C232,C240, C242	AVX	0402YC103KAT2A
82	2	4.7K 31MW 5%	RN3–4	CTS	746X101472J
83	16	499 1/10W 1%	R23, R25,R45, R51,R111, R114,R124, R133,R140–146,R154	VISHAY	CRCW080549900FRT1
84	1	1UH 5.9MOHMS 30%	L6	DIGIKEY	919AS-1RON=P3-ND
85	2	1.5UH 45MOHM 20%	L4–5	TYCO	DS6630-1R5M
86	1	0.01 1.5W 5%	R219	IRC	LR2512-01-R010-F
87	1	2.55K 1/10W 1%	R105	VISHAY	CRCW080522551FRT1
88	1	30K 1/10W 5%	R218	VISHAY	CRCW0805303JRT1
89	1	80.6K 1/10W 1%	R221	VISHAY	CRCW080580062FRT1
90	2	SUPERMINI SCHOTTKY	D6–7	CENTRAL SEMI	CMDSH-3
91	1	3A MBRS340T3	D3	ON SEMI	MBRS340T3

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
92	1	680uF 6.3V 10% TANT-LOW-ESR	CT15	AVX	TPSE687K006R0045
93	2	0.18uF 25V 10% CERM	C55, C58	AVX	08053C184KAT2A
94	2	100uF 10V 10% TANT-LOW-ESR	CT16–17	AVX	TPSC107K010R0075
95	1	150uF 10V 10% TANT-LOW-ESR	CT14	KEMET	T494D157K010AS
96	2	2.2uF 10V 10% CERM	C59–60	AVX	0805ZD225KAT2A
97	44	1000PF 50V 5% CERM	C67, C168–180, C186,C188–196, C206–215, C217, C226,C233–236, C243–246	AVX	04025C102JAT2A
98	1	64.9K 1/10W 1%	R191	VISHAY	CRCW08056492FRT1
99	2	57.6K 1/4W 1%	R147–148	VISHAY	CRCW12065762FRT1
100	1	210K 1/4W 1%	R190	VISHAY	CRCW08052103FRT1
101	22	100 1/10W 1%	R13, R15–22, R27, R29, R31, R33, R36, R43, R83, R96,R98, R230–233	VISHAY	CRCW08051000FRT1
102	3	100K 1/8W 5%	R58–59, R228	AVX	CR1206-1003FRT1

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
103	7	270 1/8W 5%	R79–82, R84, R90, R151	AVX	CR32-271J-T
104	1	20MHZ 1/2	U18	ECLIPTEK	EC1100HS-20.000M
105	2	10.0K 1/8W 1%	R216, R222	DALE	CRCW1206-1002FRT1
106	1	13.0K 1/8W 1%	R225	PANASONIC	ERJ-8ENF1302V
107	2	RED-SMT GULL-WING	LED2,LED8	PANASONIC	LN1261C
108	1	GREEN-SMT GULL-WING	LED1	PANASONIC	LN1361C
109	2	604 1/8W 1%	R74–75	DALE	CRCW12066040FRT1
110	6	1uF 25V 20% TANT	CT8–13	PANASONIC	ECS-T1EY105R
111	2	QUICKSWITCH-257	U22–23	ANALOG DEVICES	ADG774ABRQ
112	1	IDC 7X2	P4	BERG	54102-T08-07
113	1	2.5A RESETABLE	F1	RAYCHEM	SMD250-2
114	2	3.5MM STEREO_JACK	P1–2	A/D ELEC.	ST-323-5
115	5	10uF 6.3V 10% TANT	C91, C100, C154, C163, C164	AVX	08056D106KAT2A

ADSP-TS201S EZ-KIT Lite

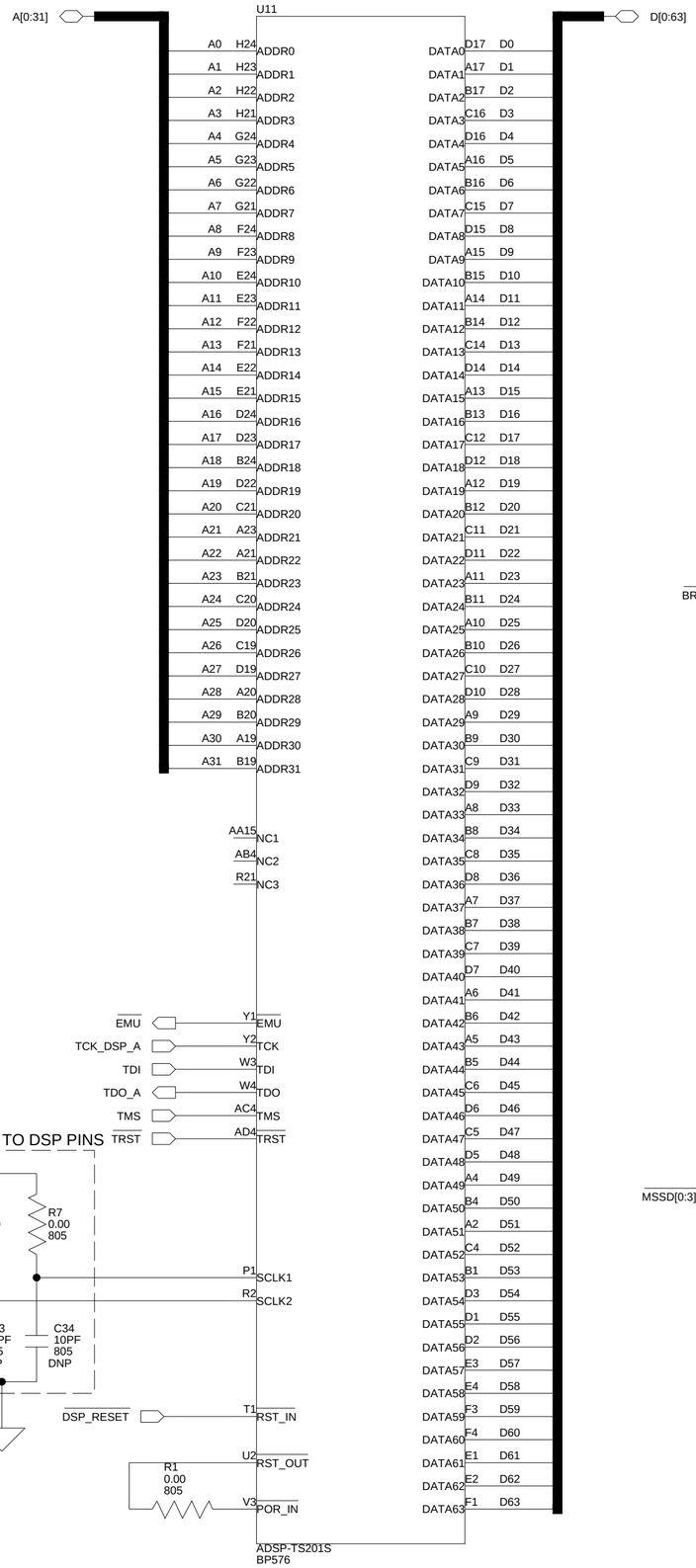
Approvals	Date
Drawn	
Checked	
Engineering	

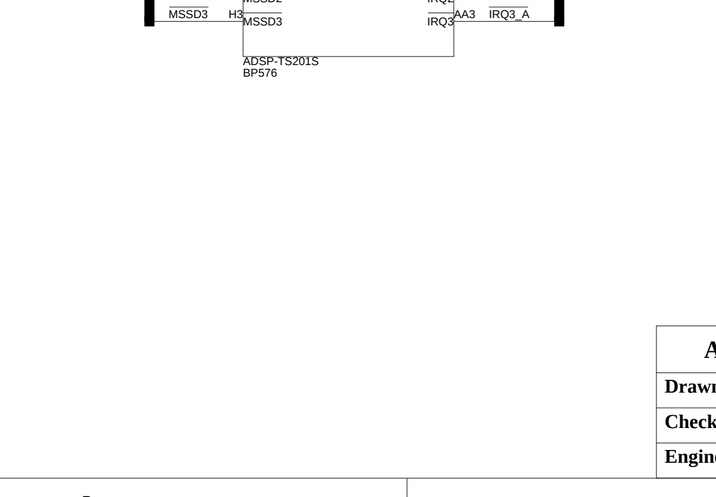
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

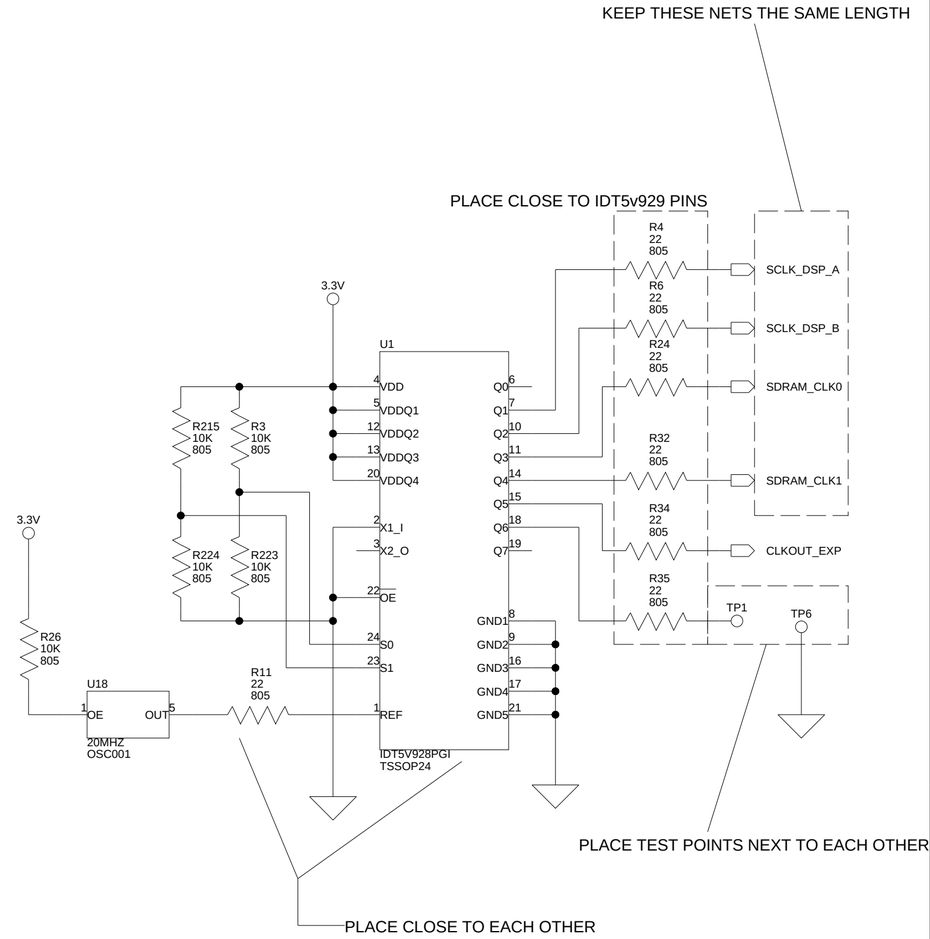
Title	ADSP-TS201S EZ-KIT LITE - TITLE		
Size C	Board No. A0178-2002		Rev 1.1C
Date 3-1-2004_10:59		Sheet 1 of 15	

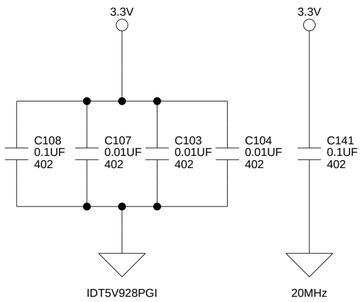
DSP A

LABEL "DSP A" near this DSP









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Engineering	

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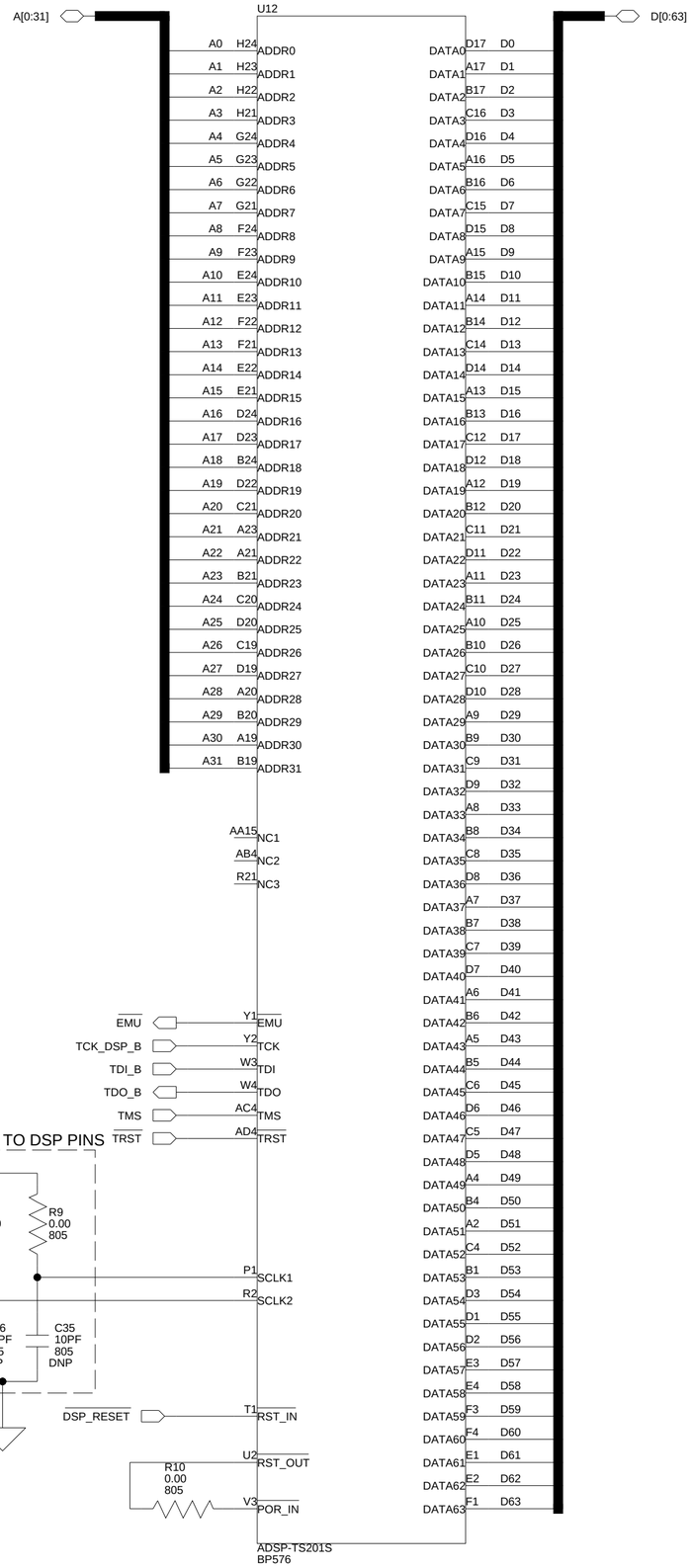
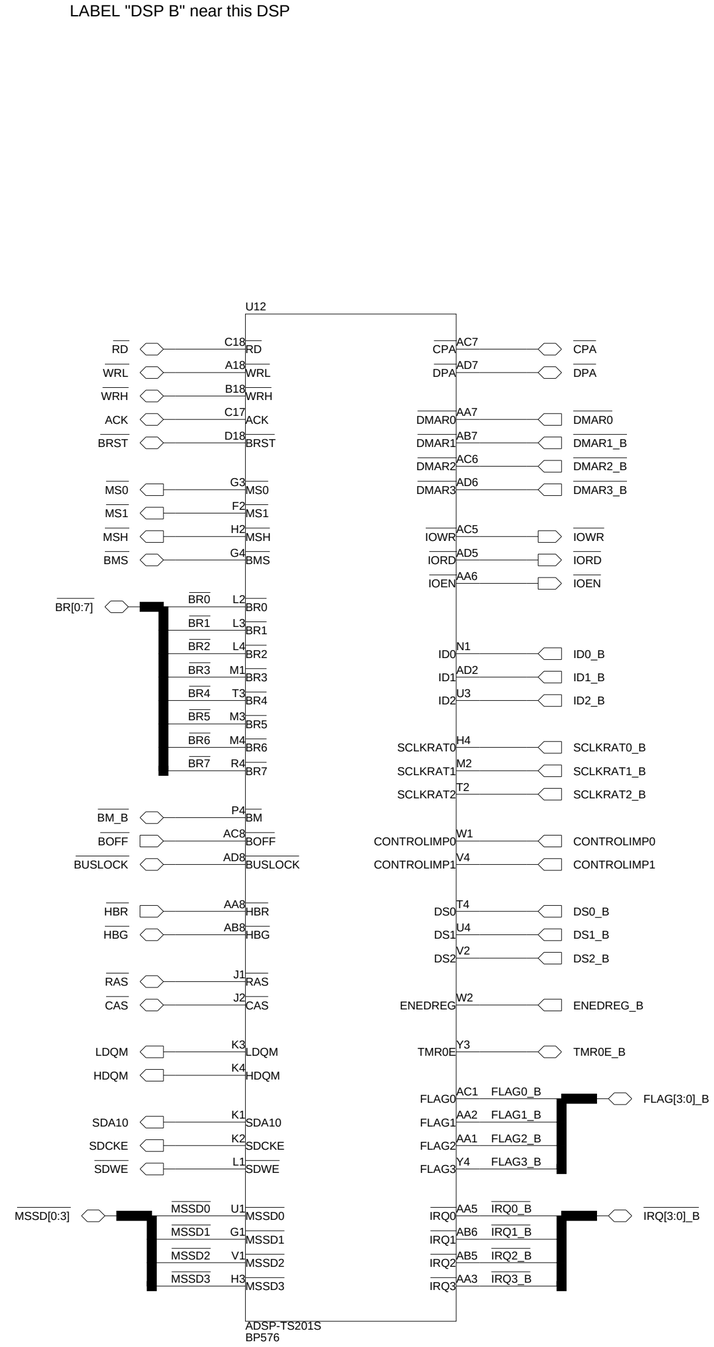
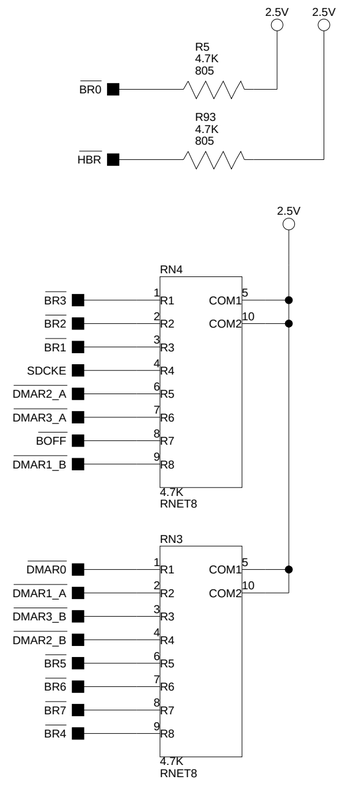
Title	ADSP-TS201S EZ-KIT LITE - DSP A		
Size C	Board No. A0178-2002		Rev 1.1C
Date 3-1-2004_10:59		Sheet 2 of 15	

DSP B

LABEL "DSP B" near this DSP







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Engineering	

ANALOG DEVICES
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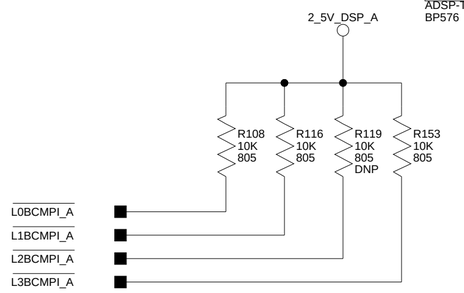
Title	ADSP-TS201S EZ-KIT LITE - DSP B		
Size C	Board No. A0178-2002		Rev 1.1C
Date 3-1-2004_10:59		Sheet 3 of 15	

ALL NETS ON THIS PAGE EXCEPT L?ACK?_? and L?BCMP?_? ARE DIFFERETIAL PAIRS
THESE SIGNAL SHOULD BE ROUTING ACCORDING THE GUIDELINES SET IN EE-179

	DSP A	DSP B
Link Port 0	FPGA	FPGA
Link Port 1	EXP INT	EXP INT
Link Port 2	DSP B	DSP A
Link Port 3	RJ45	RJ45

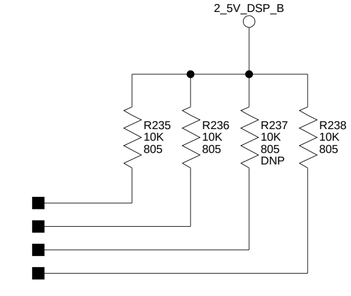
DSP A

PLACE CLOSE TO DSP A PINS (CRITICAL)



DSP B

PLACE CLOSE TO DSP B PINS (CRITICAL)



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Engineering	

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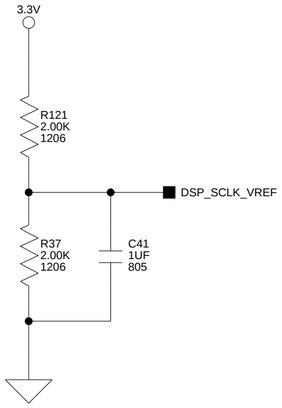
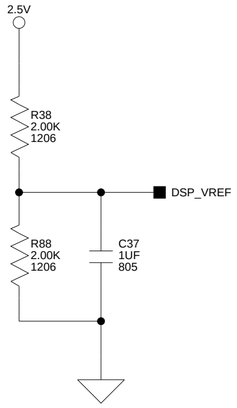
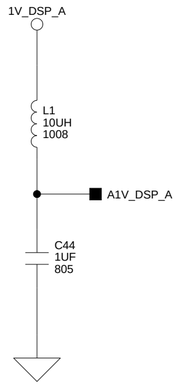
Title: ADSP-TS201S EZ-KIT LITE - DSP LINK PORTS

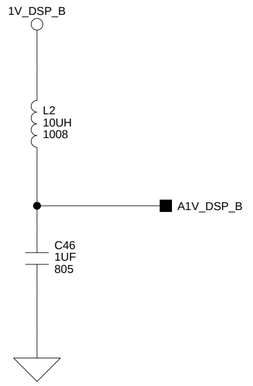
Size	Board No.	Rev
C	A0178-2002	1.1C

Date: 3-1-2004_10:59 Sheet 4 of 15

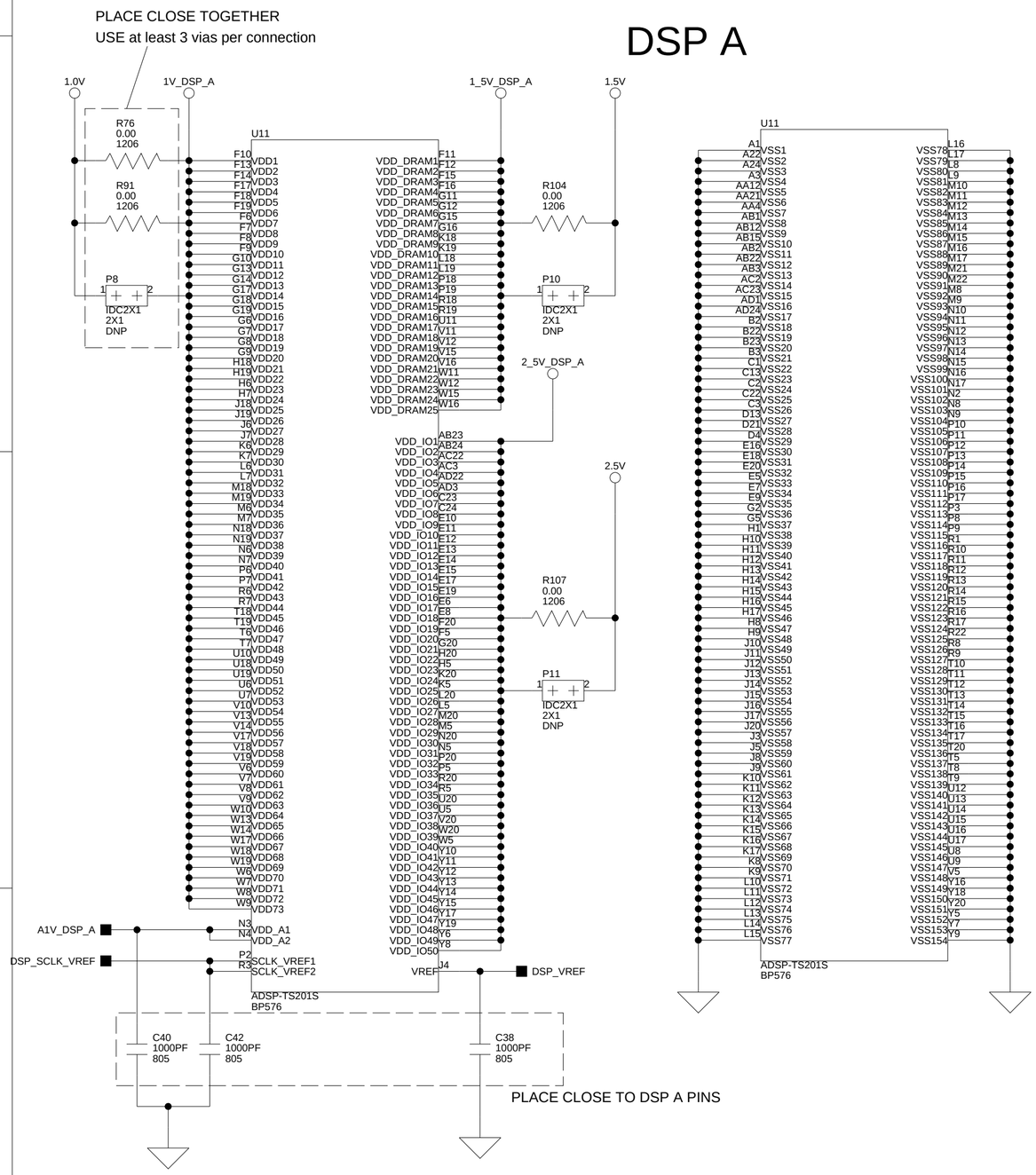




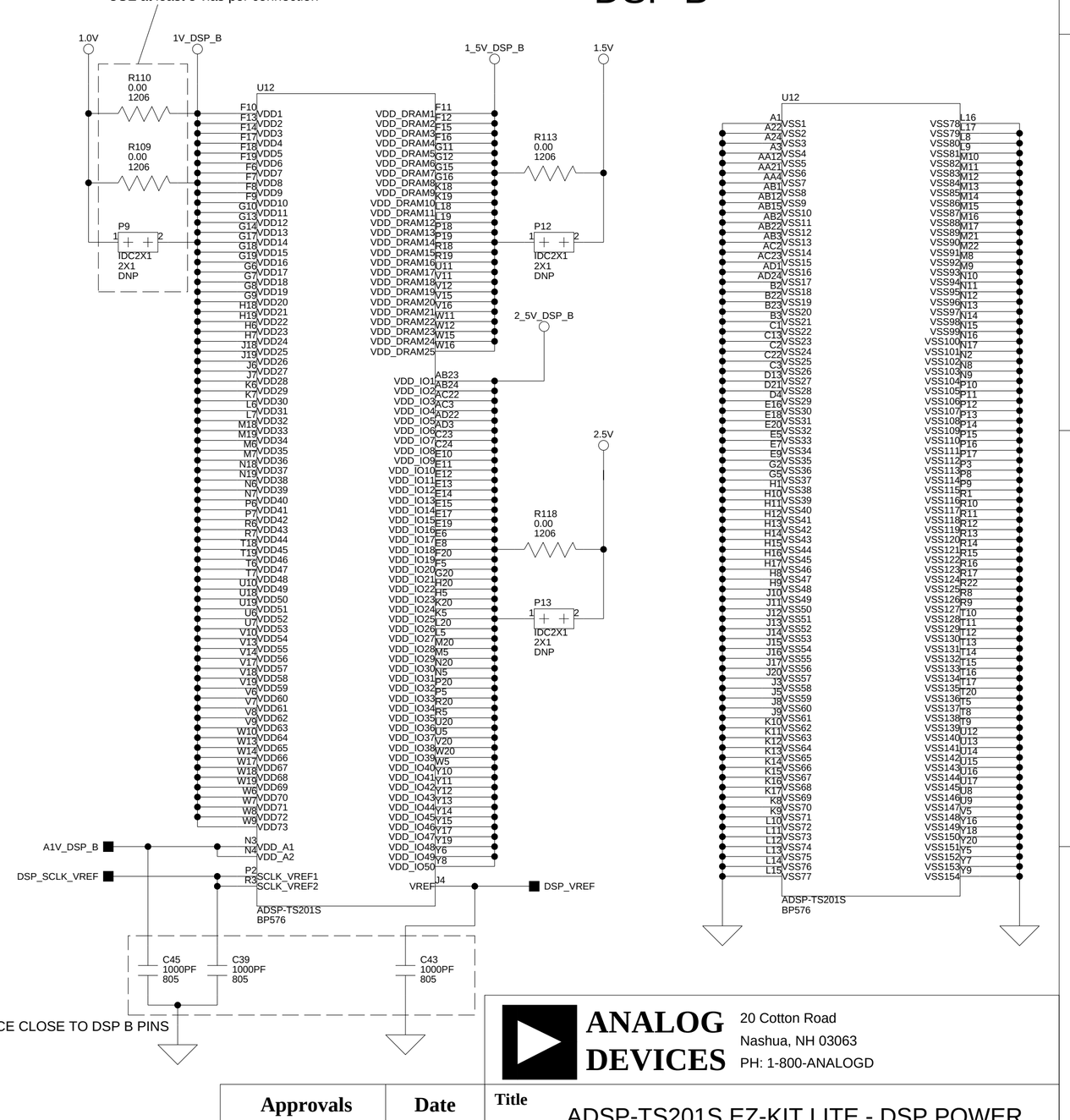




DSP A



DSP B



Approvals	Date
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Checked	
Engineering	

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
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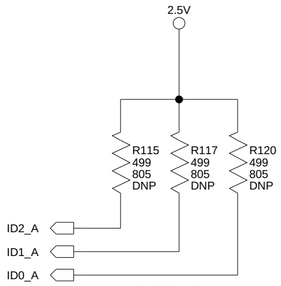
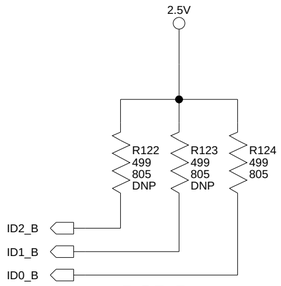
Title: ADSP-TS201S EZ-KIT LITE - DSP POWER		
Size: C	Board No.: A0178-2002	Rev: 1.1C
Date: 3-1-2004_10:59	Sheet: 5 of 15	



DSP A
Default ID = 0

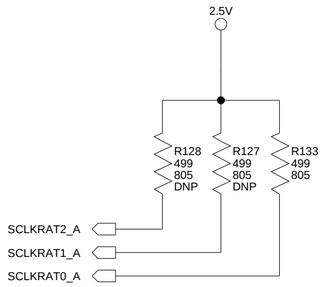


DSP B
Default ID = 1

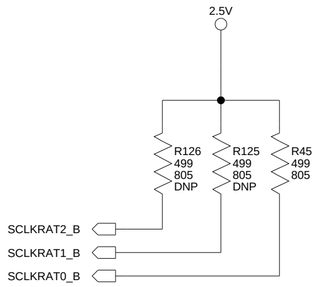
ID[2-0] have internal 5Kohm pull-down resistors

ID(2-0)	Proc ID
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

THESE RESISTORS DO NOT NEED TO BE VERY CLOSE TO THE DSP
IF POSSIBLE I WOULD LIKE THEM ALL ON THE BOTTOM OF THE BOARD
ORGANIZED IN GROUPS SIMILAR TO SHOW HERE
DEPENDING ON HOW MUCH ROOM YOU CAN LEAVE NEAR THEM
I WOULD LIKE TO LABEL SOME OF THEM



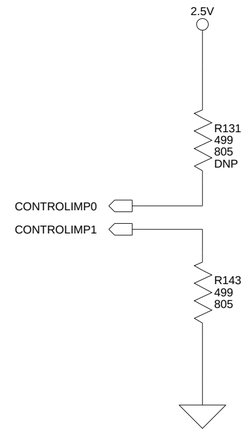
DSP A
Default PLL Ratio = 5X
CCLK = 500MHz



DSP B
Default PLL Ratio = 5X
CCLK = 500MHz

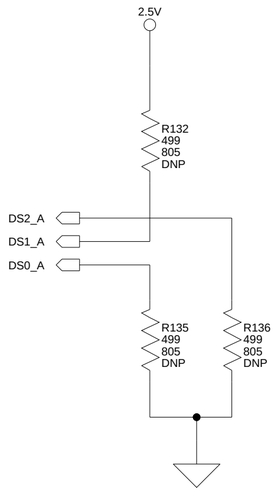
SCLKRAT[2-0] have internal 5Kohm pull-down resistors

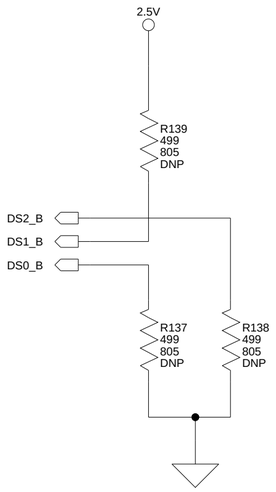
SCLKRAT(2-0)	PLL Ratio
000	4
001	5
010	6
011	7
100	8
101	10
110	12
111	RESERVED



DEFAULT = NORMAL
CONTROLIMP0 has an internal 5Kohm pull-down resistor
CONTROLIMP1 has an internal 5Kohm pull-up resistor

CONTROLIMP(1:0)	Driver Mode
00	Normal
01	Pulse Mode
10	A/D Mode
11	Pulse Mode, A/D Mode

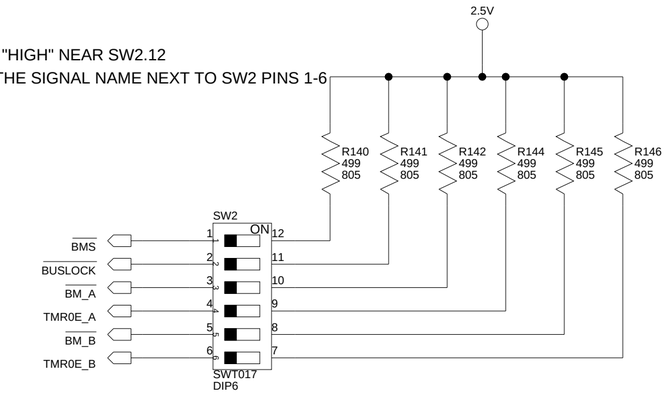




DS1 has internal 5Kohm pull-down resistor
DS2 and DS0 have internal 5Kohm pull-up resistors

DS(2-0)	Drive Strength	OUTPUT IMP	
000	11.1%	26	
001	23.8%	32	
010	36.5%	40	
011	49.2%	50	
100	61.9%	62	
101	74.6%	70	DEFAULT
110	87.3%	96	
111	100%	120	

PLACE A LABEL "HIGH" NEAR SW2.12
PLACE A LABEL FOR THE SIGNAL NAME NEXT TO SW2 PINS 1-6

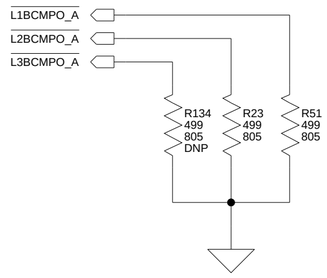


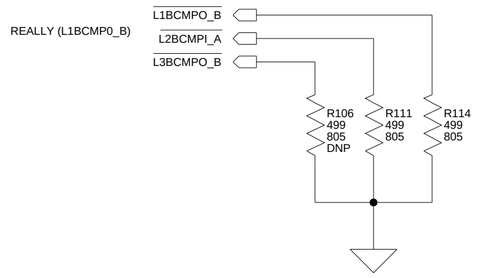
All strap pins have internal 5Kohm pull-down resistors during DSP reset

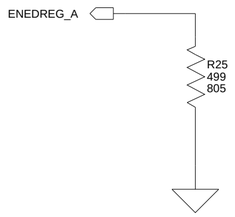
		Switch OFF (Signal Pulled Low)	Switch ON (Signal Pulled High)
BMS	*	EPROM Boot	External or link port boot
BM	*	Disable interupts, level sensitive	Enable interupts, edge sensitive
TMR0E	*	1-bit Link Port Data Width	4-bit Link Port Data Width
BUSLOCK	*	SYSCON/SDRCON one-time writable	SYSCON/SDRCON always writable

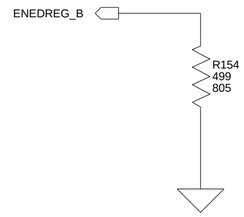
* indicates DEFAULT

KEEP STUB TO THE SIGNAL AS SMALL AS POSSIBLE









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Title: ADSP-TS201S EZ-KIT LITE - CONFIG

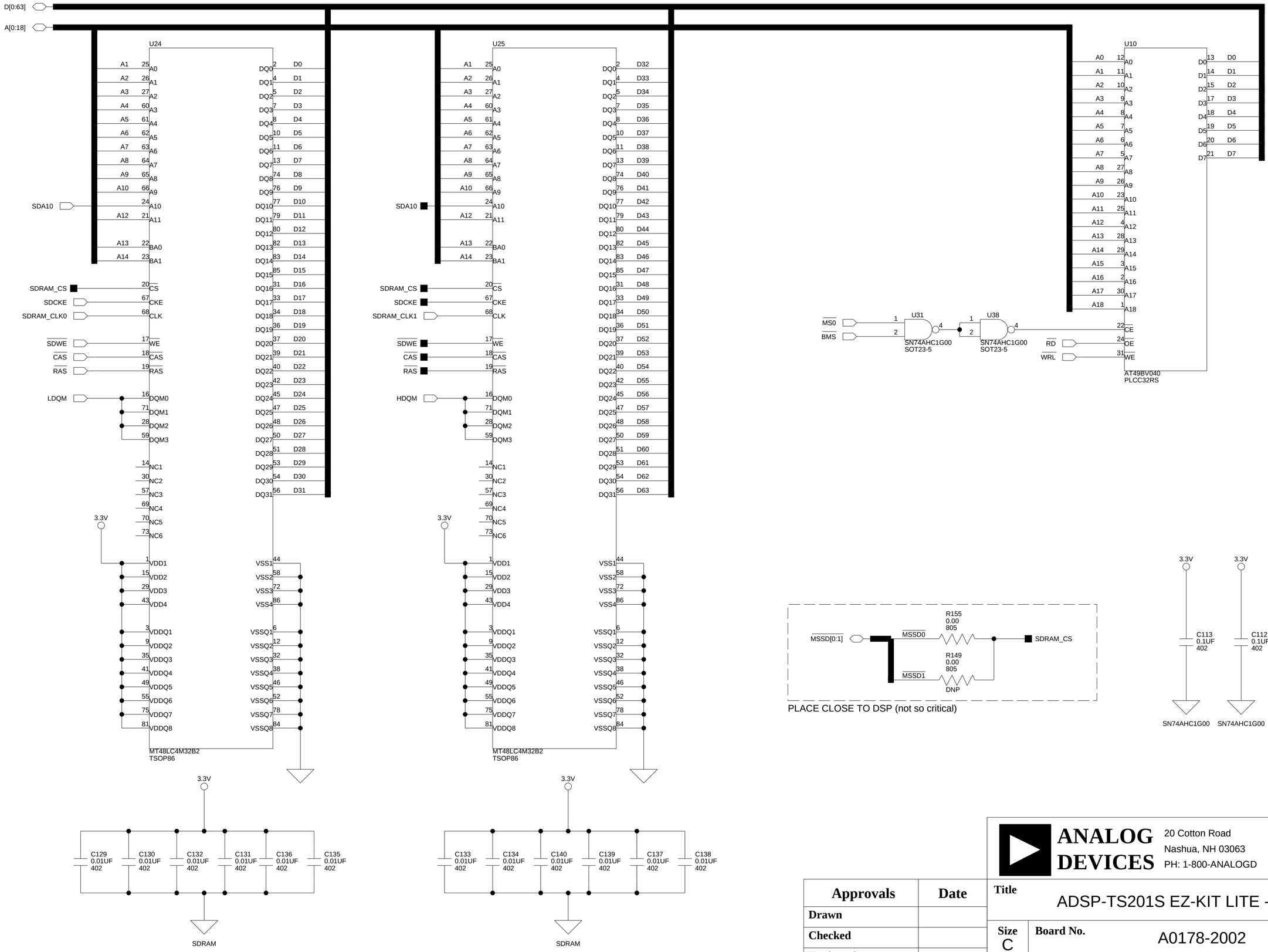
Size	Board No.	Rev
C	A0178-2002	1.1C

Date: 3-4-2004_10:58 Sheet 6 of 15

SDRAM 256Mb
(32MB - 4M x 64bits)

LABEL "SDRAM(LOW)"

LABEL "SDRAM(HIGH)"



FLASH (512Kbx8)

PLACE CLOSE TO DSP (not so critical)

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Title	ADSP-TS201S EZ-KIT LITE - MEMORY		
Size C	Board No. A0178-2002		Rev 1.1C
Date 3-4-2004_11:06		Sheet 7 of 15	

KEEP ALL OF THESE COMPONENTS OVER THE AGND PLANE

TRY TO KEEP ALL TRACES AS SHORT AS POSSIBLE

PLACE NEAR CONNECTOR

FER2 600 1206
R58 100K 1206
C20 100PF 1206
AGND

CT5 10UF CAP002
R44 5.76K 1206
INL-_AMPIN
R148 57.6K 1206
C16 120PF 1206
U6 LMV722M SOIC8
INL-_AMPOUT
R52 237 1206
INL-
C14 0.001UF 805
C12 100PF 1206
C11 0.001UF 805
AGND
INL+
R50 237 1206

LABEL "LINE IN"

P1
CON001 STEREO_JACK
AUDIO_IN_LEFT
LOOPBACK_LEFT
LOOPBACK_RIGHT
AUDIO_IN_RIGHT
AGND

VREF_AUDIO
R55 5.76K 1206
R54 5.76K 1206
C17 120PF 1206
R49 750K 1206
U6 LMV722M SOIC8
AGND

ADC LEFT

ADC

U9 AD1871YRS SSOP28
CAPLN
CAPLP
VINLP
VINLN
VINRP
VINRN
CAPRN
CAPRP
MCLK
RESET
CASC
XCTRL
CCLK/{256~/512}
COUT/{DF0}
CIN/{DF1}
CLATCH/{M~/S}
LRCLK
BCLK
DOUT
DIN
VREF
LRCLK
BCLK
DR
VREF_AUDIO

3.3V
R42 10K 805
R39 10K 805

SLAVE MODE
MCLK IS 256 x Fs
48 kHZ SAMPLE RATE
I S I/F MODE

C4 0.1UF 805
CT2 10UF B
AGND

FER1 600 1206
R59 100K 1206
C15 100PF 1206
AGND
PLACE NEAR CONNECTOR

CT4 10UF CAP002
R53 5.76K 1206
INR-_AMPIN
R147 57.6K 1206
C18 120PF 1206
U7 LMV722M SOIC8
INR-_AMPOUT
R48 237 1206
INR-
C13 0.001UF 805
C9 100PF 1206
C10 0.001UF 805
AGND
INR+
R46 237 1206

R57 5.76K 1206
R56 5.76K 1206
C19 120PF 1206
R47 750K 1206
U7 LMV722M SOIC8
AGND

ADC RIGHT

C3 100PF 1206
C6 100PF 1206
C8 0.01UF 805
C7 0.01UF 805
C2 0.01UF 805
C1 0.01UF 805
KEEP THESE CLOSE TO AD1871
AGND

U26 LMV722M SOIC8
AGND

THE GND AND AGND PLANES SHOULD GO FROM PIN 8 to PIN 21 of U9

R179 0.00 1206
AGND
PLACE RESISTOR BETWEEN AD1871 and AD1854

U26 LMV722M SOIC8
VREF_AUDIO
R157 2.00K 1206
R156 2.00K 1206
R150 5.76K 1206
INR-_AMPIN
R152 5.76K 1206
INL-_AMPIN

WHEN USING AN ELECTRET MICROPHONE
PLACE SW1.1 AND SW1.2 IN ON POSITION
PLACE SW1.3 AND SW1.4 IN OFF POSITION

SW1 SWT018 DIP4
AUDIO_IN_RIGHT
AUDIO_IN_LEFT
INR-_AMPOUT
INL-_AMPOUT

A5V A5V A5V A5V 3.3V 5V
C147 0.1UF 805
C146 0.1UF 805
C145 0.1UF 805
C148 0.1UF 805
C249 0.1UF 805
C149 0.1UF 805
AGND
NEAR U6 NEAR U7 NEAR U26 AD1871 AD1871 AD1871

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Title: ADSP-TS201S EZ-KIT LITE - AUDIO IN

Size	Board No.	Rev
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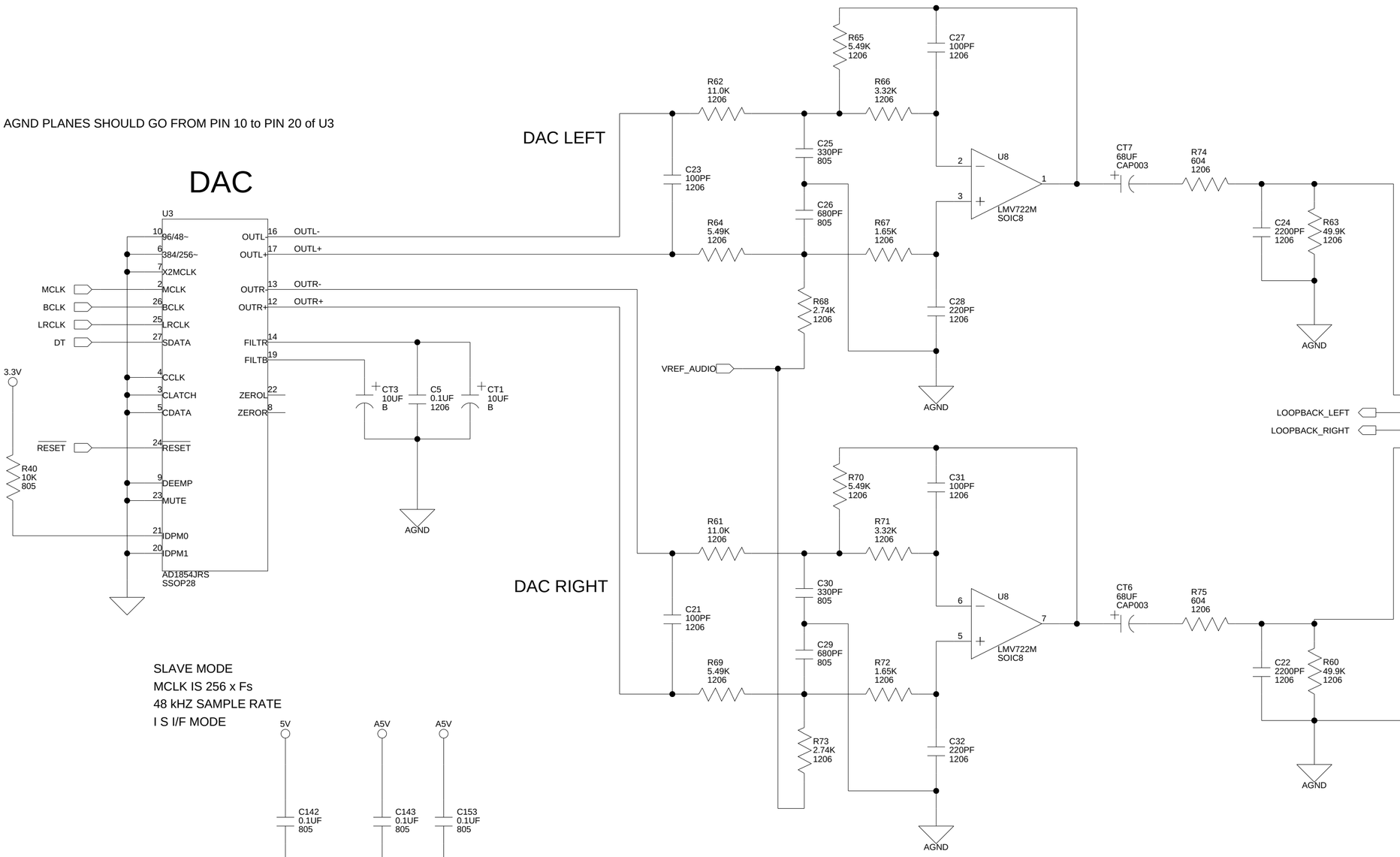
THE GND AND AGND PLANES SHOULD GO FROM PIN 10 to PIN 20 of U3

KEEP ALL OF THESE COMPONENTS OVER THE AGND PLANE

DAC

DAC LEFT



DAC RIGHT

SLAVE MODE
MCLK IS 256 x Fs
48 kHZ SAMPLE RATE
I S I/F MODE

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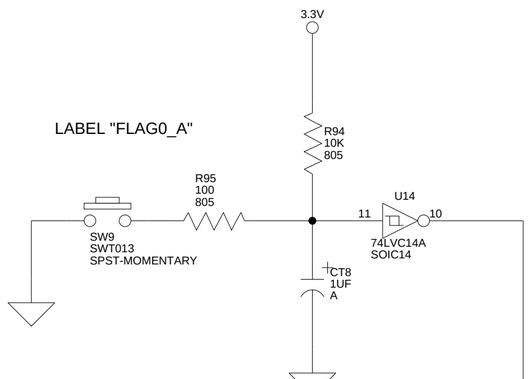
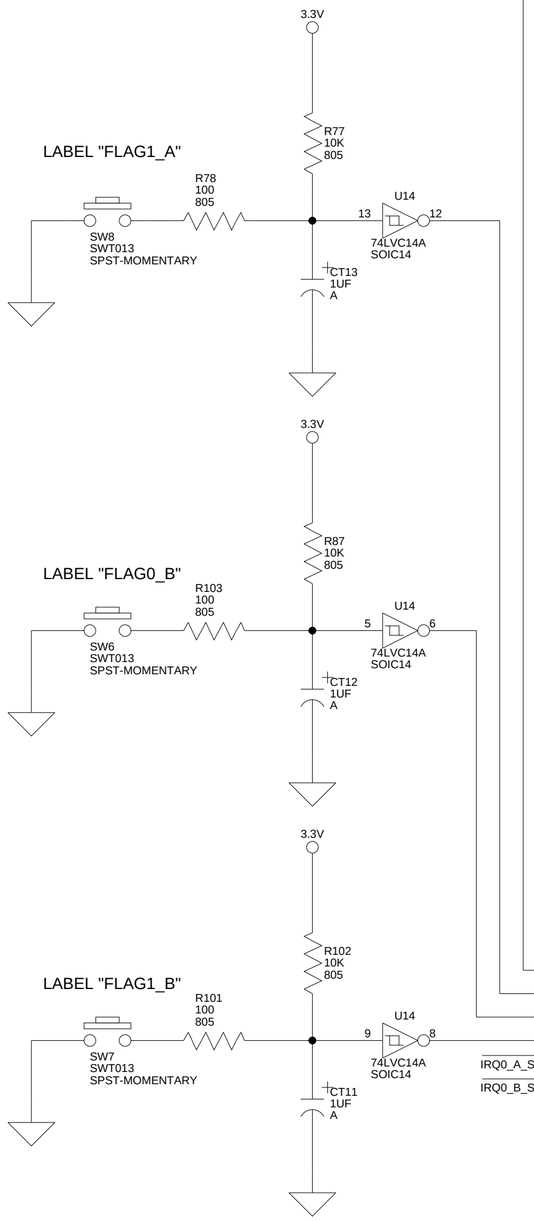
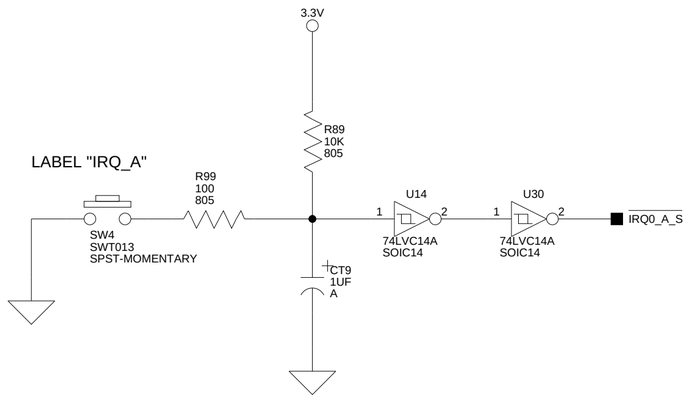
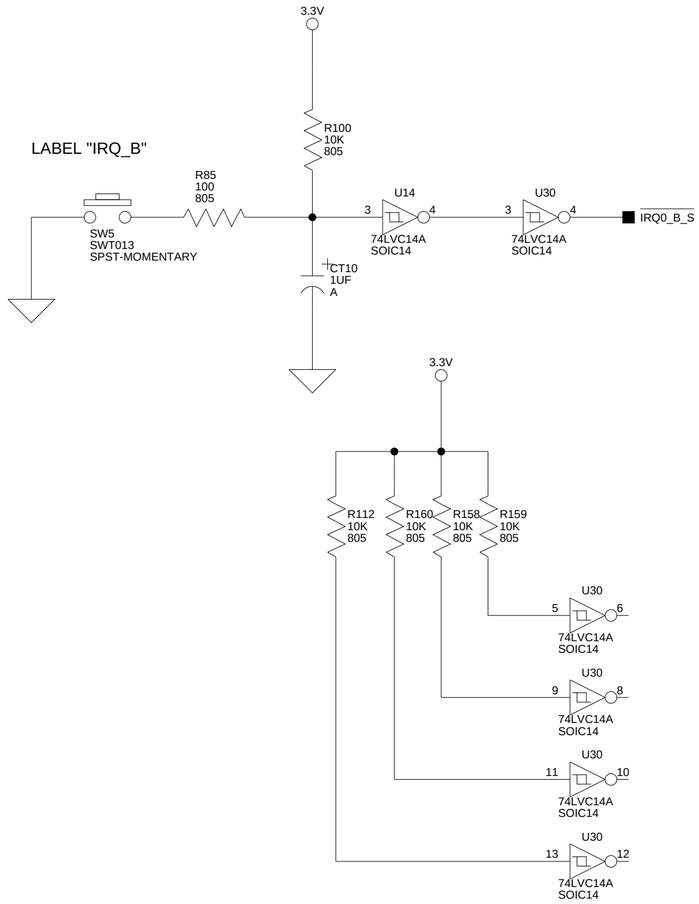
Title	ADSP-TS201S EZ-KIT LITE - AUDIO OUT	
Size C	Board No. A0178-2002	Rev 1.1C
Date 3-1-2004_10:59	Sheet 9 of 15	

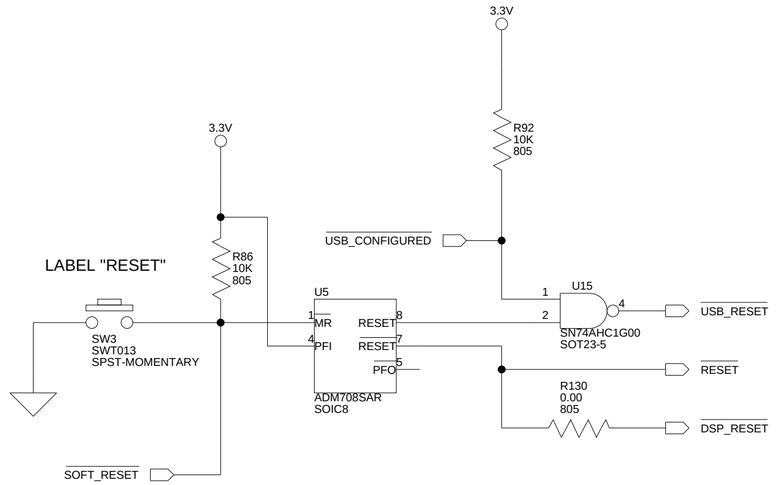


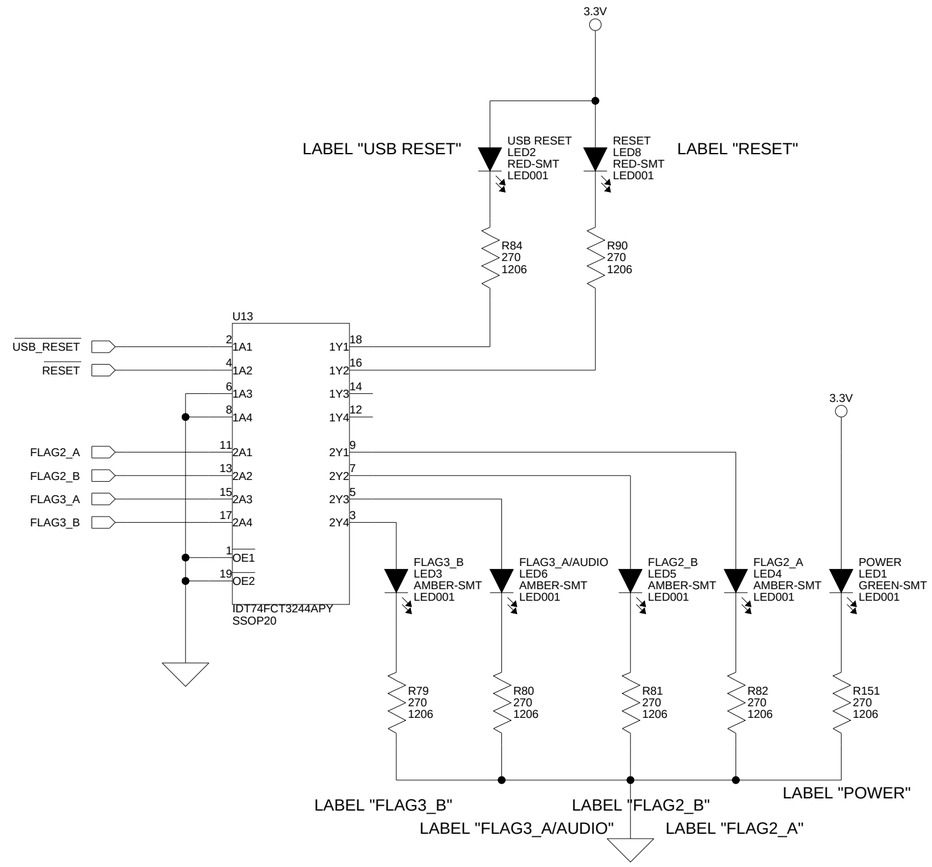


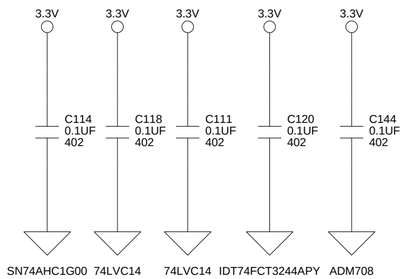
Switch ON = Pushbutton will drive DSP net.
Switch OFF = DSP net can come from an external source
DEFAULT = All Switches ON











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Title: ADSP-TS201S EZ-KIT LITE - RESET/PB/LED

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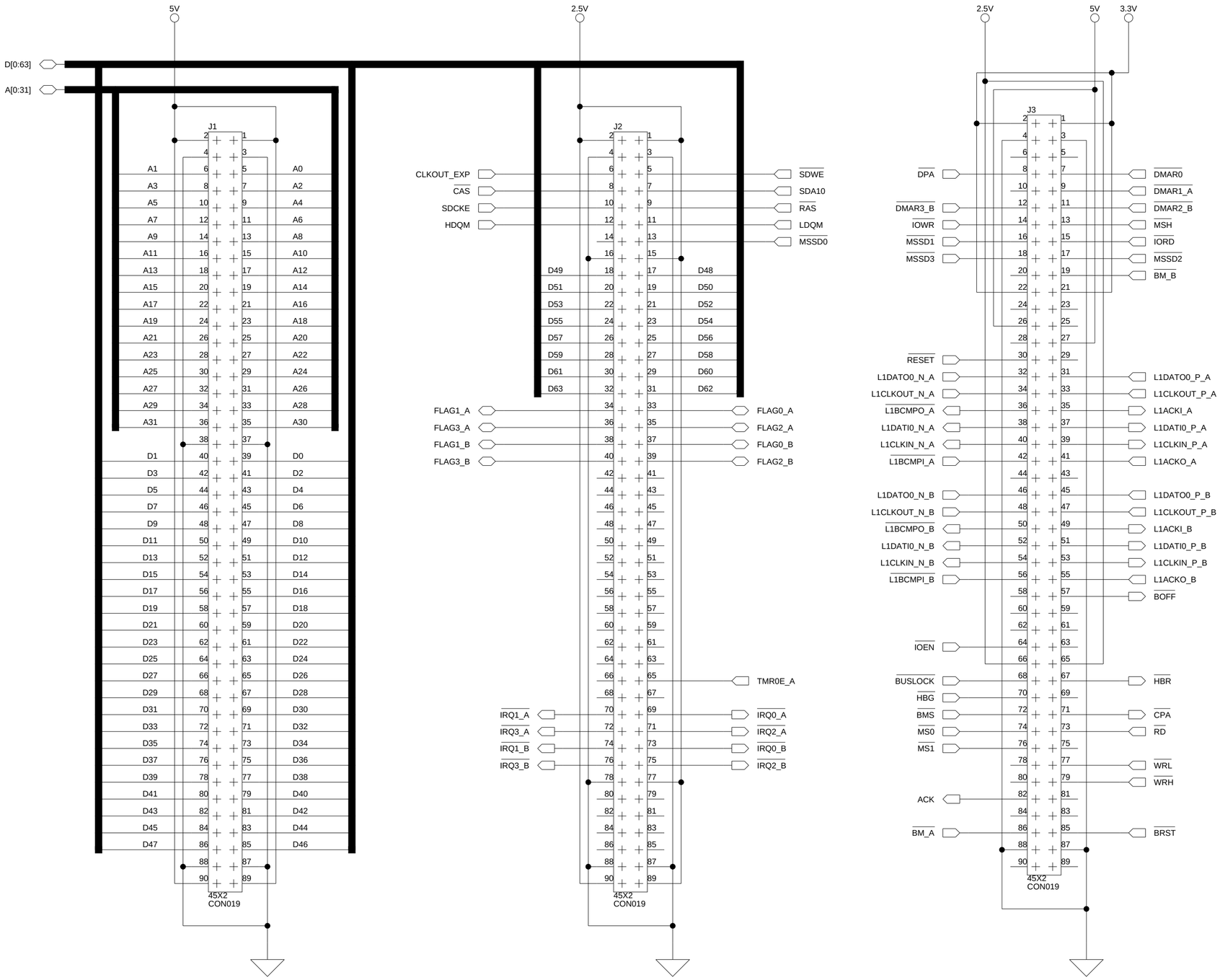
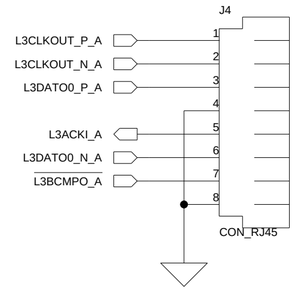
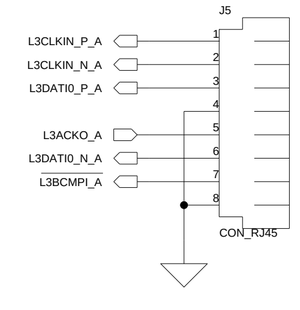
Expansion Interface (TYPE A)

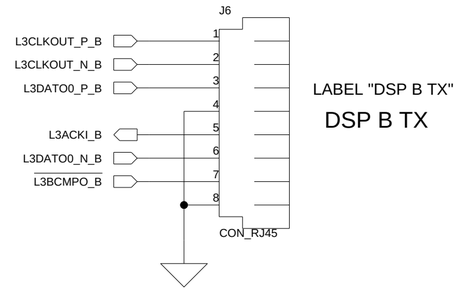
PLACE LABEL "EXPANSION INTERFACE (TYPE A)" NEAR MIDDLE CONNECTOR

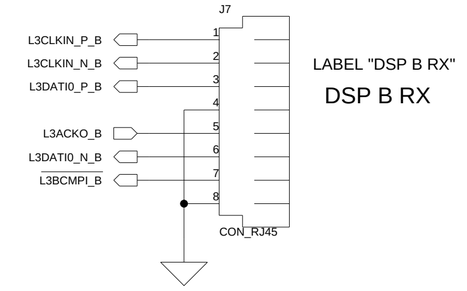


WARNING: WHEN CONNECTING TO ANOTHER BOARD
MAKE SURE TX CONNECTOR GOES TO A RX CONNECTOR
DO NOT USE CROSSOVER CABLE









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Title	ADSP-TS201S EZ-KIT LITE - EXPANSION INT		
Size C	Board No. A0178-2002		Rev 1.1C
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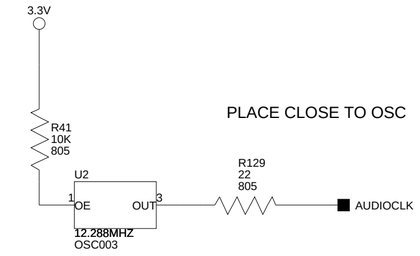
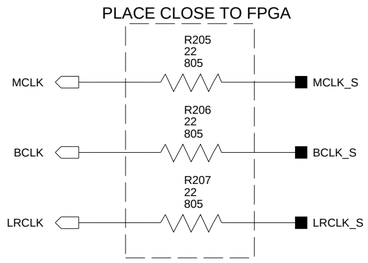
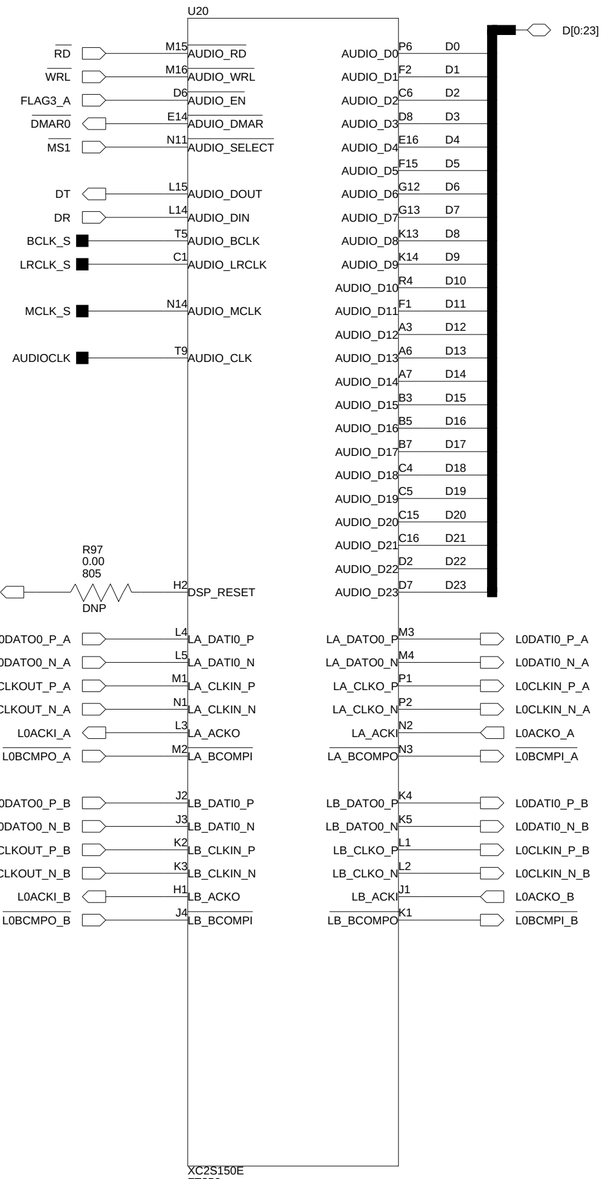


PLACE CLOSE TO OSC



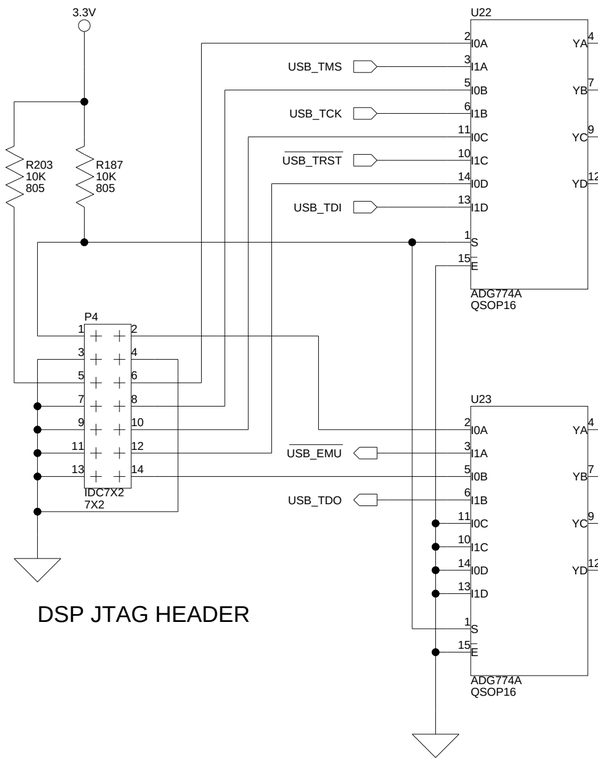
PLACE CLOSE TO FPGA



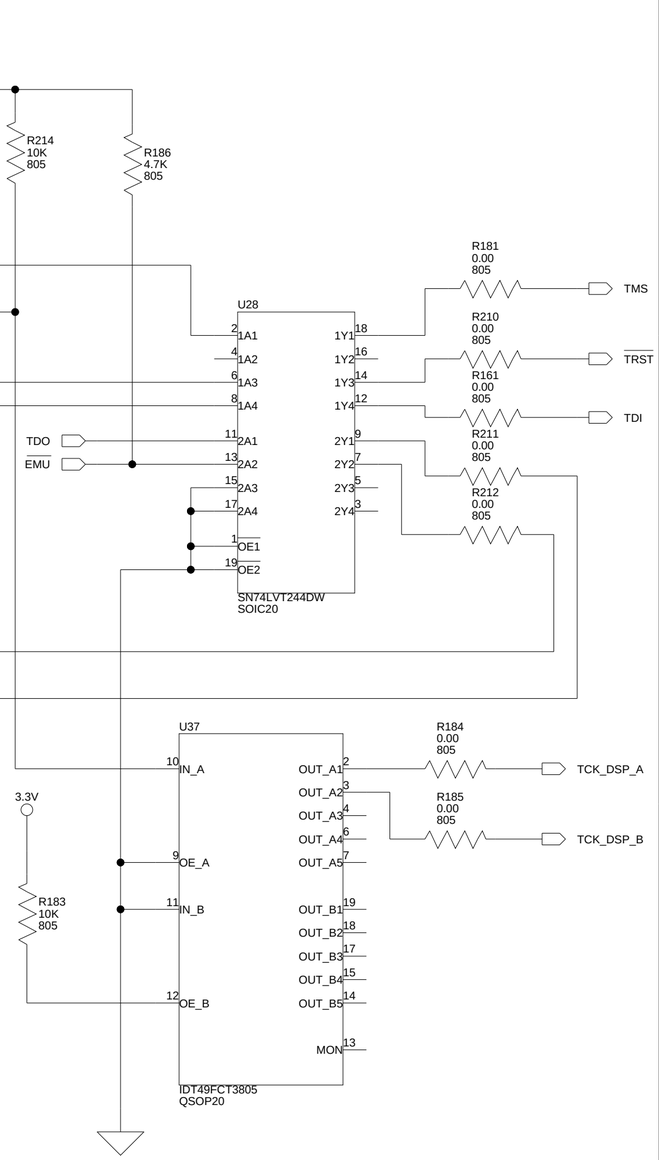
PLACE CLOSE TO FPGA PINS (CRITICAL)

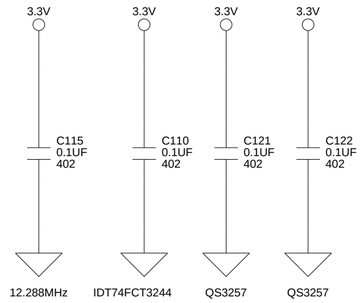
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

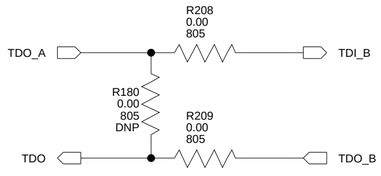
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com



DSP JTAG HEADER







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Title: ADSP-TS201S EZ-KIT LITE - JTAG/FPGA

Size	Board No.	Rev
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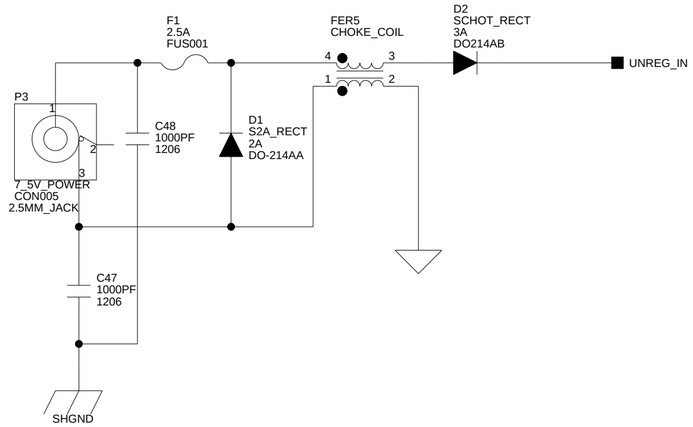

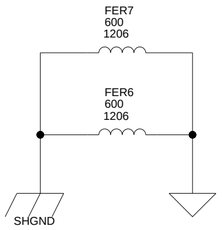

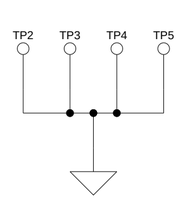

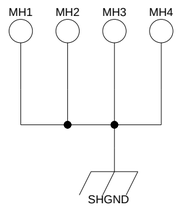

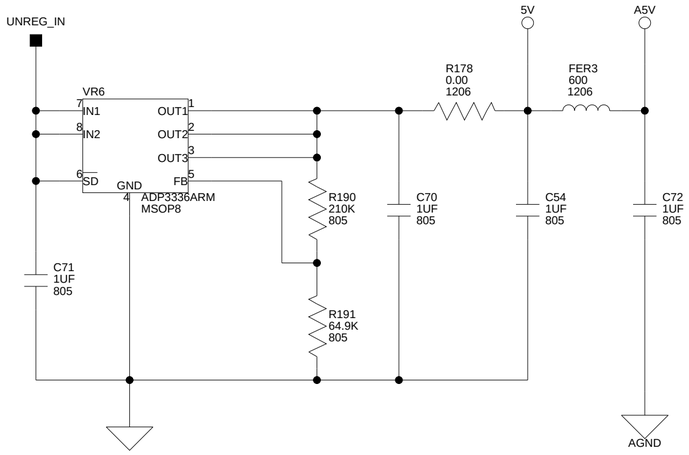

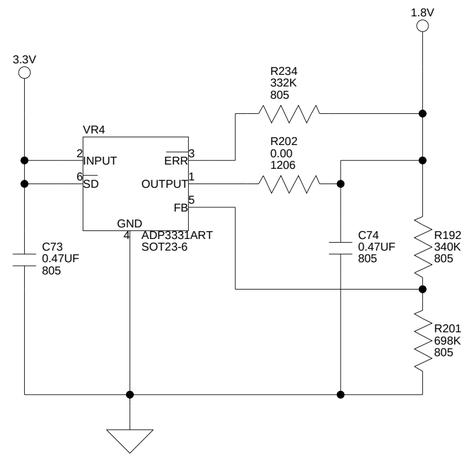

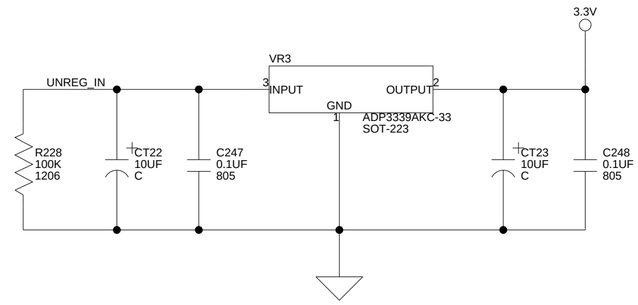

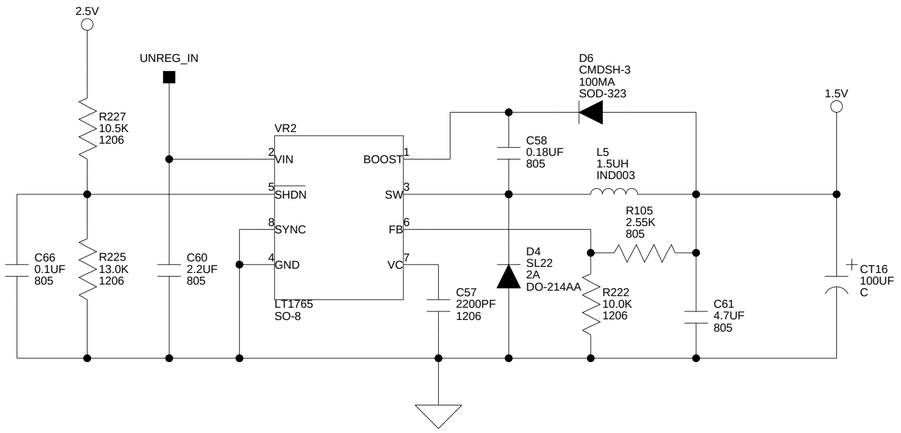

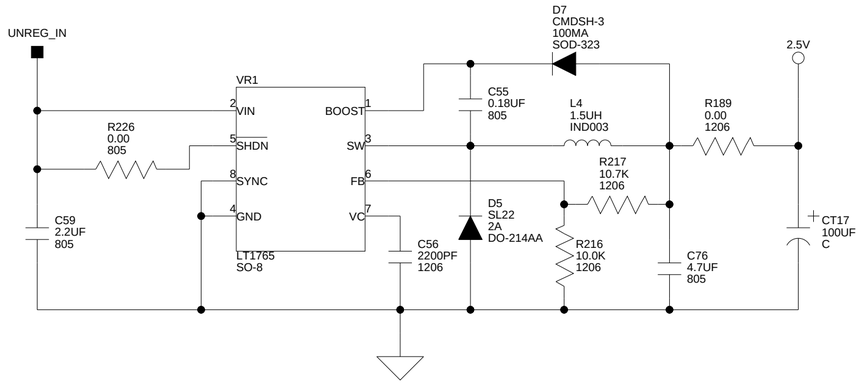

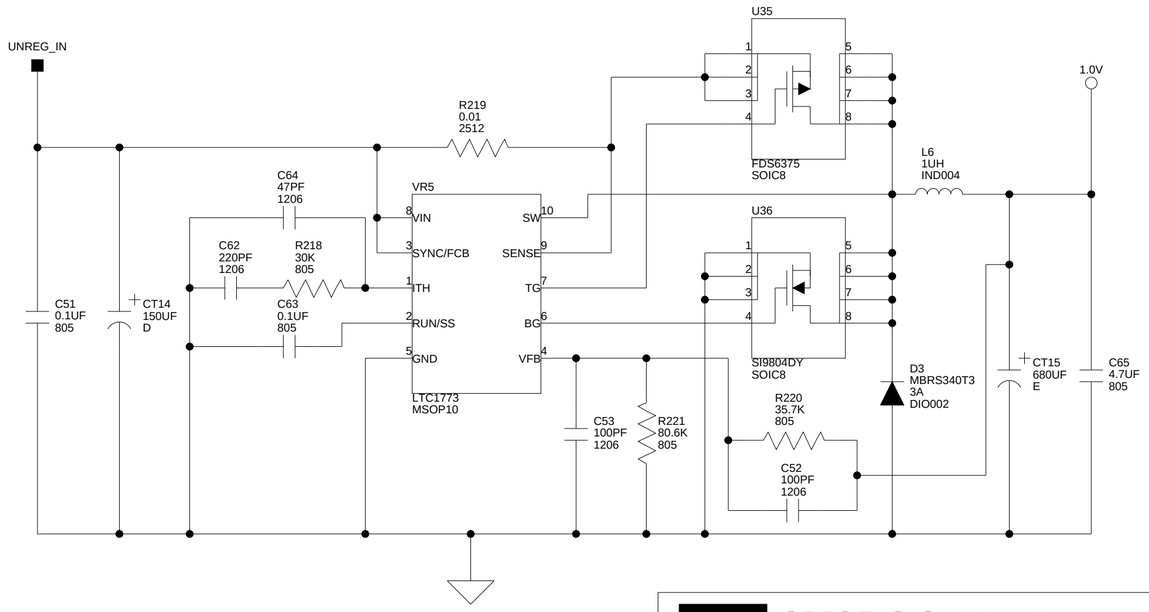

Approvals	**Date**	**Title**	ADSP-TS201S EZ-KIT LITE - POWER
Drawn		**Size** C	**Board No.** A0178-2002 **Rev** 1.1C
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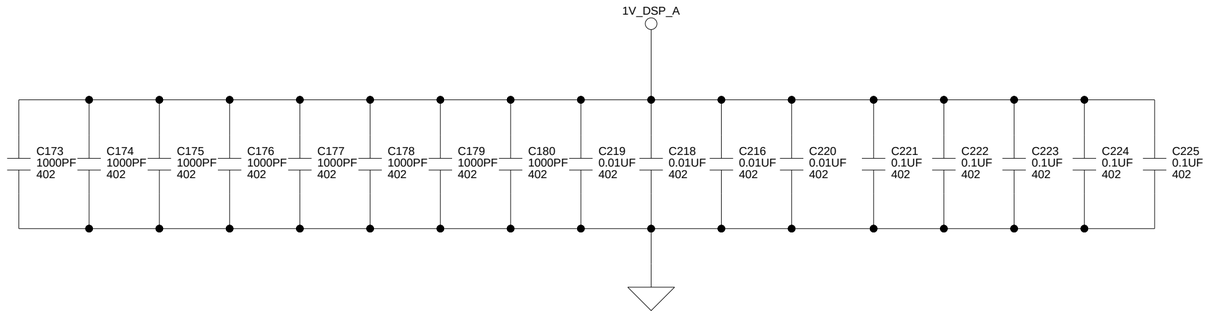
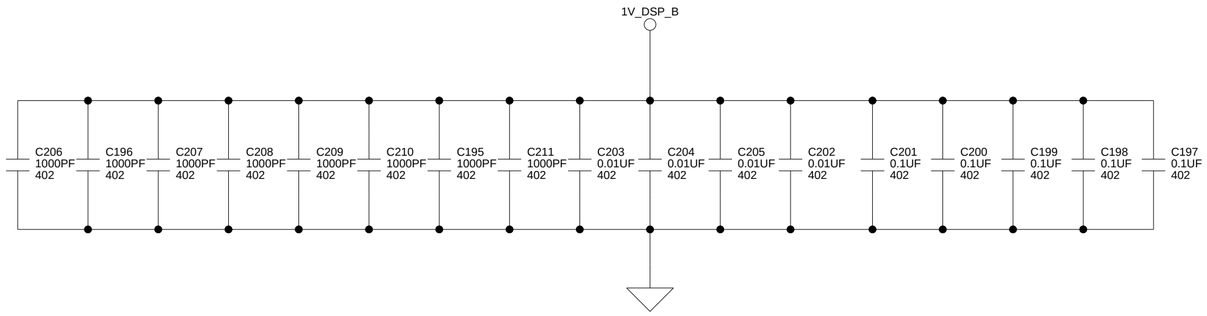
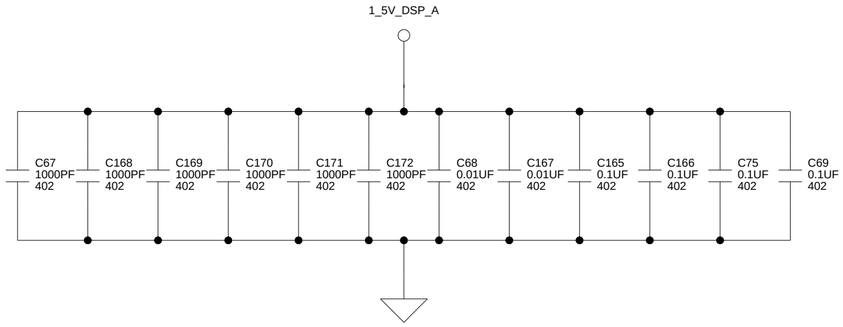
VDD (1.0V) Bypass Caps (per DSP)
(8) 1nF
(4) 0.01uF
(5) 0.1uF
(1) 100uF

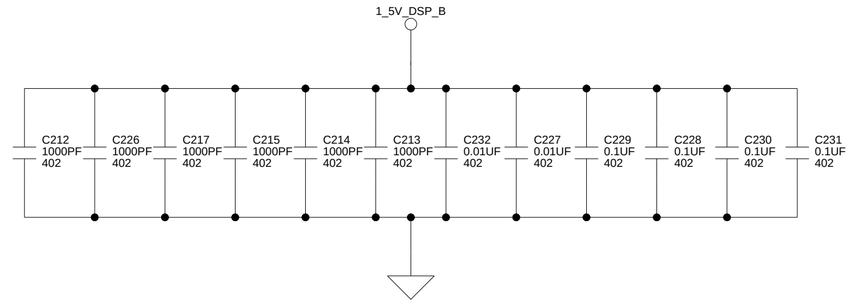




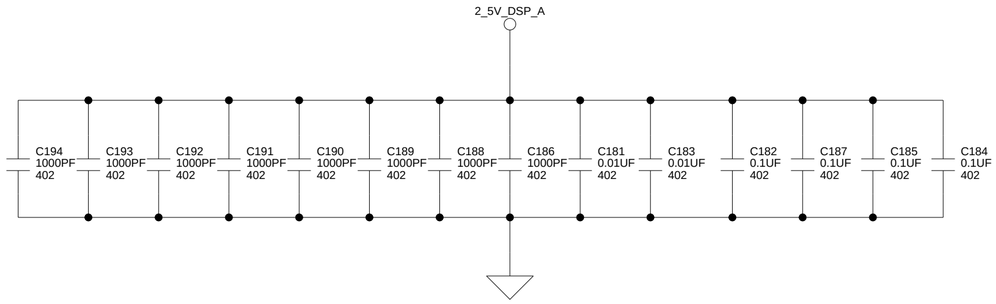
ALL BYPASS CAPS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CORISPONDING IC
TRACES FROM COMPONENT TO CAPACITOR AND FROM THE CAPACITOR TO GND SHOULD BE AS SHORT AS POSSIBLE
THE PRIORITY FOR THE PLACEMENT:
1V_DSP_X
1_5V_DSP_X
2_5V_DSP_X

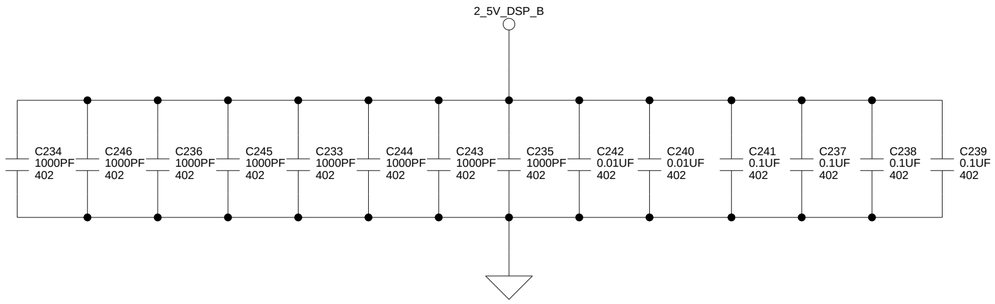
VDD_DRAM (1.5V) Bypass Caps (per DSP)
(6) 1nF
(2) 0.01uF
(4) 0.1uF
(1) 100uF





VDD_IO (2.5V) Bypass Caps (per DSP)
(8) 1nF
(2) 0.01uF
(4) 0.1uF
(1) 100uF





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Title	ADSP-TS201S EZ-KIT LITE - DSP BYPASS		
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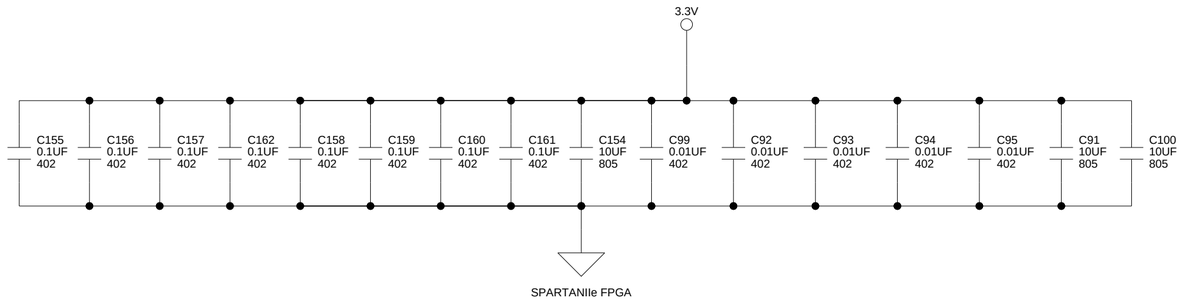

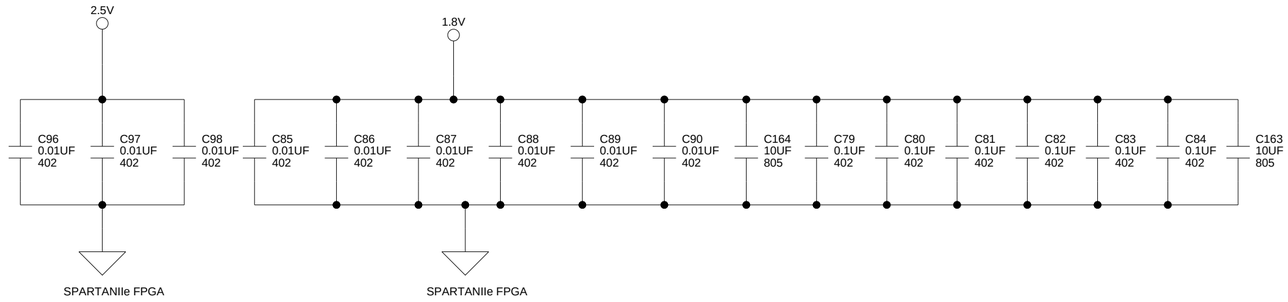

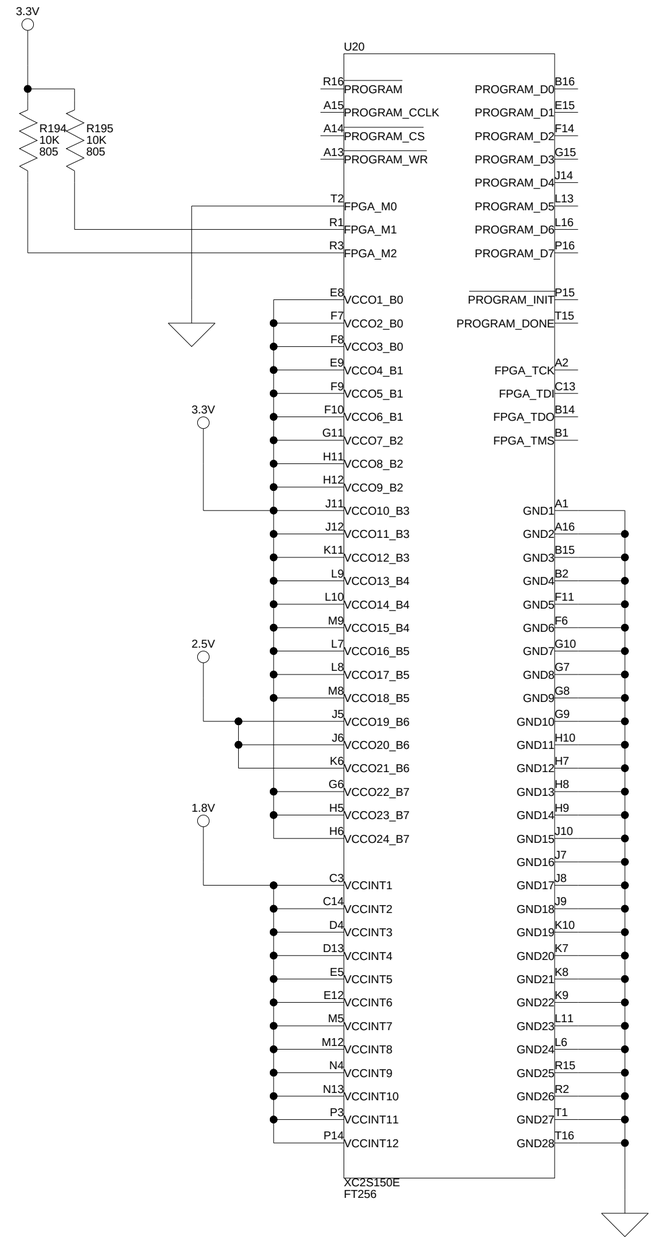

Approvals	Date
Drawn	
Checked	
Engineering	

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title: ADSP-TS201S EZ-KIT LITE - CONTROLLER		
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