ADSP-21161N EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
One Technology Way
Norwood, Mass. 02062-9106

ANALOG DEVICES

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The ADSP-21161N EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The ADSP-21161N EZ-KIT Lite evaluation system had been appended to the Technical Construction File referenced "**DSPTOOLS1**" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

Technical Certificate No: Z600ANA1.005

Issued by: Technology International (Europe) Limited
41 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TZ, UK

CE

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

CONTENTS

CONTENTS

PREFACE

Purpose of This Manual xiv
Intended Audience xiv
Manual Contents xv
What's New in This Manual xv
Technical or Customer Support xvi
Supported Processors xvi
Product Information xvi
MyAnalog.com xvii
DSP Product Information xvii
Related Documents xviii
Online Documentation xix
Printed Manuals xix
VisualDSP++ Documentation Set xix
Hardware Manuals xx
Data Sheets xx
Contacting DSP Publications xx
Notation Conventions xxi

GETTING STARTED

Contents of EZ-KIT Lite Package 1-1
PC Configuration 1-3
Installation Tasks 1-3
Installing VisualDSP++ and EZ-KIT Lite Software 1-4
Installing and Registering VisualDSP++ License 1-4
Setting Up EZ-KIT Lite Hardware 1-5
Installing EZ-KIT Lite USB Driver 1-6
Windows 98 USB Driver 1-7
Windows 2000 USB Driver 1-11
Windows XP USB Driver 1-12
Verifying Driver Installation 1-14
Starting VisualDSP++ 1-16

USING EZ-KIT LITE

EZ-KIT Lite License Restrictions 2-2
Memory Map 2-2
Using SDRAM Memory 2-3
Using FLAG Pins 2-5
Using Interrupt Pins 2-6
Using Audio Interface 2-6
Example Programs 2-8
Using Flash Programmer Utility 2-8
Using EZ-KIT Lite VisualDSP++ Interface 2-9

Boot Load 2-9
Target Options 2-9
While Target is Halted and On Emulator Exit Options 2-10
Other Options 2-10
Core Hang Conditions 2-11
Hardware Breakpoints 2-12
Common Hardware Breakpoint Attributes 2-13
Global Hardware Breakpoint Options 2-13
Data Hardware Breakpoints 2-15
Instruction Hardware Breakpoints 2-16
Other Breakpoints 2-17
Tips and Tricks Using Hardware Breakpoints 2-18
Latency 2-18
Restrictions 2-18
Setting a Breakpoint on a Single Address 2-18
Restricted Software Breakpoints 2-19

EZ-KIT LITE HARDWARE REFERENCE

System Architecture 3-2
External Port 3-3
Host Processor Interface (HPI) 3-3
SPORT Audio Interface 3-3
SPI Audio Interface 3-4
Breadboard Area 3-4
JTAG Emulation Port 3-5

Jumper Settings 3-5
SDRAM Disable Jumper (JP1) 3-5
SPDIF Selection Jumper (JP2) 3-5
MCLK Selection Jumper (JP3) 3-6
FLAG0 Enable Jumper (JP4) 3-7
FLAG1 Enable Jumper (JP5) 3-7
Sample Frequency Jumper (JP6) 3-7
ADC2 Input Mode Selection Jumpers (JP7–8) 3-8
MIC Gain Selection Jumpers (JP9–10) 3-8
ADC1 Input Selection Jumper (JP11) 3-9
Processor ID Jumper (JP19) 3-10
Boot Mode Selection Jumper (JP20) 3-10
Clock Mode Selection Jumper (JP21) 3-11
~BMS Enable Jumper (JP22) 3-12
AD1836 Control Selection Jumper (JP23) 3-12
SW1 Enable Jumper (JP26) 3-12
SW2 Enable Jumper (JP27) 3-12
LEDs and Push Buttons 3-13
Reset LEDs (LED1 and LED8) 3-14
FLAG LEDs (LED2–7) 3-14
VERF LED (LED9) 3-14
USB Monitor LED (LED10) 3-15
Power LED (LED11) 3-15
Programmable FLAG Push Buttons (SW1–4) 3-15

Interrupt Push Buttons (SW5–7) 3-15
Board Reset Push Button (SW8) 3-16
Connectors 3-16
USB Connector (P2) 3-16
Audio Connectors (P4–8, P17) 3-18
External Port Connector (P9) 3-18
Host Processor Interface Connector (P10) 3-19
JTAG Connector (P12) 3-19
Link Port Connectors (P13–14) 3-19
SPORT1 and SPORT3 Connector (P15) 3-20
Power Connector (P16) 3-20
Specifications 3-21
Power Supply 3-21
Board Current Measurements 3-21

BILL OF MATERIALS

INDEX

PREFACE

Thank you for purchasing the ADSP-21161N EZ-KIT Lite®, Analog Devices (ADI) evaluation system for SHARC® processors.

The SHARC processors are based on a 32-bit super Harvard architecture that includes a unique memory architecture comprised of two large on-chip, dual-ported SRAM blocks coupled with a sophisticated IO processor, which gives SHARC the bandwidth for sustained high-speed computations. SHARC represents today's de facto standard for floating-point DSP targeted for premium audio applications.

The evaluation system is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-21161N SHARC processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-21161N assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-21161N processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-21161N processor and the

evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and DSP development tools, go to `http://www.analog.com/dsp/tools/`.

ADSP-21161N EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The VisualDSP++ license provided with this EZ-KIT Lite evaluation system limits the size of a user program to 5K words of internal memory.

The board features:

- Analog Devices ADSP-21161N processor
  - 100 MHz Core Clock Speed
  - Core Clock Mode Jumper Configurable
- Analog Devices AD1836 96 kHz Audio Codec
  - Jumper Selectable Line-In or Mic-In 3.5 mm Stereo Jack
  - Line-Out 3.5 mm Stereo Jack
  - 4 RCA Jacks for Audio Input
  - 8 RCA Jacks for Audio Output
- Analog Devices AD1852 192 kHz Auxiliary DAC
- Crystal Semiconductor CS8414 96 kHz SPDIF Receiver
  - Optical and Coaxial Connectors for SPDIF Input
- Flash Memory
  - 512K x 8-bits

- Interface Connectors
  - 14-Pin Emulator Connector for JTAG Interface
  - SPORT Connectors
  - Link Port 0 and Link Port 1
  - External Port Connectors (not populated)
- General-Purpose IO
  - 4 Push Button Flags
  - 3 Push Button Interrupts
  - 6 LED Outputs
- Analog Devices ADP3338 and ADP3339 Voltage Regulators
- Breadboard area with typical SMT footprints

The EZ-KIT Lite board has a Flash memory device that can be used to store user-specific boot code. By configuring the jumpers for EPROM boot, the board can run as a stand-alone unit. The ADSP-21161N EZ-KIT Lite package contains a Flash programmer utility, which allows you to program the flash memory. The "Using Flash Programmer Utility" is described on page 2-8.

`SPORT0` and `SPORT2` connect to the audio codec, facilitating creation of audio-signal processing applications. `SPORT1` and `SPORT3` connect to off-board connectors of other serial devices.

Additionally, the EZ-KIT Lite board provides un-installed expansion connector footprints that allow you to connect to the processor's External Port (EP) and Host Processor Interface (HPI).

Purpose of This Manual

The *ADSP-21161N EZ-KIT Lite Evaluation System Manual* provides instructions for using the hardware and installing the software on your PC. The text includes guidelines for running your own code on the ADSP-21161N EZ-KIT Lite. The manual also describes the board's configuration and components. Finally, a schematic and a bill of materials are provided as a reference for future ADSP-21161N board designs.

Intended Audience

This manual is a user's guide and reference to the ADSP-21161N EZ-KIT Lite evaluation system. Programmers who are familiar with the Analog Devices SHARC processor architecture, operation, and programming are the primary audience for this manual.

Programmers who are unfamiliar with Analog Devices SHARC processors can use this manual in conjunction with the *ADSP-21161 SHARC Processor Hardware Reference* and *ADSP-21160 SHARC Processor Instruction Set Reference*, which describe the DSP'a architecture and instruction set. Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and the VisualDSP++ user's or getting started guides. For the locations of these documents, see "Related Documents" on page -xviii.

Manual Contents

The manual consists of:

- Chapter 1, "Getting Started" on page 1-1
  Provides software and hardware installation procedures, PC system requirements, and basic board information.
- Chapter 2, "Using EZ-KIT Lite" on page 2-1
  Provides information on the EZ-KIT Lite from a programmer's perspective and provides a simplified memory map.
- Chapter 3, "EZ-KIT Lite Hardware Reference" on page 3-1
  Provides information on the hardware aspects of the evaluation system.
- Appendix A, "Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "Schematics" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.
  The appendix is not part of the online Help. The online Help viewers should go the PDF version of the *ADSP-21161N EZ-KIT Lite Evaluation System Manual* located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics.

What's New in This Manual

This is the third edition of the *ADSP-21161N EZ-KIT Lite Evaluation System Manual*. The new edition includes the updated installation and license registration procedures.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the DSP Development Tools website at

  `www.analog.com/technology/dsp/developmentTools/index.html`

- Email questions to

  `dsptools.support@analog.com`

- Phone questions to **1-800-ANALOGD**
- Contact your ADI local sales office or authorized distributor
- Send questions by mail to

  ```
  Analog Devices, Inc.
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA
  ```

Supported Processors

The ADSP-21161N EZ-KIT Lite evaluation system supports Analog Devices ADSP-21161N SHARC processors.

Product Information

You can obtain product information from the Analog Devices website, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at www.analog.com. Our website provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices website that allows customization of a webpage to display only the latest information on products you are interested in. You can also choose to receive weekly email notification containing updates to the webpages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your email address.

DSP Product Information

For information on digital signal processors, visit our website at www.analog.com/dsp, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- Email questions or requests for information to dsp.support@analog.com
- Fax questions or requests for information to **1-781-461-3010** (North America) or **+49 (0) 89 76903-157** (Europe)

Related Documents

For information on product related development software, see the following publications.

Table 1. Related DSP Publications

Title	Description
ADSP-21161N DSP Data Sheet	General functional description, pinout, and timing
ADSP-21161 SHARC Processor Hardware Reference	Description of internal processor architecture, registers, and all peripheral functions
ADSP-21160 SHARC Processor Instruction Set Reference	Description of all allowed processor assembly instructions

Table 2. Related VisualDSP++ Publications

Title	Description
VisualDSP++ 3.5 User's Guide for 32-Bit Processors	Detailed description of VisualDSP++ 3.5 features and usage
VisualDSP++ 3.5 Assembler and Preprocessor Manual for SHARC Processors	Description of the assembler function and commands for SHARC processors
VisualDSP++ 3.5 C/C++ Complier and Library Manual for SHARC Processors	Description of the complier function and commands for SHARC processors
VisualDSP++ 3.5 Linker and Utilities Manual for 32-Bit Processors	Description of the linker function and commands for the 32-bit processors
VisualDSP++ 3.5 Loader Manual for 32-Bit Processors	Description of the loader function and commands for the 32-bit processors

The listed documents can be found through online Help or in the `Docs` folder of your VisualDSP++ installation. Most documents are available in printed form.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, refer to the documentation that accompanies the emulator.

Online Documentation

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-21161N EZ-KIT Lite evaluation system.

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and select **Start –>Programs –>Analog Devices–>VisualDSP++ for 32-bit Processors –>VisualDSP++ Documentation**.

To view ADSP-21161N EZ-KIT Lite Help, which now is a part of the VisualDSP++ Help system, go the **Contents** tab of the Help window and select **Manuals –>Hardware Tools –>EZ-KIT Lite Evaluation Systems**.

For more documentation, please go to
`http://www.analog.com/technology/dsp/library.html`.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

Printed copies of VisualDSP++ manuals may be purchased through Analog Devices Customer Service at **1-781-329-4700**; ask for a Customer Service representative. The manuals can be purchased only as a kit. For additional information, call **1-603-883-2430**.

If you do not have an account with Analog Devices, you will be referred to Analog Devices distributors. To get information on our distributors, log onto `www.analog.com/salesdir/continent.asp`.

Hardware Manuals

Printed copies of hardware reference and instruction set reference manuals can be ordered through the Literature Center or downloaded from the Analog Devices website. The phone number is **1-800-ANALOGD** (**1-800-262-5643**). The manuals can be ordered by a title or by product number located on the back cover of each manual.

Data Sheets

All data sheets can be downloaded from the Analog Devices website. As a general rule, printed copies of data sheets with a letter suffix (L, M, N, S) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) or downloaded from the website. Data sheets without the suffix can be downloaded from the website only—no hard copies are available. You can ask for the data sheet by part name or by product number.

If you want to have a data sheet faxed to you, the phone number for that service is **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. Call the Literature Center first to find out if requested data sheets are available.

Contacting DSP Publications

Please send your comments and recommendations on how to improve our manuals and online Help. You can contact us at `dsp.techpubs@analog.com`.

Notation Conventions

The following table identifies and describes text conventions used in this manual.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

Example	Description
Close command (**File** menu) or **OK**	Text in **bold** style indicates the location of an item within the VisualDSP++ environment's and boards' menu system and user interface items.
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets separated by vertical bars; read the example as `this` or `that`.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of `this`.
`PF9-0`	Registers, connectors, pins, commands, directives, keywords, code examples, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	A note providing information of special interest or identifying a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	A caution providing information about critical design or programming issues that influence operation of a product. In the online version of this book, the word **Caution** appears instead of this symbol.

1 GETTING STARTED

This chapter provides information you need to begin using ADSP-21161N EZ-KIT Lite evaluation system. For correct operation, install the software and hardware in the order presented in "Installation Tasks" on page 1-3.

The chapter includes the following sections.

- "Contents of EZ-KIT Lite Package" on page 1-1
  Provides a list of the components shipped with this EZ-KIT Lite evaluation system.
- "PC Configuration" on page 1-3
  Describes the minimum requirements for the PC to work with the EZ-KIT Lite.
- "Installation Tasks" on page 1-3
  Describes the step-by-step procedures for setting up the hardware and software.

Contents of EZ-KIT Lite Package

Your ADSP-21161N EZ-KIT Lite evaluation system package contains the following items.

- ADSP-21161N EZ-KIT Lite board
- *EZ-KIT Lite Installation Procedure*
- *VisualDSP++ 3.5 Installation Quick Reference Card*

- CD containing:
  - VisualDSP++ 3.5 for 32-bit processors with a limited license
  - ADSP-21161N EZ-KIT Lite debug software
  - USB driver files
  - Example programs
  - *ADSP-21161N EZ-KIT Lite Evaluation System Manual* (this document)
- Universal 7V DC power supply
- USB 2.0 type cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

PC Configuration

For correct operation of the VisualDSP++ software and the EZ-KIT Lite, your computer must have the minimum configuration:

Windows 98, Windows 2000, Windows XP
Intel (or comparable) 166MHz processor
VGA Monitor and color video card
2-button mouse
50 MB free on hard drive
32 MB RAM
Full-speed USB port
CD-ROM Drive

EZ-KIT Lite does not run under Windows 95 or Windows NT.

Installation Tasks

The following task list is provided for the safe and effective use of the ADSP-21161N EZ-KIT Lite. Follow the instructions in the presented order to ensure correct operation of your software and hardware.

1. VisualDSP++ and EZ-KIT Lite software installation
2. VisualDSP++ license installation and registration
3. EZ-KIT Lite hardware setup
4. EZ-KIT Lite USB driver installation
5. USB driver installation verification
6. VisualDSP++ startup

Installing VisualDSP++ and EZ-KIT Lite Software

This EZ-KIT Lite comes with the latest version of VisualDSP++ 3.5 for 32-bit processors. VisualDSP++ installation includes EZ-KIT Lite installations.

To install VisualDSP++ and EZ-KIT Lite software:

1. Insert the VisualDSP++ installation CD into the CD-ROM drive.
2. If Autoplay is enabled on your PC, you see the **Install Shield Wizard Welcome** screen. Otherwise, choose **Run** from the **Start** menu, and enter `D:\ADI_Setup.exe` in the **Open** field, where `D` is the name of your local CD-ROM drive.
3. Follow the on-screen instructions to continue installing the software.
4. At the **Custom Setup** screen, select your EZ-KIT Lite from the list of available systems and choose the installation directory. Click an icon in the **Feature Description** field to see the selected system's description. When you have finished, click **Next**.
5. At the **Ready to Install** screen, click **Back** to change your install options, click **Install** to install the software, or click **Cancel** to exit the install.
6. When the EZ-KIT Lite installs, the **Wizard Completed** screen appears. Click **Finish**.

Installing and Registering VisualDSP++ License

VisualDSP++ and EZ-KIT Lites are licensed products. You may run only one copy of the software for each license purchased. Once a new copy of the VisualDSP++ or EZ-KIT Lite software is installed on your PC, you must install, register, and validate your licence.

The *VisualDSP++ 3.5 Installation Quick Reference Card* included in your package will guide you through the licence installation and registration process (refer to Tasks 1, 2, and 3).

Setting Up EZ-KIT Lite Hardware

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-21161N EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

To connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package. Be careful when handling the board to avoid the discharge of static electricity, which may damage some components.
2. Figure 1-1 shows the default jumper settings, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before moving to the next step.
3. Plug the provided power supply into `P16` on the EZ-KIT Lite board. Visually verify that the green power LED (`LED11`) is on. Also verify that the two red RESET LEDs (`LED1` and `LED8`) go on for a moment and then go off.

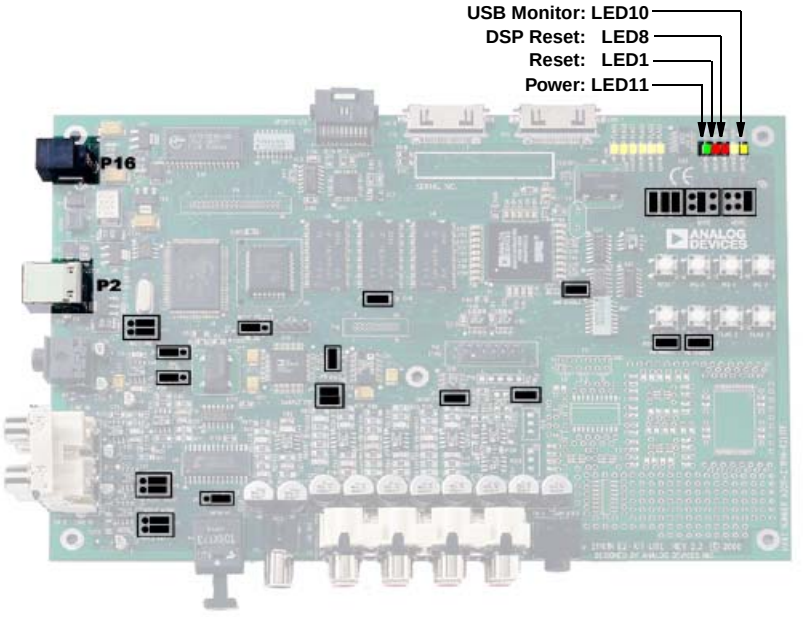


Figure 1-1. EZ-KIT Lite Hardware Setup

4. Connect one end of the USB cable to an available full-speed USB port on your PC and the other end to P2 on the ADSP-21161N EZ-KIT Lite board.

Installing EZ-KIT Lite USB Driver

The EZ-KIT Lite evaluation system installed on the following platforms requires one full-speed USB port.

- "Windows 98 USB Driver" on page 1-7 describes the installation on Windows 98.
- "Windows 2000 USB Driver" on page 1-11 describes the installation on Windows 2000.

- "Windows XP USB Driver" on page 1-12 describes the installation on Windows XP.

The USB driver used by the debug agent is not Microsoft certified because it is intended for a development or laboratory environment, not a commercial environment.

Windows 98 USB Driver

Before using the ADSP-21161N EZ-KIT Lite for the first time, the Windows 98 USB driver must first be installed.

To install the USB driver:

1. Insert the CD into the CD-ROM drive.
   The connection of the device to the USB port activates the Windows 98 **Add New Hardware Wizard** shown in Figure 1-2.

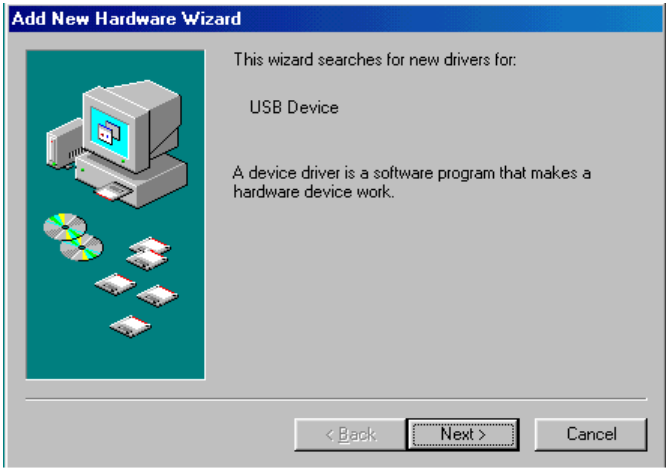


Figure 1-2. Windows 98 – Add New Hardware Wizard

2. Click **Next**.

3. Select **Search for the best driver for your device**, as shown in Figure 1-3.

Figure 1-3. Windows 98 – Searching for Driver

4. Click **Next**.
5. Select **CD-ROM drive**, as shown in Figure 1-4.

Figure 1-4. Windows 98 – Searching for CD-ROM

6. Click **Next**.
   Windows 98 locates the `WmUSBEz.inf` file on the installation CD, as shown in Figure 1-5.

Figure 1-5. Windows 98 – Locating Driver

7. Click **Next**.
   The **Coping Files** dialog box appears (Figure 1-6).

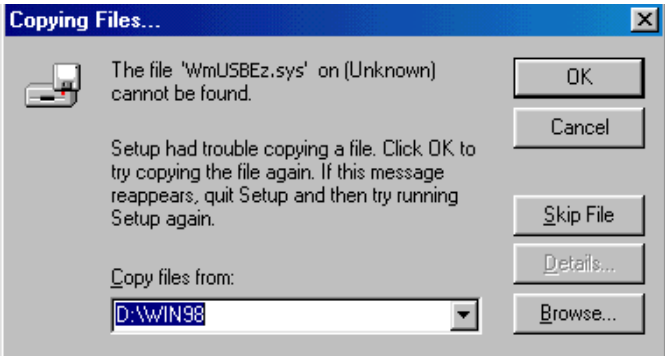


Figure 1-6. Windows 98 – Searching for .SYS File

8. Click **Browse**.
   The **Open** dialog box, shown in Figure 1-7, appears on the screen.

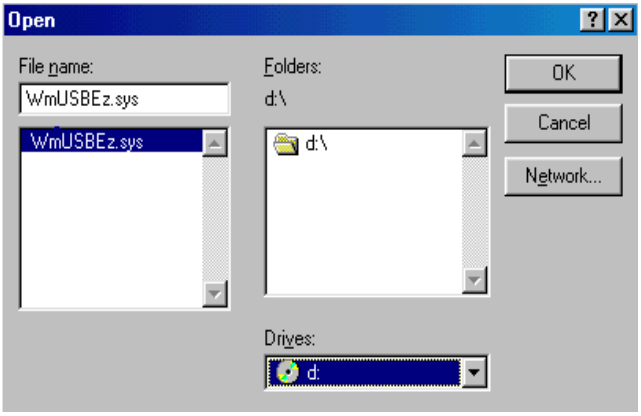


Figure 1-7. Windows 98 – Opening .SYS File

9. In **Drives**, select your CD-ROM drive.
10. Click **OK**. The **Copying Files** dialog box (Figure 1-8) appears.

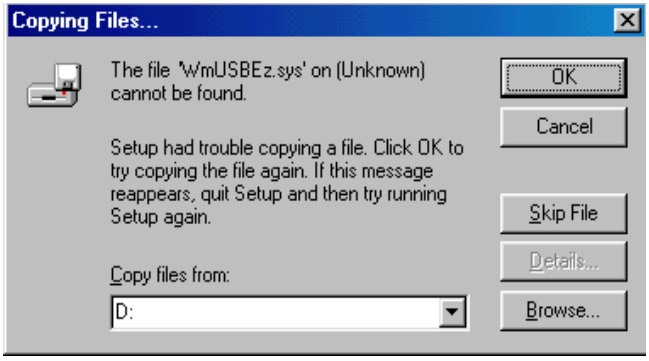


Figure 1-8. Windows 98 – Copying .SYS File

11. Click **OK**.
    The driver installation is now complete, as shown in Figure 1-9.

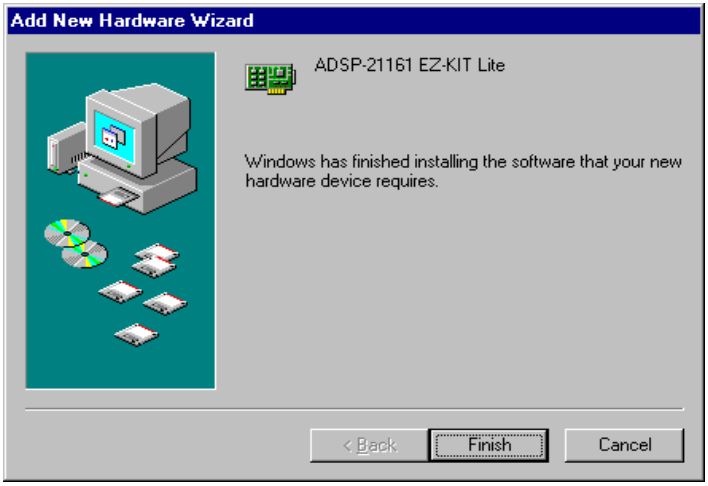


Figure 1-9. Windows 98 – Completing Software Installation

12. Click **Finish** to exit the wizard.
13. Verify the installation by following the instructions in "Verifying Driver Installation" on page 1-14.

Windows 2000 USB Driver

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the selected EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.

To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the *VisualDSP++ 3.5 Installation Quick Reference Card* for a detailed installation description.
   When installing VisualDSP++ 3.5 on Windows 2000, make sure the appropriate EZ-KIT Lite component is selected for the installation.
2. Connect the EZ-KIT Lite device to your PC's USB port. Windows 2000 automatically detects an EZ-KIT device and automatically installs the appropriate driver for the selected device (see step 1).
3. Verify the installation by following the instructions in "Verifying Driver Installation" on page 1-14.

Windows XP USB Driver

VisualDSP++ 3.5 installation software pre-installs the necessary drivers for the selected EZ-KIT Lite. The install also upgrades an older driver if such is detected in the system.

Prior to running the VisualDSP++ 3.5 installer, ensure there are no other Hardware Wizard windows running in the background. If there are any wizard windows running, close them before starting the installer.

To install the USB driver:

1. If VisualDSP++ 3.5 is already installed on your system, go to step 2.
   Otherwise, run VisualDSP++ 3.5 installation. Refer to the *VisualDSP++ 3.5 Installation Quick Reference Card* for a detailed

installation description.
When installing VisualDSP++ 3.5 on Windows XP, make sure the appropriate EZ-KIT Lite component is selected for the installation.

2. Connect the EZ-KIT Lite device to your PC's USB port.
   By connecting the device to the USB port you activate the Windows XP **Found New Hardware Wizard**, shown in Figure 1-10.

Figure 1-10. Windows XP – Found New Hardware Wizard

3. Select **Install the software automatically** (**Recommended**) and click **Next**.

When Windows XP completes the driver installation for the selected device (see step 1), a window shown in Figure 1-11 appears on the screen.

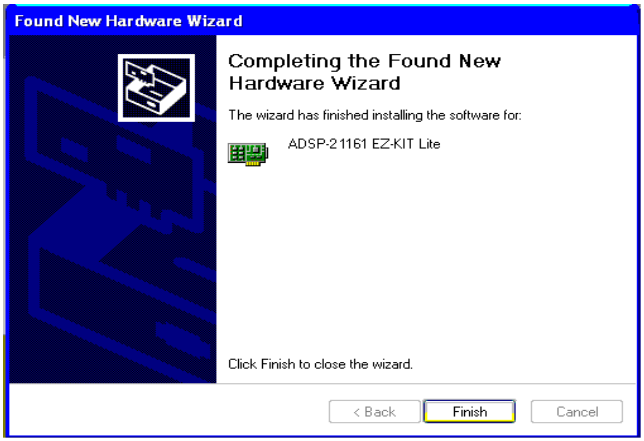


Figure 1-11. Windows XP – Completing Driver Installation

4. Verify the installation by following the instructions in "Verifying Driver Installation".

Verifying Driver Installation

Before launching the EZ-KIT Lite evaluation system, verify that the USB driver software is installed properly:

1. Ensure that the USB cable connects to the evaluation board and the PC.
2. Press and release the RESET button (SW8) on the evaluation board.
3. Verify that the red DSP RESET LED (LED8) blinks once and then blinks again in 15 seconds.

4. After the DSP RESET LED (LED8) blinks for the second time, verify that the yellow USB monitor LED (LED10) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

5. Verify that the USB driver software is installed properly. Open Windows **Device Manager** and verify that **ADSP-21161N EZ-KIT Lite** shows under **ADI Development Tools** with no exclamation point, as in Figure 1-12.

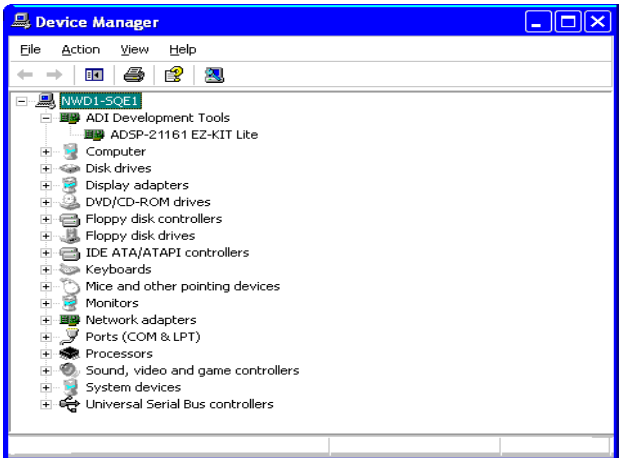


Figure 1-12. Device Manager Window

If using an EZ-KIT Lite on Windows 98, disconnect the USB cable from the board before booting the PC. When Windows 98 is booted and you are logged on, re-connect the USB cable to the board. The operation should continue normally from this point.

Starting VisualDSP++

To set up a session in VisualDSP++:

1. Verify that the yellow USB monitor LED (LED10, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. Hold down the **Control** (CTRL) key.
3. Select the **Start** button on the Windows taskbar, then choose **Programs–>Analog Devices –>VisualDSP++ for 32-bit Processors–>VisualDSP++ Environment**.
   If you are running VisualDSP++ for the first time, go to step 4. If you already have existing sessions, the **Session List** dialog box appears on the screen.
4. Click **New Session**.
5. The **New Session** dialog box, shown in Figure 1-13, appears on the screen.

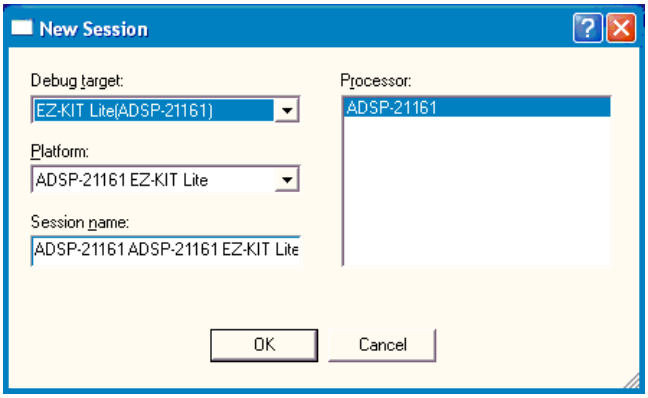


Figure 1-13. New Session Dialog Box

6. In **Debug Target**, choose **EZ-KIT Lite (ADSP-21161N)**.

7. In **Processor**, choose the appropriate processor, **ADSP-21161N**.
8. Type a new target name in **Session Name** or accept the default name.
9. Click **OK** to return to the **Session List**. Highlight the new session and click **Activate**.

2 USING EZ-KIT LITE

This chapter provides specific information to assist you with developing programs for the ADSP-21161N EZ-KIT Lite evaluation system. This information appears in the following sections.

- "EZ-KIT Lite License Restrictions" on page 2-2
  Describes the restrictions of the VisualDSP++ license shipped with the EZ-KIT Lite.
- "Memory Map" on page 2-2
  Defines the ADSP-21161N EZ-KIT Lite's memory map.
- "Using SDRAM Memory" on page 2-3·
  Defines the register values to configure the on-board SDRAM.
- "Using FLAG Pins" on page 2-5
  Describes the board's FLAG pins.
- "Using Interrupt Pins" on page 2-6
  Describes the board's interrupt pins.
- "Using Audio Interface" on page 2-6
  Describes the board's audio interface.
- "Example Programs" on page 2-8
  Provides information about example programs included in the ADSP-21161N EZ-KIT Lite.
- "Using Flash Programmer Utility" on page 2-8
  Provides information on the Flash Programmer utility included with the EZ-KIT Lite software.

- "Using EZ-KIT Lite VisualDSP++ Interface" on page 2-9
  Describes the trace, performance monitoring, boot loading, context switching, and target options facilities of the EZ-KIT Lite system.

For detailed information on how to program the ADSP-21161N SHARC processor, refer to the documents referenced in "Related Documents".

EZ-KIT Lite License Restrictions

The license shipped with the EZ-KIT Lite imposes the following restrictions.

- The size of a user program's code is limited to 5K words (1/4) of the ADSP-21161N processor's program memory space.
- No connections to simulator or emulator sessions are allowed.
- The EZ-KIT Lite hardware must be connected and powered up in order to use VisualDSP++ with a kit license.

Memory Map

The ADSP-21161N processors includes 1 Mbit of internal SRAM for program storage or data storage. The configuration of internal SRAM is detailed in the *ADSP-21161 SHARC Processor Hardware Reference*.

The ADSP-21161N EZ-KIT Lite board contains 512K x 8-bits of external Flash memory. The Flash memory is connected to the processors's ~MS1 and ~BMS memory select pins. The Flash memory can be accessed in either the boot memory space or the external memory space. The external memory interface is also connected to 1M x 48-bit SDRAM memory. The Flash memory is connected to the ~MS0 pin.

Table 2-1. EZ-KIT Lite Evaluation Board Memory Map

	Start Address	End Address	Content
Internal Memory	0x0000 0000	0x0001 FFFF	IOP Registers (Internal)
	0x0002 0000	0x0002 1FFF	Block 0 Long Word Addressing
	0x0002 8000	0x0002 9FFF	Block 1 Long Word Addressing
	0x0004 0000	0x0004 3FFF	Block 0 Normal Word Addressing
	0x0005 0000	0x0005 3FFF	Block 1 Normal Word Addressing
	0x0008 0000	0x0008 7FFF	Block 0 Short Word Addressing
	0x000A 0000	0x000A 7FFF	Block 1 Short Word Addressing
	0x0010 0000	0x001F FFFF	Multi-processor Memory Space
External Memory	0x0020 0000	0x002F FFFF	External Memory Space Bank 0 (SDRAM)
	0x0400 0000	0x047F FFFF	External Memory Space Bank 1 (FLASH)
	0x0800 0000	0x0BFF FFFF	External Memory Space Bank 2
	0x0C00 0000	0x0FFF FFFF	External Memory Space Bank 3

Using SDRAM Memory

To use the SDRAM memory, set the two SDRAM control registers to the values shown in Listing 2-1.

Listing 2-1. ADSP-21161N EZ-KIT Lite – SDRAM Settings

```
/* SDRAM Controller Setup for the ADSP-21161N EZ-KIT Lite    */
/* Assumes SDRAM part# Micron MT48LC16M16A1-7SE (1Mx16-bit,
2 banks)                                                     */
/* Default Factory Hardware settings (rev2.3)                */
/* LK_CFG[1:0]= 10,~CLDBL=1                                  */
/* CLKIN=25 MHz, => CCLK=100 MHz                             */
/* 3 SDRAMs by 16 bits wide total = 3x(1Mx16-bit) = 1M x 48-bit */
```

```
/* Mapped to MS0 addresses 0x00200000-0x002fffff */
/* Estimated SDCLK 50 MHz => SDCKR=0             */
/* Settings must be double counted for SDCKR-bit=0, except CAS
Latency) */
/* 50 MHz min @ CL=2 -> SDCL=2 [CAS Latency]             */
/* tRAS=42ns min     -> SDTRAS=5*2=10 [precharge delay]  */
/* tRP=21ns min      -> SDTRP=3*2=6   [active delay]     */
/* tRCD=20ns min     -> SDTRCD=2*2=4  [CAS-to-RAS delay] */
/* tREF=64ms/4K rows ->                                  */
/* -> SDRDIV= (100MHz*64ms/4096) - 13 = 1549 = 0x60D cycles */

/* Note: If you change any clock, you have to change all settings
for best performance */

init_21161_SDRAM_controller:
ustat1=dm(WAIT);
bit clr ustat1 0x000FFFFF;  /* clear MS0 wait state count */
dm(WAIT)=ustat1;
ustat1=0x60D;               /* refresh rate */
dm(SDRDIV)=ustat1;
ustat1=0x040146A2;          /* mask in SDRAM settings */
dm(SDCTL)=ustat1;
init_21161_SDRAM_controller.end:
rts;
```

The SDRAM registers are configured automatically through the debugger. Checking the **Manual External Mem configuration** box in the **Target Options** dialog box, as shown in Figure 2-1 on page 2-10, disables the automatic setting.

Using FLAG Pins

The ADSP-21161N holds 12 asynchronous FLAG IO pins. Ten of these pins (FLAG0-9) are available for interaction with the running program.

After the processor is reset, the FLAGs are configured as inputs. The directions of the FLAGs are configured though the MODE2 register and are set and read though the FLAG registers. The FLAG registers are summarized in Table 2-2. For more information on FLAGs, refer to the *ADSP-21161 SHARC Processor Hardware Reference.*

Table 2-2. FLAG Pin Summary

FLAG[1]	Connects To	Description
FLAG0	SW1/AD1836_SPI_SELECT	FLAG0 connects to push button SW1 for user input and to the SPI select pin on the AD1836 audio codec.
FLAG1	SW2/AD1852_SPI_SELECT	FLAG1 connects to push button SW2 for user input and to the SPI select pin on the AD1852 auxiliary DAC.
FLAG2	SW3	FLAG2 connects to push button SW3 for user input.
FLAG3	SW4	FLAG3 connects to push button SW4 for user input.
FLAG4-FLAG9	LED2-LED7	FLAG4-9 connect to LEDs on the EZ-KIT Lite board and are for user output.
FLAG10 and FLAG11	Not connected	Not available

1 FLAG0-FLAG3 are available on connector P10.

Using Interrupt Pins

The ADSP-21161N holds three interrupt pins (IRQ0-2) that let you interact with the running program. Each of the three external interrupts is directly accessible through the push button switches SW5-SW7 on the EZ-KIT Lite board. Interrupt pins are summarized in Table 2-3. For more information, refer to the *ADSP-21161 SHARC Processor Hardware Reference*.

Table 2-3. Interrupt Pin Summary

Interrupt[1]	Connects To	Description
IRQ0	SW5	IRQ0-2 connect to the push buttons and supply feedback for program execution. For instance, you can write your code to trigger a FLAG when a routine is complete.
IRQ1	SW6	
IRQ2	SW7	

1 IRQ0-3 are available on connector P10.

Using Audio Interface

The audio interface consists of the AD1836 audio codec, the AD1852 auxiliary DAC and the CS8414 SPDIF receiver. SPORT0 and SPORT2 connect to the audio devices and provide 3 channels of stereo input (1 channel digital, 2 channels analog) and 4 channels of stereo output.

Analog audio input is facilitated by a 3.5 mm stereo jack (P7) and four RCA mono jacks (P6). One of the AD1836 stereo input channels is dedicated to two of the RCA mono jacks. The other stereo input channels can either be supplied by the 3.5 mm stereo jack or the other two RCA mono jacks. JP11 determines which jack is used for audio input. Digital audio input can be provided on either a single RCA mono jack (P5) or an optical input connector (P4). JP2 determines the source. Three of the stereo out-

put channels come from the AD1836, while the final channel is from the AD1852. See "Audio Connectors (P4–8, P17)" on page 3-18 for more information about the connectors.

The AD1836 multi-channel codec features six digital-to-analog converters (DACs) and four analog-to-digital converters (ADCs) and supports multiple digital stereo channels with 24-bit conversion resolution and a 96 kHz sample rate. The AD1836 features a 108 dB dynamic range for each of its six DACs and a 104 dB dynamic range for its four ADCs. The AD1836 is configured through its SPI port. The ADSP-21161N processor is capable of accessing the AD1836's SPI port through the SPI port as well as through `SPORT1`. For more information, see "AD1836 Control Selection Jumper (JP23)" on page 3-12.

The AD1852 is a complete 18/20/24-bit single-chip stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator, digital interpolation filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port. The AD1852 is fully compatible with all known DVD formats, including 192 kHz and 96 kHz sample frequencies and 24 bits. It also is backwards compatible by supporting 50/15µs digital de-emphasis intended for "redbook" Compact Discs, as well as de-emphasis at 32 kHz and 48 kHz sample rate.

The CS8414 is a monolithic CMOS device that receives and decodes audio data up to 96 kHz, according to the AES/EBU, IEC958, S/PDIF, and EIAJ CP340/1201 interface standards. The CS8414 receives data from a transmission line, recovers the clock and synchronization signals, and de-multiplexes the audio and digital data. The CS8414 is setup to operate in I^2S compatible mode.

The `Microphone` and `Line-In` jacks connect to the left and right `ADC1` channel on the AD1836, depending on the setting of jumpers. See "MIC Gain Selection Jumpers (JP9–10)" on page 3-8 and "ADC1 Input Selection Jumper (JP11)" on page 3-9 for more information. Two RCA jacks

connect to ADC2 on the AD1836. This input is configured though the input mode selection jumpers, See "ADC2 Input Mode Selection Jumpers (JP7–8)" on page 3-8 for more information.

The Line-Out jacks connect to the left and right DAC outputs of the AD1836 and AD1852.

The CS8414 includes an error flag (VERF) to indicate that the audio output may not be valid. This signal connects to a LED (LED9) on the board. This signal may also be used by interpolation filters to provide error correction.

Example Programs

Example programs are provided with the ADSP-21161N EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in \…\VisualDSP 3.5 32-Bit\211xx\EZ-KITs\ADSP-21161N\Examples. Please refer to the readme file provided with each example for more information.

Using Flash Programmer Utility

The ADSP-21161N EZ-KIT Lite evaluation system includes a Flash Programmer utility. The utility allows you to program the Flash memory on the EZ-KIT Lite. The Flash Programmer is installed with VisualDSP++. Once the utility is installed, it is accessible from the **Tools** pull-down menu.

For more information on the Flash Programmer utility, select **Start** and choose **Programs–>Analog Devices–>VisualDSP++ 3.5 for 32-bit Processors–>VisualDSP++ Documentation**.

Using EZ-KIT Lite VisualDSP++ Interface

This section provides information about the following parts of the VisualDSP++ graphical user interface:

- "Boot Load" on page 2-9
- "Target Options" on page 2-9
- "Core Hang Conditions" on page 2-11
- "Hardware Breakpoints" on page 2-12
- "Restricted Software Breakpoints" on page 2-19

Boot Load

Choosing **Boot Load** from the **Settings** menu runs the processor and performs a hard reset on the board. This command saves you from having to shut down VisualDSP++, reset the EZ-KIT Lite board, and bring up VisualDSP++ again when you want to perform a hard reset.

Use this feature when loading debug boot code from an external part or when you want to put the device into a known state.

Target Options

Choosing **Target Options** from the **Settings** menu opens the **Target Options** dialog box (Figure 2-1). Use target options to control certain aspects of the processor on the ADSP-21161N EZ-KIT Lite evaluation system.

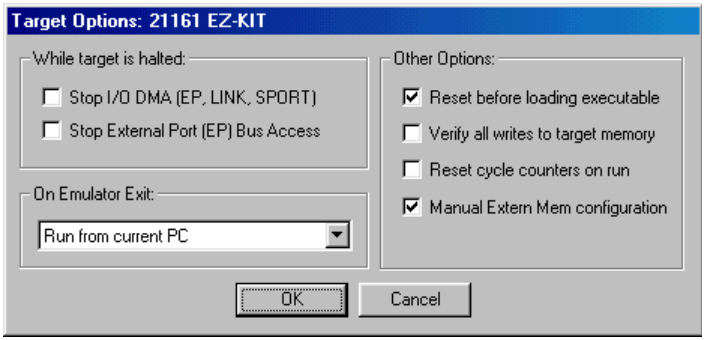


Figure 2-1. Target Options Dialog Box

While Target is Halted and On Emulator Exit Options

This target option controls the processor's behavior when VisualDSP++ relinquishes DSP control (for example, when exiting VisualDSP++). The options are detailed in Table 2-4 and Table 2-5.

Table 2-4. While Target is Halted Options

Option	Description
Stop I/O DMA	Stops IO DMAs in emulator space. This option disables DMA requests when the emulator has control of the DSP. Data in the **EP**, **LINK**, or **SPORT DMA** buffers are held there unless the internal **DMA** request was already granted. This option holds off incoming data and ceases outgoing data. Because SPORT-receive data cannot be held off, it is lost, and the overrun bit is set. The direct write buffer (internal memory write) and the EP pad buffer are allowed to flush any remaining data to internal memory.

Other Options

Table 2-6 describes other available target options.

Table 2-5. On Emulator Exit Options

Option	Description
On Emulator Exit	Determines the state the DSP is left in when the emulator relinquishes control of the DSP: **Reset DSP and Run** causes the DSP to reset and begin execution from its reset vector location. **Run from current PC** causes the DSP to begin running from its current location.

Table 2-6. Other Target Options

Option	Description
Reset before loading executable	Resets registers before loading a DSP executable. Clear this option when DSP registers must not change to their reset values when a file load occurs.
Verify all writes to target memory	Validates all memory writes to the DSP. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files since VisualDSP++ does not perform the extra reads that are required to verify each write.
Reset cycle counters on run	Resets the cycle count registers to zero before a **Run** command is issued. Select this option to count the number of cycles executed between breakpoints in a program.
Manual Extern Mem configuration	Disables the automatic configuration of the SDRAM registers (done through the debugger).

Core Hang Conditions

Certain peripheral devices, such as host ports, DMA, and link ports, can hold off the execution of processor instructions. This is known as a hung condition and commonly occurs when reading from an empty port or writing to a full port. If an attempt to halt the processor is made during one of these conditions, the EZ-KIT Lite may encounter a core hang.

Normally, a core hang can be cleared by the board using a special clear/abort bit. However, there are cases in which it is desirable or possible not to clear the core hang. Sometimes it is desirable to wait for the core hang to clear itself, such as when waiting for a host processor to read or write data. In other cases, it is not possible to clear the core hang, and a DSP reset must occur to continue the debugging session.

Table 2-7 describes the EZ-KIT Lite's core hang operations.

Table 2-7. Core Hang Operations

Option	Description
Abort	Abort the hung operation. This causes the offending instruction to be aborted in the pipeline.
Retry	Allows you to remedy the hung operation. For example, if a host processor is holding off the DSP, you can cause the host to clear the hung condition.
Ignore	Performs a software reset on the target board.
Clear	Aborts the hung operation. This causes the offending instruction to be aborted in the pipeline.
Acknowledge	Allows you to remedy the hung operation. For example, if a host processor is holding off the DSP, you can cause the host to clear the hung condition.
Reset	Performs a software reset on the target board.

Hardware Breakpoints

Hardware breakpoints work similarly to watchpoints. Set hardware breakpoints on:

- Data transfers within a user-defined memory range
- Instructions
- Register reads and writes

To enable hardware breakpoints for ADSP-21161N DSPs:

1. From the **Settings** menu, choose **Hardware Breakpoints**.
2. The **Hardware Breakpoints** dialog box appears. The dialog box has three tabbed pages: **Data**, **Instruction**, and **Other** (Figure 2-2).

Figure 2-2. Hardware Breakpoints Dialog Box

Refer to the following sections for information about hardware breakpoints.

- "Common Hardware Breakpoint Attributes" on page 2-13
- "Global Hardware Breakpoint Options" on page 2-13
- "Data Hardware Breakpoints" on page 2-15
- "Instruction Hardware Breakpoints" on page 2-16
- "Other Breakpoints" on page 2-17
- "Tips and Tricks Using Hardware Breakpoints" on page 2-18

Common Hardware Breakpoint Attributes

Each of the three tabs in the **Hardware Breakpoints** dialog box has common attributes. The common attributes are described in Table 2-8.

Global Hardware Breakpoint Options

For ADSP-21161N DSPs, the options listed in Table 2-9 apply to all hardware breakpoints, regardless of their type.

Table 2-8. Common Hardware Breakpoint Attributes

Attribute	Description
Enable	Enables each individual breakpoint.
Start Address **End Address**	Specify inclusive start and end addresses. Each pair of addresses sets up an address range for the particular breakpoint.
Exclusive	Enables breaks outside of the specified (inclusive) address range.
Mode	**Data** page and **Other** page only. This option specifies the modes that trigger hardware breakpoints. The available choices are: **Disabled**—disables the breakpoint **On Write**—triggers the breakpoint on any write operation to the specified address range **On Read**—triggers the breakpoint on any read operation from the specified address range **Any Access**—triggers the breakpoint on any read or write access to the specified address range.

Table 2-9. Global Hardware Breakpoint Options

Option	Description
Skip N Breakpoint Events	Specifies the number of breakpoint events to be ignored before stopping the processor. Each time a hardware breakpoint condition occurs, the count decrements. When the count reaches zero (0), the DSP processes the hardware break. Use this option to count the number of times a break operation occurs. Breakpoints within the group are ORed together to create this condition.
Restore Skip Count on Break	Enables skip-count decrement as specified in **Skip N Breakpoint Events**.
Restore Skip Count on Break	Causes the emulator to restore the Skip Count to the value at program RESTART. Otherwise, the Skip Count remains at its current value.
AND All Breakpoints	ANDs the interrupts to form the composite interrupt. Normally, the group interrupts are ORed to create a composite interrupt.

Data Hardware Breakpoints

For ADSP-21161N DSPs, use data breakpoints to break on accesses to internal memory, IOP registers, the external port (EP), and multiprocessor memory space (MMS).

The following actions trigger a data breakpoint:

- `DAG1` access
- `DM()` modifier access

The two data breakpoints are ORed to generate a single data breakpoint condition.

The **Data** page of the **Hardware Breakpoints** dialog box, which permits the specification of two data breakpoints, is shown in Figure 2-3.

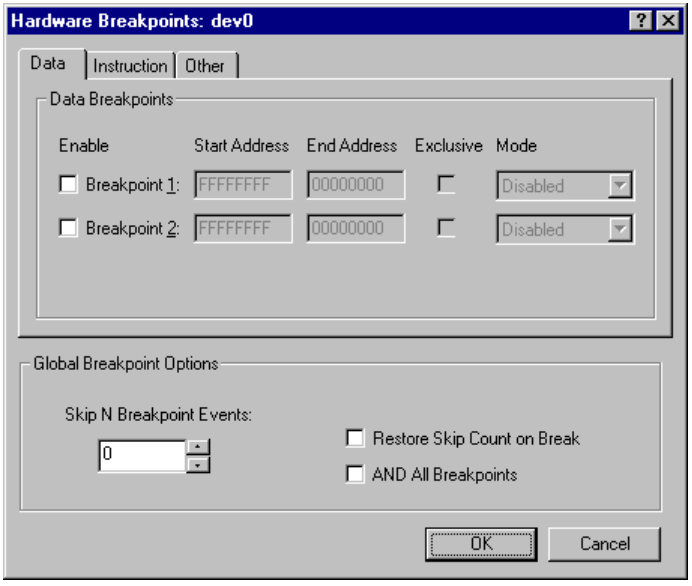


Figure 2-3. Data Page of Hardware Breakpoints Dialog Box

Instruction Hardware Breakpoints

For ADSP-21161N DSPs, an instruction breakpoint occurs when an instruction is executed within one of the specified address ranges. The four individual instruction breakpoints are ORed to generate a single instruction breakpoint condition.

Shown below is the **Instruction** page of the **Hardware Breakpoints** dialog box, which permits the specification of four individual instruction breakpoints.

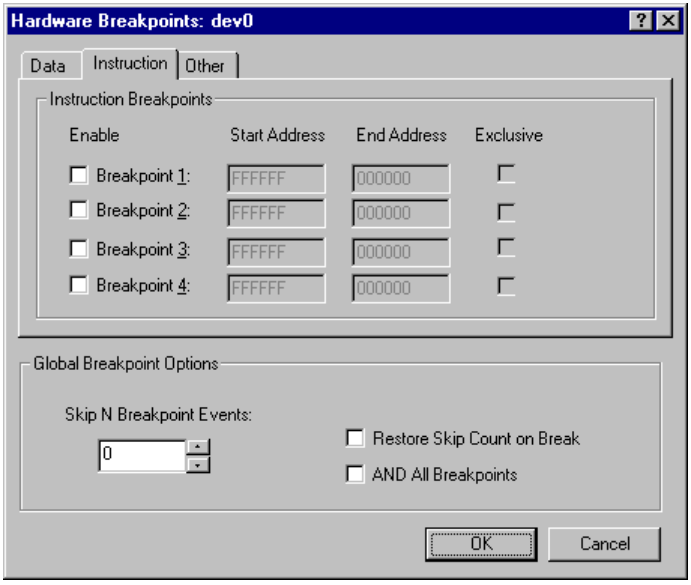


Figure 2-4. Instruction Page of Hardware Breakpoints Dialog Box

Other Breakpoints

For SHARC DSPs, the **Other** page of the **Data Breakpoints** dialog box permits the specification of hardware breakpoints triggered by access to PM data, IO, or the external port.

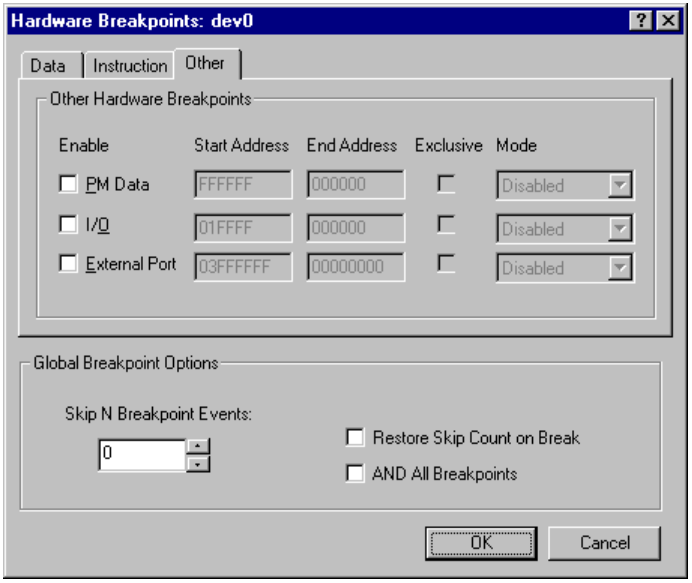


Figure 2-5. Other Page of Hardware Breakpoints Dialog Box

Table 2-10. Other Hardware Breakpoint Options

Option	Description
PM DataEvents	Enables PM data breakpoints. PM data breakpoints are similar to data breakpoints (Data page), except accesses that trigger a PM breakpoint are made by DAG2 or the PM() modifier. Like data breakpoints, PM data breakpoints cause a break on accesses to internal memory, IOP registers, the external port (EP), and multiprocessor memory space (MMS).
I/O	Enables IO breakpoints. IO breakpoints are triggered by accesses made on the IO Address Bus. Use an IO breakpoint to break on accesses made during DMA transfers, MMS accesses, and Host accesses.

Table 2-10. Other Hardware Breakpoint Options (Cont'd)

Option	Description
External Port	Enables external port breakpoints.External port (EP) breakpoints are triggered by accesses made through the External Port. Use an EP breakpoint to break on accesses made to any external device that may be tied to the EP, such as external memory.
AND All Breakpoints	ANDs the interrupts to form the composite interrupt. Normally, the group interrupts are ORed to create a composite interrupt.

Tips and Tricks Using Hardware Breakpoints

Be aware of the following tips and tricks when using hardware breakpoints on ADSP-21161N processors.

Latency

For SHARC processors, hardware breakpoints do not assert until two (2) instruction cycles after the actual break condition occurs

Restrictions

When using hardware breakpoints, do not place breaks at any address where a `JUMP`, `CALL`, or `IDLE` instruction would be illegal.

Do not place breaks in the last few instructions of a `DO LOOP` or in the delay slots of a delayed branch. For more information on these illegal locations, refer to your DSP's Hardware Reference.

Setting a Breakpoint on a Single Address

To set a breakpoint on a single address, set the **Start Address** equal to the **End Address**.

Restricted Software Breakpoints

The EZ-KIT Lite development system restricts breakpoint placement when certain conditions are met. That is, under some conditions, breakpoints cannot be placed effectively. Such conditions depend on bus architecture, pipeline depth, and ordering of the EZ-KIT Lite and its target processor.

3 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-21161N EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 3-2
  Describes the configuration of the ADSP-21161N EZ-KIT Lite board and explains how the board components interface with the processor.
- "Jumper Settings" on page 3-5
  Shows the location and describes the function of the on-board jumpers.
- "LEDs and Push Buttons" on page 3-13
  Shows the location and describes the function of the LEDs and push buttons.
- "Connectors" on page 3-16
  Shows the location and gives the part number for the on-board connectors. Also, the manufacturer and part number information is given for the mating parts.
- "Specifications" on page 3-21
  Provides the board's measurements and power supply specifications.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

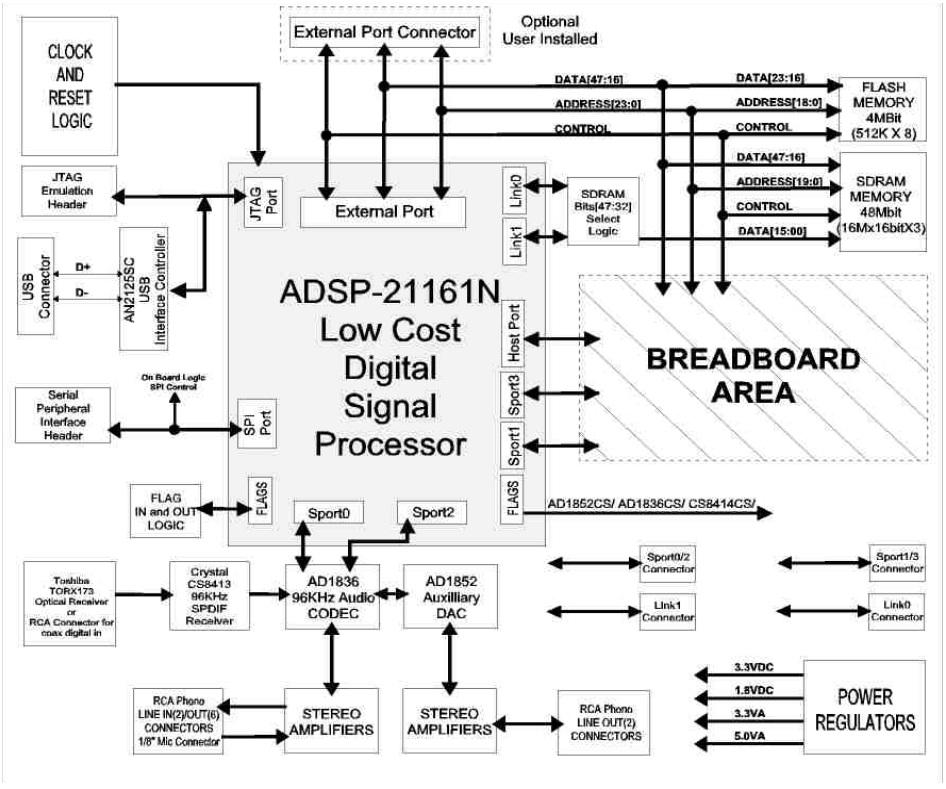


Figure 3-1. System Architecture Block Diagram

The ADSP-21161N processor's core voltage is 1.8V, and the external interface voltage is 3.3V.

A 25 MHz through-hole oscillator supplies the input clock to the processor. Footprints are provided on the board for a surface-mount oscillator and a through-hole crystal for alternate user-installed clocks. The speed at

which the core operates is determined by the location of the clock mode jumper (JP21) as described on page 3-11. By default, the processor core runs at 100 MHz.

External Port

The External Port (EP) of the processor connects to a 512K x 8-bit Flash memory. The Flash memory connects to the boot memory select (~BMS) pin and the memory select 1 (~MS1) pin. The connection allows the Flash memory to be used to boot the processor as well as to store information during normal operation.

The external memory interface also connects to 1M x 48-bit SDRAM memory. The SDRAM memory connects to the memory select 0 (~MS0) pin. Refer to "SDRAM Disable Jumper (JP1)" on page 3-5 for information on how to configure the width of the SDRAM. Refer to "Using SDRAM Memory" on page 2-3 for a summary of the processor's memory map.

Some of the address, data, and control signals are available externally via two off-board connectors. The EP connectors' pinout (P9 and P10) can be found in Appendix B, "Schematics".

Host Processor Interface (HPI)

The Host Port Interface (HPI) signals are brought to an unpopulated off-board connector (P9). This allows the HPI to interface with a user application. The pinout of the host port connector can be found in Appendix B, "Schematics".

SPORT Audio Interface

SPORT0 and SPORT2 are connected to the AD1836 codec (U10). A 3.5 mm stereo jack and four RCA mono jacks facilitate an audio input, while a 3.5 mm stereo jack and eight RCA mono jacks facilitate an audio output.

The codec contains two input channels. One channel connects to a 3.5 mm stereo jack and two RCA jacks. The 3.5 mm stereo jack connects to a microphone. The two RCA jacks can connect to a LINE-OUT from an audio device. You can supply an audio input to the codec microphone input channel (MIC1) or to the LINE_IN input channel. The jumper settings of JP11 determine whether the LINE_IN channel of the codec is driven by the P6 connector or by the P7 connector.

SPI Audio Interface

The SPI port is connected to the AD1836 and AD1852. The SPI port is used for writing and reading the control registers of the audio devices.

Breadboard Area

Use the breadboard area to add external circuitry to:

- All board voltages and grounds
- Package footprints:
  - 1x SOIC16
  - 1x SOIC20
  - 4x SOT23-6
  - 1x PSOP44
  - 2x SOT23
  - 27x 0805

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory, as well as the special function registers, through a 14-pin header.

For a detailed description of the interface's connectors, see EE-68 published on the Analog Devices website. For more information, see "JTAG Connector (P12)" on page 3-19. For more information about available emulators, contact Analog Devices (see "Product Information").

Jumper Settings

This section describes the function of all the jumpers. Figure 3-2 shows the locations of all the jumpers.

SDRAM Disable Jumper (JP1)

The JP1 jumper is used to enable or disable the third SDRAM device. When the jumper is installed, the ADSP-21161N can access the SDRAM as 48-bit-wide external memory.

The upper 16 bits of data are multiplexed with the Link Ports and the external data bus; therefore, when the jumper is installed, the Link Ports are not available. To use the Link Ports, the JP1 jumper must be removed.

SPDIF Selection Jumper (JP2)

The JP2 jumper is used select the SPDIF input to the CS8414 digital audio receiver. When the jumper is configured for an optical connection, the TOSLINK optical input connector (P4) should be used. When the jumper is configured for a coax connection, the RCA input connector (P5) should be used.

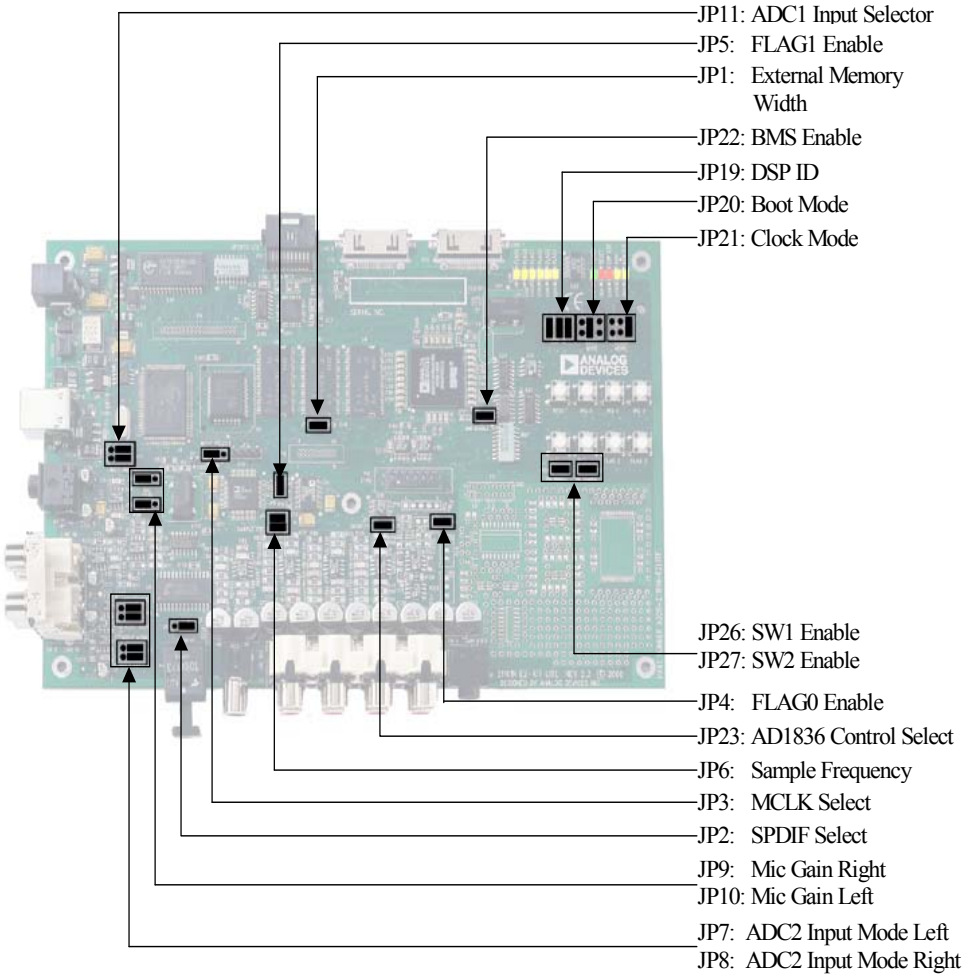


Figure 3-2. Jumper Locations

MCLK Selection Jumper (JP3)

The JP3 jumper is used to select the MCLK source for the AD1836 and AD1852.

Table 3-1. SPDIF Modes

Jumper Location	Mode
1 and 2	**Optical (factory default)**
2 and 3	Coax

Table 3-2. MCLK Selection

Jumper Location	MCLK Source
1 and 2	**Audio Oscillator (12.288 MHz) (factory default)**
2 and 3	Derived clock from SPDIF Stream

FLAG0 Enable Jumper (JP4)

In standard configuration, FLAG0 is connected to the AD1836 and used as a select for the SPI port. This jumper should be removed to use the push button switch or the signal on the expansion connector (P10). Once the jumper is removed, the SPI can no longer communicate with the AD1836.

FLAG1 Enable Jumper (JP5)

In standard configuration, FLAG1 is connected to the AD1852 and used as a select for the SPI port. The JP5 jumper should be removed to use the push button switch or the signal on the expansion connector (P10). Once the jumper is removed, the SPI can no longer communicate with the AD1852.

Sample Frequency Jumper (JP6)

The JP6 jumper is used to select the sample frequency for the AD1852 device. Table 3-3 shows the valid frequency modes.

Table 3-3. Sample Frequencies

Jumper Location	Sample Frequency
None installed	Not allowed
3 and 4	192 kHz (2x Interpolator)
1 and 2	96 kHz (4x Interpolator)
1 and 2, 3 and 4	**48 kHz (8x Interpolator) (factory default)**

ADC2 Input Mode Selection Jumpers (JP7–8)

The JP7 and JP8 jumpers control the input mode to ADC2 on the AD1836 (see Table 3-4). In high-performance mode, the signal is routed straight in to the ADC. In PGA mode, the signal goes through a multiplexer and a programmable gain amplifier inside of the codec.

Table 3-4. ADC Input Mode

Jumper Location	Input Mode
3 and 5, 4 and 6	**PGA (factory default)**
1 and 3, 2 and 4	High Performance

MIC Gain Selection Jumpers (JP9–10)

The JP9 and JP10 jumpers are used to select the pre-amp gain for the microphone circuit (see Table 3-5). The gain for the left and right channel should be configured the same.

Table 3-5. MIC Pre Amp Gain

Jumper Position	Gain
Not Installed	0 dB

Table 3-5. MIC Pre Amp Gain (Cont'd)

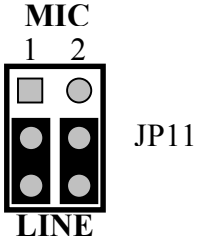
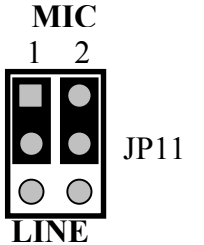
Jumper Position	Gain
1 and 2	20 dB
2 and 3	**40 dB (factory default)**

ADC1 Input Selection Jumper (JP11)

The JP11 jumper is used to select the input source for ADC2. If the input source for ADC2 is LINE-IN, then the RCA connector P6 should be used. If the input source for ADC2 is a microphone, then the mini stereo plug P7 should be used. If a microphone is used, the gain of the circuit may be increased, as described in "MIC Gain Selection Jumpers (JP9–10)" on page 3-8.

When the JP11 jumpers are between pins 1 and 3 and between pins 2 and 4, the connection is to P7. When the jumpers are between pins 3 and 5 and between pins 4 and 6, the connection is to P6. The jumper settings are illustrated in Table 3-6). (The words MIC and LINE are on the board as a reference.)

Table 3-6. Audio Input Jumper Settings

Microphone Input	Stereo LINE_IN (Default)
	

Processor ID Jumper (JP19)

The JP19 jumper is used to select a different ID for the processor. During typical operation of the EZ-KIT Lite board, there is only a single DSP in the system. The jumper should be set to the single processor setting. When a second processor is attached to the board though the link port, these jumpers should be changed to configure one board for processor 1 and the other board for processor 2. System configuration options are shown in Table 3-7.

Table 3-7. Processor ID Modes

Jumper Position	Description
1 and 2, 3 and 4, 5 and 6	**Single processor (default)**
3 and 4, 5 and 6	Processor 1
1 and 2, 5 and 6	Processor 2
Other	Invalid

Boot Mode Selection Jumper (JP20)

The JP20 jumper determines how the ADSP-21161N processor boots. Table 3-8 shows the jumper setting for the boot modes.

Table 3-8. Boot Mode Select Jumper (JP20) Settings

EBOOT Pins 1 & 2	LBOOT Pins 3 & 4	BMS Pins 5 & 6	Boot Mode
Not installed	**Installed**	**Not installed (output)**	**EPROM BOOT (default)**
Installed	Installed	Not installed (input)	Host Processor Boot
Installed	Not installed	Installed (input)	Serial Boot via SPI

Table 3-8. Boot Mode Select Jumper (JP20) Settings (Cont'd)

EBOOT Pins 1 & 2	LBOOT Pins 3 & 4	BMS Pins 5 & 6	Boot Mode
Installed	Not installed	Not installed (input)	Link Port Boot
Installed	Installed	Installed (input)	No Boot
Not installed	Not installed	Installed (input)	Reserved

Clock Mode Selection Jumper (JP21)

The JP21 jumper controls the speed for the core and external port of the ADSP-21161N processor. The frequency supplied to CLKIN of the DSP may be changed by removing the 25 MHz oscillator (U24) that is shipped with the board and replacing it with a different oscillator or crystal (Y2). A clock mode and frequency should be selected so that the minimum and maximum specs of the ADSP-21161N processor are not exceeded. For more information on clock modes, see the *ADSP-21161 SHARC Processor Hardware Reference*. Table 3-9 shows the jumper setting for the clock modes.

Table 3-9. Clock Mode Selections

CLKDBL Pins 1 & 2	CLK_CFG1 Pins 3 & 4	CLK_CFG0 Pins 5 & 6	Core Clock Ratio	External Port Clock Ratio
Not installed	Installed	Installed	2:1	1x
Not installed	Installed	Not installed	3:1	1x
Not installed	**Not installed**	**Installed**	**4:1**	**1x (default)**
Installed	Installed	Installed	4:1	2x
Installed	Installed	Not installed	6:1	2x
Installed	Not installed	Installed	8:1	2x

~BMS Enable Jumper (JP22)

The JP22 jumper is used to control the routing of the Boot Memory Select (~BMS) signal. When the jumper is installed, the ~BMS signal is routed to the Flash memory interface and can be used for reading, writing, and booting. The jumper should be installed when using EPROM boot mode. The jumper should be removed when using the serial boot or no-boot mode. If the jumper remains "ON" in serial boot or no-boot modes, the ~BMS signal is grounded, and the flash memory is selected.

AD1836 Control Selection Jumper (JP23)

The AD1836 control registers are programmed through an SPI port. The SPI port can be configured to be connected to the processor's SPI port or SPORT1. When the jumper is installed at JP23, the AD1836 SPI port is connected to SPORT1 of the processor. When the jumper is removed, the AD1836 SPI port connects to the processor's SPI port. By default, the jumper is installed.

SW1 Enable Jumper (JP26)

The SW1 push button is attached though a driver to FLAG0 of the processor. To disconnect the driver from FLAG0 (for example, to use FLAG1 as an output), remove JP26.

SW2 Enable Jumper (JP27)

The SW2 push button is attached though a driver to FLAG1 of the processor. To disconnect the driver from (for example, to use FLAG1 as an output), remove JP27.

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 3-3 shows the locations of the LEDs and push buttons.

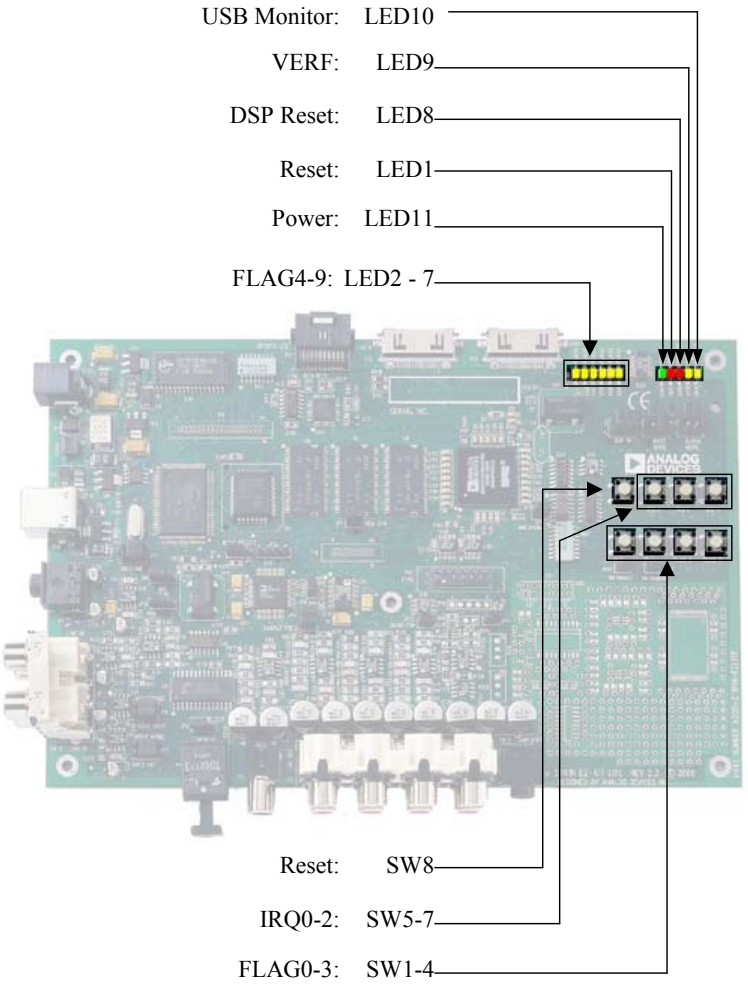


Figure 3-3. LED and Push Button Locations

Reset LEDs (LED1 and LED8)

When LED1 is lit, the master reset of all the major ICs is active.

When LED8 is lit, the ADSP-21161N processor (U1) is being reset. The USB interface resets the processor during USB communication initialization.

FLAG LEDs (LED2–7)

The FLAG LEDs connect to the processor's flag pins (FLAG4-9). The LEDs are active HIGH and are lit by an output of "1" from the processor. Refer to "LEDs and Push Buttons" on page 3-13 for more information on how to use the programmable flags to program the DSP. Table 3-10 shows the FLAG signals and the corresponding LEDs.

Table 3-10. FLAG LEDs

FLAG Pin	LED Reference Designator
FLAG4	LED7
FLAG5	LED6
FLAG6	LED5
FLAG7	LED4
FLAG8	LED3
FLAG9	LED2

VERF LED (LED9)

The VERF LED indicates that there is a possible error in the audio stream of the CS8414 digital receiver. The error may occur when digital audio cables disconnect from the optical or coaxial SPDIF connectors.

USB Monitor LED (LED10)

The USB monitor LED (LED10) indicates that USB communication has been initialized successfully, and you may connect to the processor using a VisualDSP++ EZ-KIT Lite session. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see "Installing EZ-KIT Lite USB Driver" on page 1-6).

Power LED (LED11)

When LED11 is lit (green), it indicates that power is being properly supplied to the board.

Programmable FLAG Push Buttons (SW1–4)

Four push buttons (SW1-4) are provided for general-purpose user input. The push buttons connect to the processor's FLAG pins. The push buttons are active "HIGH" and, when pressed, send a High (1) to the processor. Refer to "Using FLAG Pins" on page 2-5 for more information. The push button reference designators and corresponding FLAGs are summarized in Table 3-11.

Table 3-11. FLAG Switches

FLAG Pin	Push Button Reference Designator	FLAG Pin	Push Button Reference Designator
FLAG0	SW1	FLAG2	SW3
FLAG1	SW2	FLAG3	SW4

Interrupt Push Buttons (SW5–7)

Three push buttons are provided for general-purpose user interrupts. SW5-SW7 connect to the processor's programmable FLAG pins. The push buttons are active "HIGH" and, when pressed, send a High (1) to the

processor. Refer to "Using FLAG Pins" on page 2-5 for more information. The push button reference designators and corresponding interrupt signals are summarized in Table 3-12.

Table 3-12. Interrupt Switches

Interrupt Signal	Push Button Reference Designator
IRQ0	SW5
IRQ1	SW6
IRQ2	SW7

Board Reset Push Button (SW8)

The RESET push button (SW8) resets all of the ICs on the board. During reset, the USB interface is automatically reinitialized.

Pressing the RESET push button (SW8) while VisualDSP++ is running disrupts communication and causes errors in the current debug session. VisualDSP++ must be closed and re-opened.

Connectors

This section describes the connector functionality and provides information about mating connectors. Figure 3-4 shows the connector locations.

USB Connector (P2)

The USB connector (P2) is a standard Type B USB receptacle.

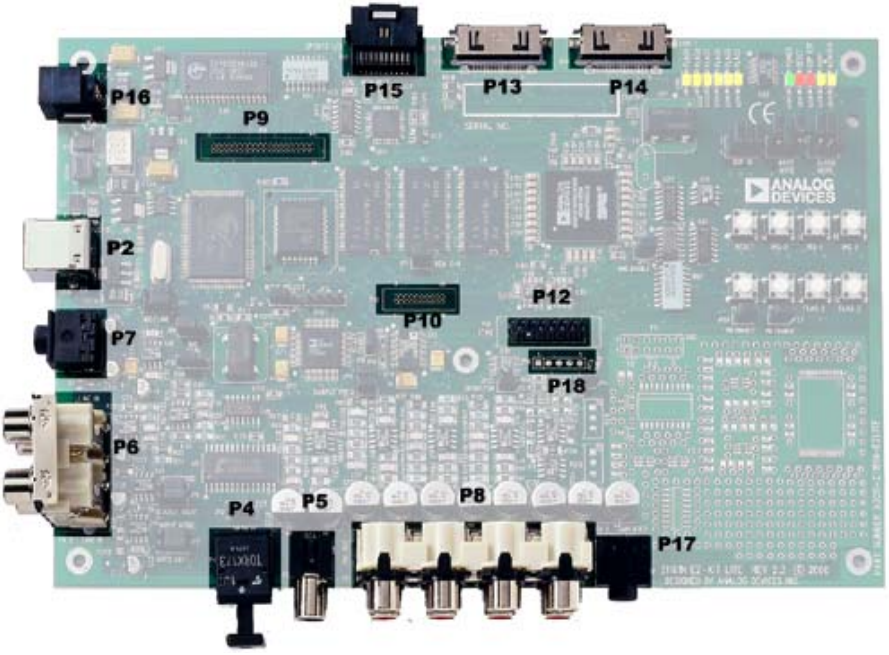


Figure 3-4. Connector Locations

Part Description	Manufacturer	Part Number
Type B USB receptacle	Mill-Max	897-30-004-90-000
	Digi-Key	ED90003-ND
Mating Connector (provided with the EZ-KIT Lite)		
USB cable	Assmann	AK672-5
	Digi-Key	AK672-5ND

Audio Connectors (P4–8, P17)

There are two 3.5 mm stereo audio jacks, 13 RCA jacks, and one optical connector.

Part Description	Manufacturer	Part Number
3.5 mm stereo jack (P7 and P17)	Shogyo	SJ-0359AM-5
RCA Jacks (P6)	SWITCHCRAFT	PJRAS2X2S01
RCA Jacks (P8)	SWITCHCRAFT	PJRAS4X2U01
TORX (P4)	TOSHIBA	TORX173
Coaxial (P5)	SWITCHCRAFT	PJRAN1X1U01
Mating Connectors		
3.5mm stereo plug to 3.5mm stereo cable (P7 and P17)	Radio Shack	L12-2397A
Two channel RCA interconnect cable (P6 and P8)	Monster Cable	BI100-1M
Digital Fiber-Optic Cable (P4)	Monster Cable	ILS100-1M
Digital Coaxial Cable (P5)	Monster Cable	IDL100-1M

External Port Connector (P9)

A 40-pin 0.05' spacing connector provides access to some of the processor's External Port signals. By default, this connector is not populated.

Part Description	Manufacturer	Part Number
40-pin 0.05' (male)	Samtec	FTSH-120-01-F-D-K
Mating Connector		
Female to female cable	Samtec	FFSD-20-D-5.000-01-N

Host Processor Interface Connector (P10)

A 20-pin 0.05' spacing connector provides access to some of the processor's External Port signals. By default, this connector is not populated.

Part Description	Manufacturer	Part Number
20-pin 0.05' (male)	Samtec	FTSH-110-01-F-D-K
Mating Connector		
Female to female cable	Samtec	FFSD-10-D-5.000-01-N

JTAG Connector (P12)

The JTAG header (P12) is the connecting point for a JTAG in-circuit emulator pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

Part Description	Manufacturer	Part Number
14-pin IDC Header (P12)	Berg	54102-T08-07

Link Port Connectors (P13–14)

Each link port is connected to a 26-pin connector. Refer to EE-106 found on the ADI website at http://www.analog.com for more information about the link port connectors.

Part Description	Manufacturer	Part Number
26 position connector	Honda	RMCA-26JL-AD
Mating Connector		
Cable connector	Honda	RMCA-E26F1S-A
Shroud	Honda	RMCA-E26L1A
Coaxial cable	Gore	DXN2132

SPORT1 and SPORT3 Connector (P15)

SPORT1 and SPORT3 are connected to a 20-pin connector.

Part Description	Manufacturer	Part Number
20 position AMPMODU system 50 receptacle	AMP	104069-1
Mating Connector		
20 position AMPMODU system 20 connector	AMP	2-487937-0
20 position AMPMODU system 20 connector (w/o lock)	AMP	2-487938-0
Flexible film contacts (20 per connector)	AMP	487547-1

Power Connector (P16)

The power connector (P16) provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm Power Jack (P16)	SWITCHCRAFT	RAPC712
	Digi-Key	SC1152-ND

Part Description	Manufacturer	Part Number
Mating Power Supply (shipped with EZ-KIT Lite)		
5V Power Supply	CUI Stack	DTS070175SUDC-p6-SZ

Specifications

This section provides the requirements for powering the board.

Power Supply

The power connector supplies DC power to the EZ-KIT Lite board. Table 3-13 shows the power supply specifications.

Table 3-13. Power Supply Specifications

Terminal	Connection
Center pin	+7V@2 amps
Outer Ring	GND

Board Current Measurements

The ADSP-21161N EZ-KIT Lite board provides two zero-ohm resistors that may be removed to measure current draw. Table 3-14 shows the resistor number, the voltage plane, and a description of the components on the plane.

Table 3-14. Current Measurement Resistors

Resistor	Voltage Plane	Description
R168	VDDINT	Core Voltage of the DSP
R169	VDDEXT	IO Voltage of the DSP

A BILL OF MATERIALS

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
1	1	M29W040 PLCC32 FLASH-512K-X-8-3V	U5	ST MICRO	M29W040B120K6
2	2	74LVC14A SOIC14 HEX-INVER-SCHMITT-TRIGGER	U21-22	TI	74LVC14AD
3	3	MT48LC1M16A1TG TSOP50 1MX16-SDRAM-143MHZ	U2-4	MICRON	MT48LC1M16A1TG-7S
4	1	CS8414 SOIC28 96KHZ-DIGI-TAL-AUDIO-RECVR	U8	CIRRUS LOGIC	CS8414
5	1	CY7C64603-128 PQFP128 USB-TX/RX MICROCON-TROLLER	U6	CYPRESS	CY7C64603-128NC
6	1	MMBT4124 SOT-23 NPN TRANSISTOR 1A	Q2	FAIRCHILD	MMBT4124
7	1	MMBT4401 SOT-23 NPN TRANSISTOR 200MA	Q1	FAIRCHILD	MMBT4401
8	2	74LVC00AD SOIC14	U9, U27	PHILIPS	74LVC00AD
9	1	CY7C1019BV33-15VC SOJ32 128K X 8 SRAM	U30	CYPRESS	CY7C1019BV33-12VC

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
10	1	AD8532AR SOIC8 DUAL AMP 250MA	U29	ANALOG DEVICES	AD8532AR
11	1	12.288MHZ 1/2 OSC001	U25	DIG01	SG-8002DC-PCC-ND 12.288MH
12	2	SN74AHC1G02 SOT23-5 SINGLE-2 INPUT-NOR	U34,U37	TI	SN74AHC1G02DBVR
13	1	SN74LV164A SOIC14 8-BIT-PARALLEL-SERIAL	U33	TI	SN74LV164AD
14	1	CY7C4201V-15AC TQFP32 64-BYTE-FIFO	U32	CYPRESS	CY7C4201V-15AC
15	1	25MHZ 1/2 OSC01 OSC	U24	DIGI-KEY	SG-8002DC-PCC-ND
16	1	12.0MHZ THR OSC006 CRYSTAL	Y1	DIG01	300-6027-ND
17	1	21161 24LC00 U7"" SEE 1000127	U7	MICROCHIP	24LC00-SN
18	2	1000pF 50V 5% 1206 CERM	C85-86	AVX	12065A102JAT2A
19	8	2200pF 50V 5% 1206 NPO	C40, C46, C52, C58, C64, C70, C76, C82	AVX	12065A222JAT050
20	1	ADM708SAR SOIC8 VOLTAGE-SUPERVISOR	U26	ANALOG DEVICES	ADM708SAR
21	1	AD1852 SSOP28 MULTI-BIT-SIGMA-DELTA-DAC	U11	ANALOG DEVICES	AD1852JRS
22	1	AD1836AS MQFP52 MULTI-CHAN-NEL-96KHZ-CODEC	U10	ANALOG DEVICES	AD1836AS

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
23	1	ADSP-21161NKCA100 PBGA225 1MM SPACING REV. X1.2	U1	ANALOG DEVICES	ADSP-21161NCCA100
24	1	ADP3338AKC-33 SOT-223 3.3V-1.0AMP REGULATOR	VR2	ANALOG DEVICES	ADP3338AKC-3.3
25	2	ADP3339AKC-5 SOT-223 5V-1.5A REGULATOR	VR1, VR5	ANALOG DEVICES	ADP3339AKC-5-REEL
26	1	ADP3338AKC-18 SOT-223 1.8V-1A REGULATOR	VR3	ANALOG DEVICES	ADP3338AKC-1.8
27	10	LMV722M SOIC8 DUAL AUDIO OP AMP	U12-20, U28	NATIONAL SEMI	LMV722M
28	3	4.7uF 25V 10% C TANT	CT23-25	AVX	TAJC475K025R
29	1	PWR 2.5MM_JACK CON005 RA	P16	SWITCH-CRAFT	SC1152-ND12
30	1	USB 4PIN CON009 USB	P2	MILL-MAX	897-30-004-90-000000
31	1	TORX173 6PIN CON008 FIBER OPTIC REV MODULE	P4	TOSHIBA	TORX173
32	1	RCA 4X2 CON011 RA	P8	SWITCH-CRAFT	PJRAS4X2U01
33	1	RCA 1X1 CON012 BLK	P5	SWITCH-CRAFT	PJRAN1X1U01
34	1	RCA 2X2 CON013	P6	SWITCH-CRAFT	PJRAS2X2S01
35	2	LNKPRT 12X2 CON010	P13-14	HONDA (TSUSHINK)	RMCA-EA26LMY-0M03-A

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
36	1	.05 10X2 CON014 RA	P15	AMP	104069-1
37	8	SPST-MOMENTARY SWT013 6MM	SW1-8	PANASONIC	EVQ-PAD04M
38	1	DIP8 SWT016	SW9	C&K	CKN1365-ND
39	1	10 1/8W 5% 1206	R2	PANASONIC	P10ECT-ND
40	6	0.00 1/8W 5% 1206	R153, R154, R168-169, R217, R218	YAGEO	0.0ECT-ND
41	8	AMBER-SMT LED001 GULL-WING	LED2-7, LED9-10	PANASONIC	LN1461C-TR
42	8	330pF 50V 5% 805 NPO	C36, C42, C48, C54, C60, C66, C72, C78	AVX	08055A331JAT
43	80	0.01uF 100V 10% 805 CERM	C2, C6-7, C91-149, C154-155, C165-171, C184-C186, C174-179	AVX	08051C103KAT2A
44	11	0.22uF 25V 10% 805 CERM	C156-164, C172, C183	AVX	08053C224FAT
45	16	0.1uF 50V 10% 805 CERM	C1,C5,C9-11, C33,C87-90, C150-153, C173,C180	AVX	08055C104KAT

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
46	8	0.001uF 50V 5% 805 NPO	C14-15, C19-20, C24-25, C29-30	AVX	08055A102JAT2A
47	5	10uF 16V 10% C TANT	CT19-22, CT36	SPRAGUE	293D106X9025C2T
48	47	10K 100MW 5% 805	R3-4,R6,R13, R15,R17-20, R124,R126,R 128,R130, R132,R134, R136, R148-149, R151, R155-164, R175, R177-181, R183,R190, R171,R172, R174, R185-187, R193-194, R219-220	AVX	CR21-103J-T
49	4	33 100MW 5% 805	R1, R150, R176, R152	AVX	CR21-330JTR
50	5	4.7K 100MW 5% 805	R184, R188, R189, R191, R165	AVX	CR21-4701F-T
51	11	680 100MW 5% 805	R137-147	AVX	CR21-6800F-T
52	1	1M 100MW 5% 805	R12	AVX	CR21-1004F-T

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
53	1	475 100MW 5% 805	R16	AVX	CR21-471J-T
54	1	1.5K 100MW 5% 805	R7	AVX	CR21-1501F-T
55	2	2.00K 1/8W 1% 1206	R49-50	DALE	CRCW1206-2001FRT1
56	10	49.9K 1/8W 1% 1206	R66, R74, R82, R90, R98, R106, R114, R122, R192, R206	AVX	CR32-4992F-T
57	2	2.21K 1/8W 1% 1206	R10-11	AVX	CR32-2211F-T
58	24	100pF 100V 5% 1206 NPO	C12, C16-17, C21-22, C26-27, C31, C35, C38, C41, C44, C47, C50, C53, C56, C59, C62, C65, C68, C71, C74, C80, C77	AVX	12061A101JAT2A
59	5	10uF 16V 10% B TANT	CT1-4, CT11	AVX	TAJB106K016R
60	1	22K 100MW 5% 805	R216	AVX	CR21-223J-T
61	7	100 100MW 5% 805	R123, R125, R127, R129, R131, R133, R135	AVX	CR21-101J-T

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
62	8	220pf 50V 10% 1206 NPO	C39, C45, C51, C57, C63, C69, C75, C81	AVX	12061A221JAT2A
63	1	1000 100MHZ 1.5A FER002 0.06 CHOKE	FER13	MURATA	PLM250S40T1
64	2	2A S2A_RECT DO-214AA SILICON RECTIFIER	D1-2	GENER-ALSEMI	S2A
65	11	600 100MHZ 500MA 1206 0.70 BEAD	FER1-11	DIGI-KEY	240-1019-1-ND
66	8	237 1/8W 1% 1206	R23, R27, R30, R34, R40-41, R47-48	KOA	P11.0FCT-ND
67	4	750K 1/8W 1% 1206	R25, R32, R38, R45	KOA	RK73H2BT7503F
68	16	5.76K 1/8W 1% 1206	R21, R22, R24, R26, R28-29, R31, R33, R35-37, R39, R42-44, R46	DALE	CRCW12065761FRT1
69	8	11.0K 1/8W 1% 1206	R59, R67, R75, R83, R91, R99, R107, R115	DALE	CRCW12061102FTR1
70	1	68NF 50V 10% 805	C8	MURRATA	GRM40X7R683K050AL
71	8	120PF 50V 5% 1206 NPO	C13, C18, C23, C28, C187-190	PHILLIPS	1206CG121J9B200

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
72	1	75 1/8W 5% 1206	R14	PHILIPS	9C12063A75R0JLRT/R
73	2	820PF 100V 10% 1206 NPO	C32, C34	AVX	12061A821KAT2A
74	2	30PF 100V 5% 1206	C3-4	AVX	12061A300JAT2A
75	8	680PF 50V 1% 805 NPO	C37, C43, C49, C55, C61, C67, C73, C79	AVX	08055A681FAT2A
76	8	2.74K 1/8W 1% 1206	R63, R71, R79, R87, R95, R103, R111, R119	PANASONIC	ERJ-8ENF2741V
77	16	5.49K 1/8W 1% 1206	R60, R61, R68, R69, R76, R77, R84, R85, R92, R93, R100, R101, R108, R109, R116, R117	PANASONIC	ERJ-8ENF5491V
78	8	3.32K 1/8W 1% 1206	R62, R70, R78, R86, R94, R102, R110, R118	PANASONIC	ERJ-8ENF3321V
79	2	100 1/8W 1% 1206	R54, R57	PANASONIC	ERJ-8ENF1000V
80	8	1.65K 1/8W 1% 1206	R64, R72, R80, R88, R96, R104, R112, R120	PANASONIC	ERJ-8ENF1651V

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
81	6	10UF 16V 20% CAP002 ELEC	CT5-10	DIG01	PCE3062TR-ND
82	10	68UF 25V 20% CAP003 ELEC	CT26-35	PANASONIC	EEV-FC1E680P
83	1	2A SL22 DO-214AA SCHOTTKY	D3	GENERAL SEMI	SL22
84	2	10K 100MW 2% RNET16 BUSSED	RN1-2	CTS	767-161-103G
85	1	1K 1/8W 5% 1206	R5	AVX	CR32-102J-T
86	1	100K 1/8W 5% 1206	R167	AVX	CR1206-1003FTR1
87	2	1.00K 1/8W 1% 1206	R53, R56	AVX	
88	2	20.0K 1/8W 1% 1206	R170,R173	DALE	CRCW1206-2002FRT1
89	2	22 1/8W 5% 1206	R8-9	DALE	
90	1	74FCT244AT QSOP20 OCTAL-BUFFER	U23	CYPRESS	CY74FCT244ATQC
91	4	10.0K 1/8W 1% 1206	R51-52, R55, R58	DALE	CRCW1206-1002FRT1
92	2	RED-SMT LED001 GULL-WING	LED1, LED8	PANASONIC	LN1261C
93	1	GREEN-SMT LED001 GULL-WING	LED11	PANASONIC	LN1361C
94	8	604 1/8W 1% 1206	R65, R73, R81, R89, R97, R105, R113, R121	PANASONIC	ERJ-8ENF6040V

Reference	Quantity	Description	Reference Design	Manufacturer	Part Number
95	7	1uF 25V 20% A TANT -55+125	CT12-18	PANASONIC	ECS-T1EY105R
96	3	ADG774A QSOP16 QUICKSWITCH-257	U31.U35, U36	ANALOG DEVICES	ADG774ABRQ
97	7	IDC 2X1 IDC2X1 2X1 TIN	JP1, JP4-5, JP22-23, JP26, JP27	BERG	54101-T08-02
98	4	IDC 3X1 IDC3X1	JP2-3, JP9-10	BERG	54101-T08-03
99	1	IDC 4X1 IDC4X1	P3	BERG	54102-T08-02
100	1	IDC 2X2 IDC2X2 0.1x0.1	JP6	SULLINS	PTC02DAAN
101	6	IDC 3X2 IDC3X2	JP7-8, JP11, JP19-21	BERG	54102-T08-03
102	1	IDC 7X2 IDC7X2 HEADER	P12	BERG	54102-T08-07
103	1	2.5A RESETABLE FUS001	F1	RAYCHEM CORP.	SMD250-2
104	2	3.5MM STEREO_JACK CON001	P7, P17	SHOGYO	SJ-0359AM-5

ADSP-21161 EZ-KIT LITE Schematic

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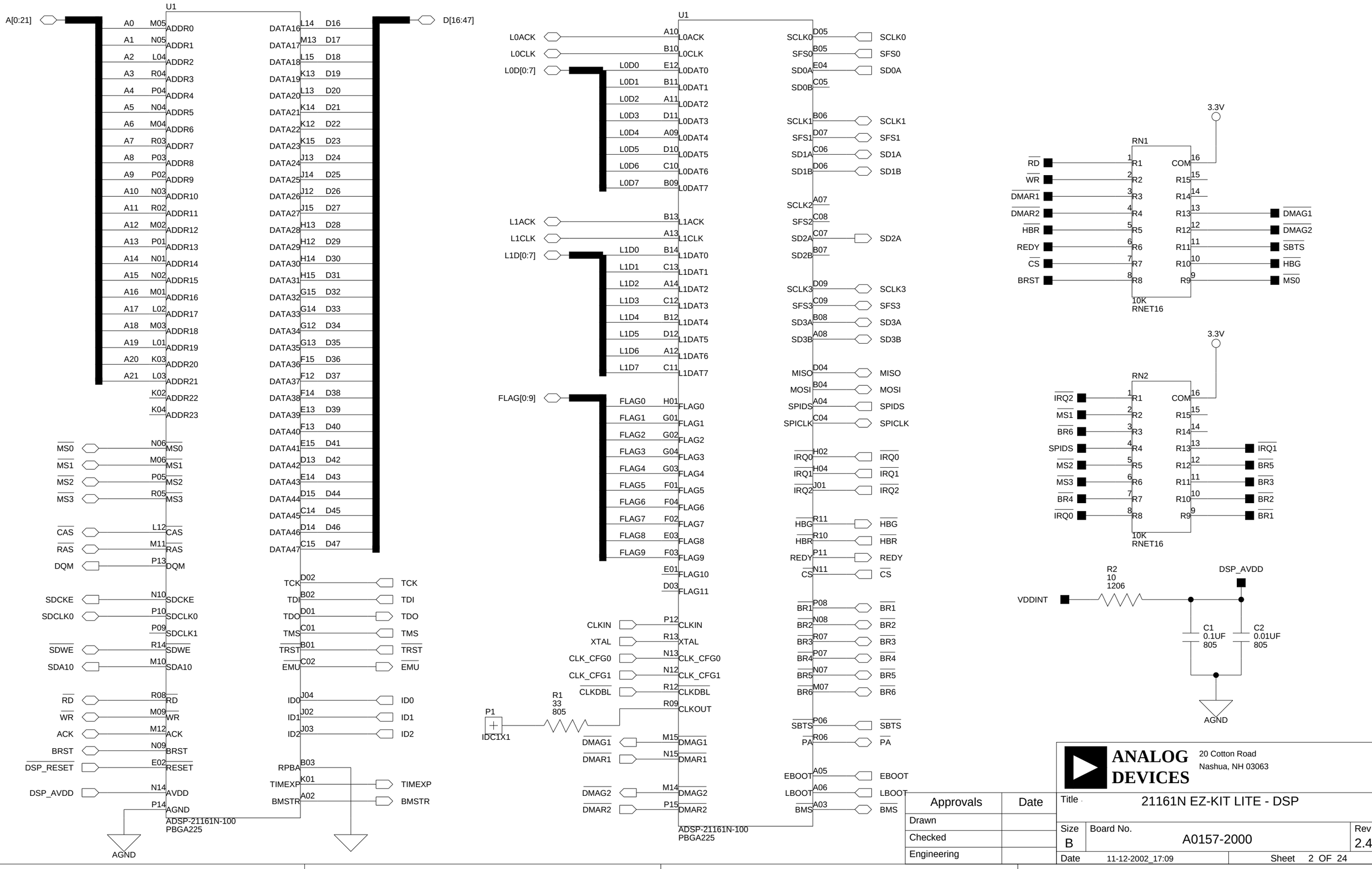
Title · 21161N EZ-KIT LITE - TITLE PAGE		
Size B	Board No. A0157-2000	Rev 2.4
Date 11-13-2003_11:40	Sheet 1 OF 24	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U1
A0 M05 ADDR0
A1 N05 ADDR1
A2 L04 ADDR2
A3 R04 ADDR3
A4 P04 ADDR4
A5 N04 ADDR5
A6 M04 ADDR6
A7 R03 ADDR7
A8 P03 ADDR8
A9 P02 ADDR9
A10 N03 ADDR10
A11 R02 ADDR11
A12 M02 ADDR12
A13 P01 ADDR13
A14 N01 ADDR14
A15 N02 ADDR15
A16 M01 ADDR16
A17 L02 ADDR17
A18 M03 ADDR18
A19 L01 ADDR19
A20 K03 ADDR20
A21 L03 ADDR21
K02 ADDR22
K04 ADDR23
D[16:47]
DATA16 L14 D16
DATA17 M13 D17
DATA18 L15 D18
DATA19 K13 D19
DATA20 L13 D20
DATA21 K14 D21
DATA22 K12 D22
DATA23 K15 D23
DATA24 J13 D24
DATA25 J14 D25
DATA26 J12 D26
DATA27 J15 D27
DATA28 H13 D28
DATA29 H12 D29
DATA30 H14 D30
DATA31 H15 D31
DATA32 G15 D32
DATA33 G14 D33
DATA34 G12 D34
DATA35 G13 D35
DATA36 F15 D36
DATA37 F12 D37
DATA38 F14 D38
DATA39 E13 D39
DATA40 F13 D40
DATA41 E15 D41
DATA42 D13 D42
DATA43 E14 D43
DATA44 D15 D44
DATA45 C14 D45
DATA46 D14 D46
DATA47 C15 D47
MS0 N06 MS0
MS1 M06 MS1
MS2 P05 MS2
MS3 R05 MS3
CAS L12 CAS
RAS M11 RAS
DQM P13 DQM
SDCKE N10 SDCKE
SDCLK0 P10 SDCLK0
P09 SDCLK1
SDWE R14 SDWE
SDA10 M10 SDA10
RD R08 RD
WR M09 WR
ACK M12 ACK
BRST N09 BRST
DSP_RESET E02 RESET
DSP_AVDD N14 AVDD
P14 AGND
ADSP-21161N-100
PBGA225
AGND
TCK D02 TCK
TDI B02 TDI
TDO D01 TDO
TMS C01 TMS
TRST B01 TRST
EMU C02 EMU
ID0 J04 ID0
ID1 J02 ID1
ID2 J03 ID2
RPBA B03
TIMEXP K01 TIMEXP
BMSTR A02 BMSTR
U1
L0ACK A10 L0ACK
L0CLK B10 L0CLK
L0D[0:7]
L0D0 E12 L0DAT0
L0D1 B11 L0DAT1
L0D2 A11 L0DAT2
L0D3 D11 L0DAT3
L0D4 A09 L0DAT4
L0D5 D10 L0DAT5
L0D6 C10 L0DAT6
L0D7 B09 L0DAT7
L1ACK B13 L1ACK
L1CLK A13 L1CLK
L1D[0:7]
L1D0 B14 L1DAT0
L1D1 C13 L1DAT1
L1D2 A14 L1DAT2
L1D3 C12 L1DAT3
L1D4 B12 L1DAT4
L1D5 D12 L1DAT5
L1D6 A12 L1DAT6
L1D7 C11 L1DAT7
FLAG[0:9]
FLAG0 H01 FLAG0
FLAG1 G01 FLAG1
FLAG2 G02 FLAG2
FLAG3 G04 FLAG3
FLAG4 G03 FLAG4
FLAG5 F01 FLAG5
FLAG6 F04 FLAG6
FLAG7 F02 FLAG7
FLAG8 E03 FLAG8
FLAG9 F03 FLAG9
E01 FLAG10
D03 FLAG11
CLKIN P12 CLKIN
XTAL R13 XTAL
CLK_CFG0 N13 CLK_CFG0
CLK_CFG1 N12 CLK_CFG1
CLKDBL R12 CLKDBL
R09 CLKOUT
P1
IDC1X1
R1
33
805
DMAG1 M15 DMAG1
DMAR1 N15 DMAR1
DMAG2 M14 DMAG2
DMAR2 P15 DMAR2
ADSP-21161N-100
PBGA225
SCLK0 D05 SCLK0
SFS0 B05 SFS0
SD0A E04 SD0A
SD0B C05
SCLK1 B06 SCLK1
SFS1 D07 SFS1
SD1A C06 SD1A
SD1B D06 SD1B
SCLK2 A07
SFS2 C08
SD2A C07 SD2A
SD2B B07
SCLK3 D09 SCLK3
SFS3 C09 SFS3
SD3A B08 SD3A
SD3B A08 SD3B
MISO D04 MISO
MOSI B04 MOSI
SPIDS A04 SPIDS
SPICLK C04 SPICLK
IRQ0 H02 IRQ0
IRQ1 H04 IRQ1
IRQ2 J01 IRQ2
HBG R11 HBG
HBR R10 HBR
REDY P11 REDY
CS N11 CS
BR1 P08 BR1
BR2 N08 BR2
BR3 R07 BR3
BR4 P07 BR4
BR5 N07 BR5
BR6 M07 BR6
SBTS P06 SBTS
PA R06 PA
EBOOT A05 EBOOT
LBOOT A06 LBOOT
BMS A03 BMS
3.3V
RN1
RD 1 R1 COM 16
WR 2 R2 R15 15
DMAR1 3 R3 R14 14
DMAR2 4 R4 R13 13 DMAG1
HBR 5 R5 R12 12 DMAG2
REDY 6 R6 R11 11 SBTS
CS 7 R7 R10 10 HBG
BRST 8 R8 R9 9 MS0
10K
RNET16
3.3V
RN2
IRQ2 1 R1 COM 16
MS1 2 R2 R15 15
BR6 3 R3 R14 14
SPIDS 4 R4 R13 13 IRQ1
MS2 5 R5 R12 12 BR5
MS3 6 R6 R11 11 BR3
BR4 7 R7 R10 10 BR2
IRQ0 8 R8 R9 9 BR1
10K
RNET16
R2
10
1206
VDDINT
DSP_AVDD
C1
0.1UF
805
C2
0.01UF
805
AGND
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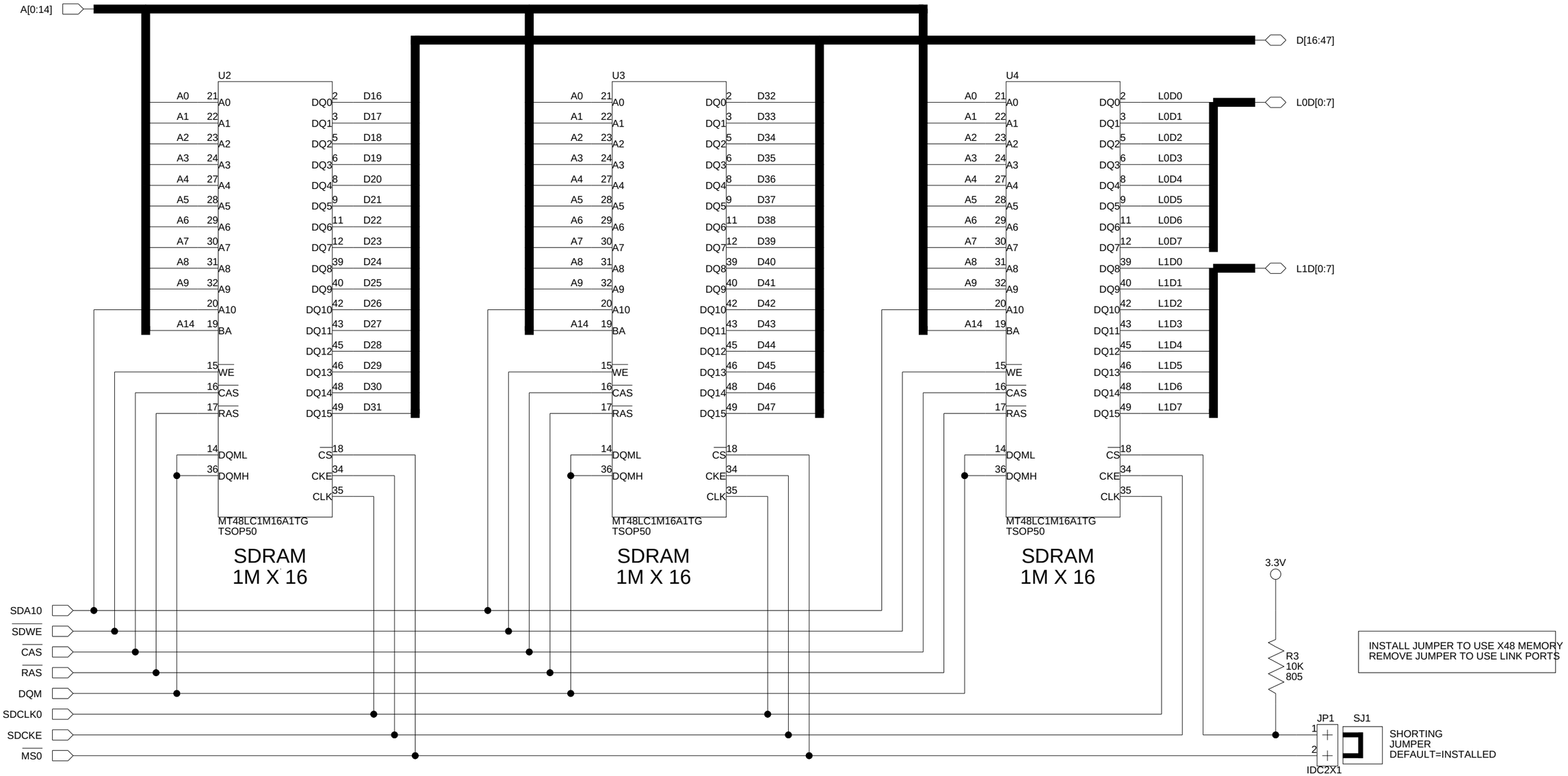
Title
21161N EZ-KIT LITE - DSP
Size
B
Board No.
A0157-2000
Rev
2.4
Date
11-12-2002_17:09
Sheet 2 OF 24



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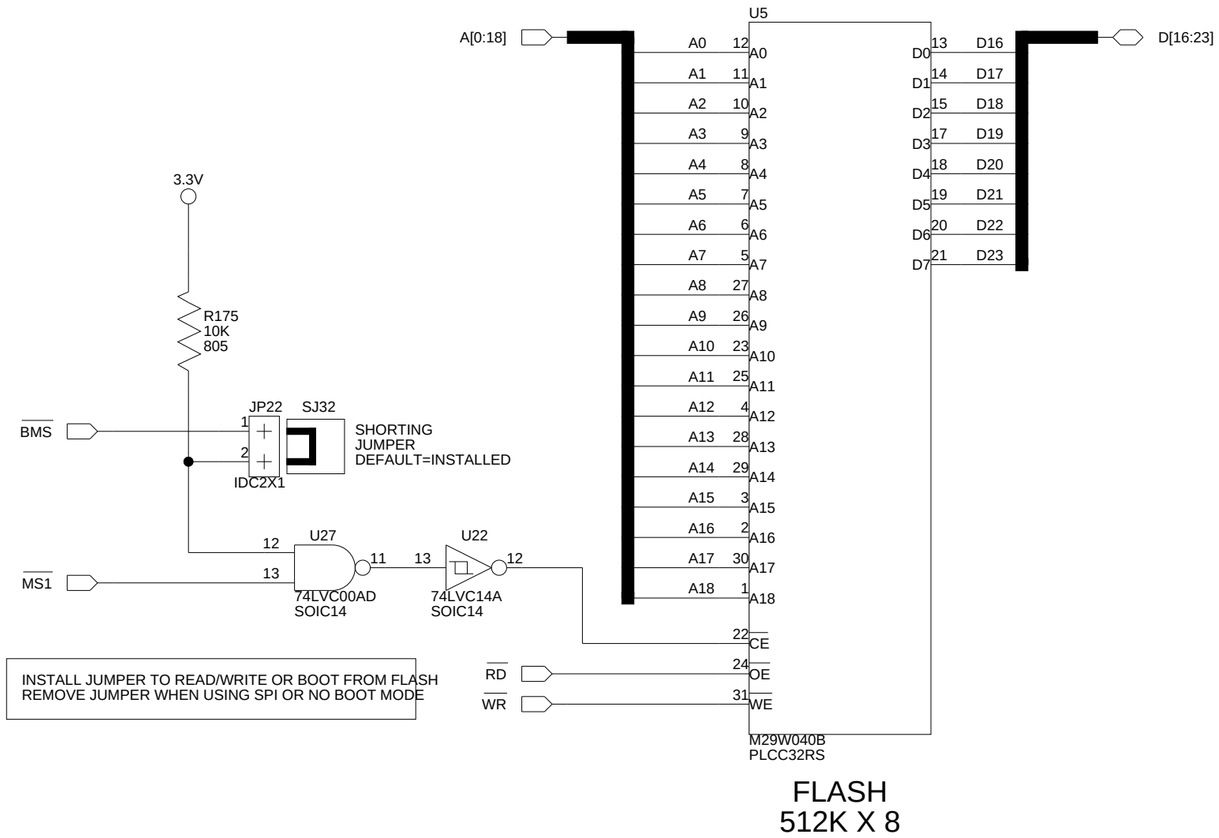
Title: 21161N EZ-KIT LITE - SDRAM

Size	Board No.	Rev
B	A0157-2000	2.4

Date: 11-12-2002_17:09 | Sheet 3 OF 24



FLASH
512K X 8

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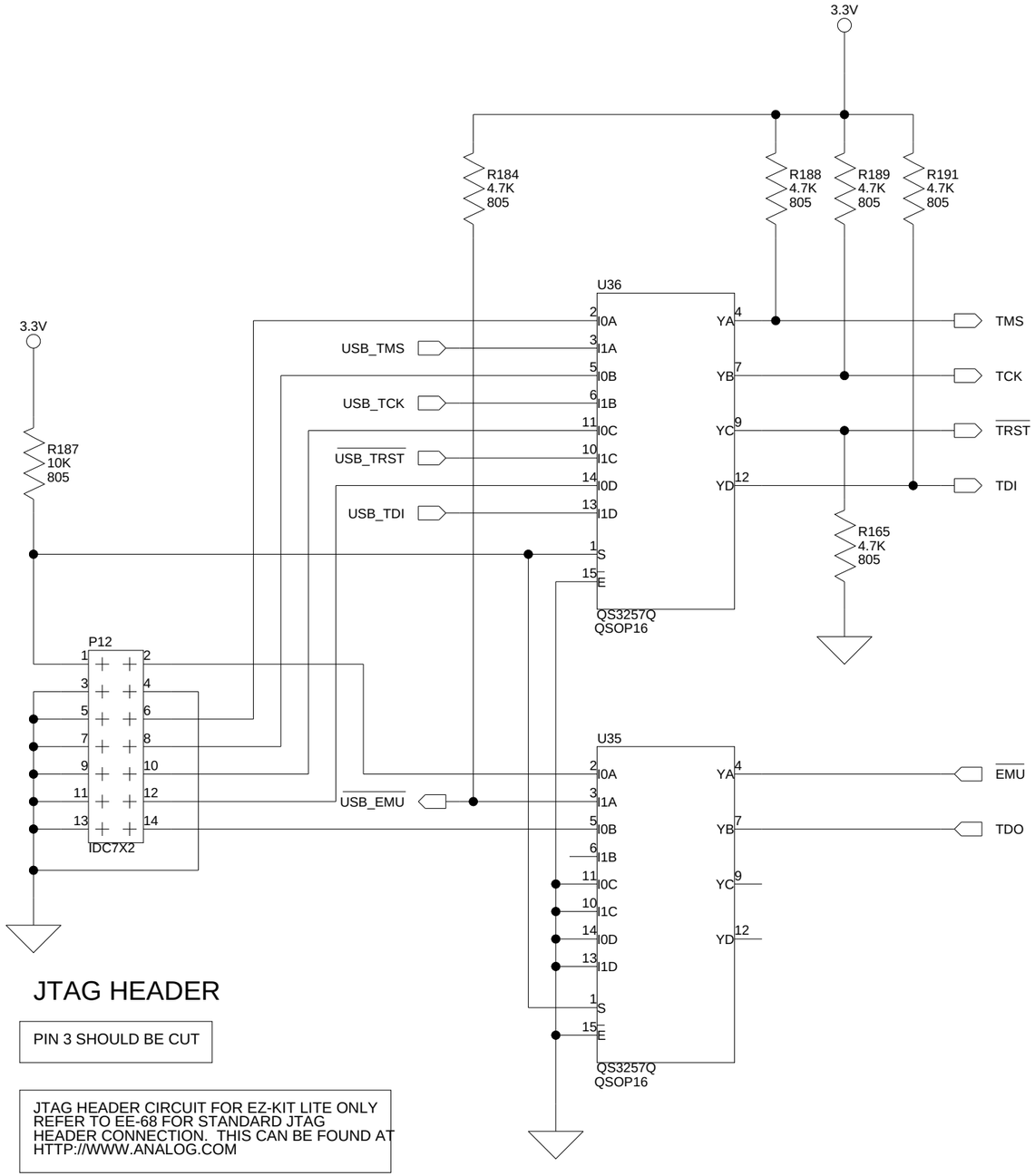
Title: 21161N EZ-KIT LITE - FLASH & SRAM

Size	Board No.	Rev
B	A0157-2000	2.4

Date 2-19-2004_15:44 Sheet 4 OF 24



JTAG HEADER

PIN 3 SHOULD BE CUT

JTAG HEADER CIRCUIT FOR EZ-KIT LITE ONLY
REFER TO EE-68 FOR STANDARD JTAG
HEADER CONNECTION. THIS CAN BE FOUND AT
HTTP://WWW.ANALOG.COM

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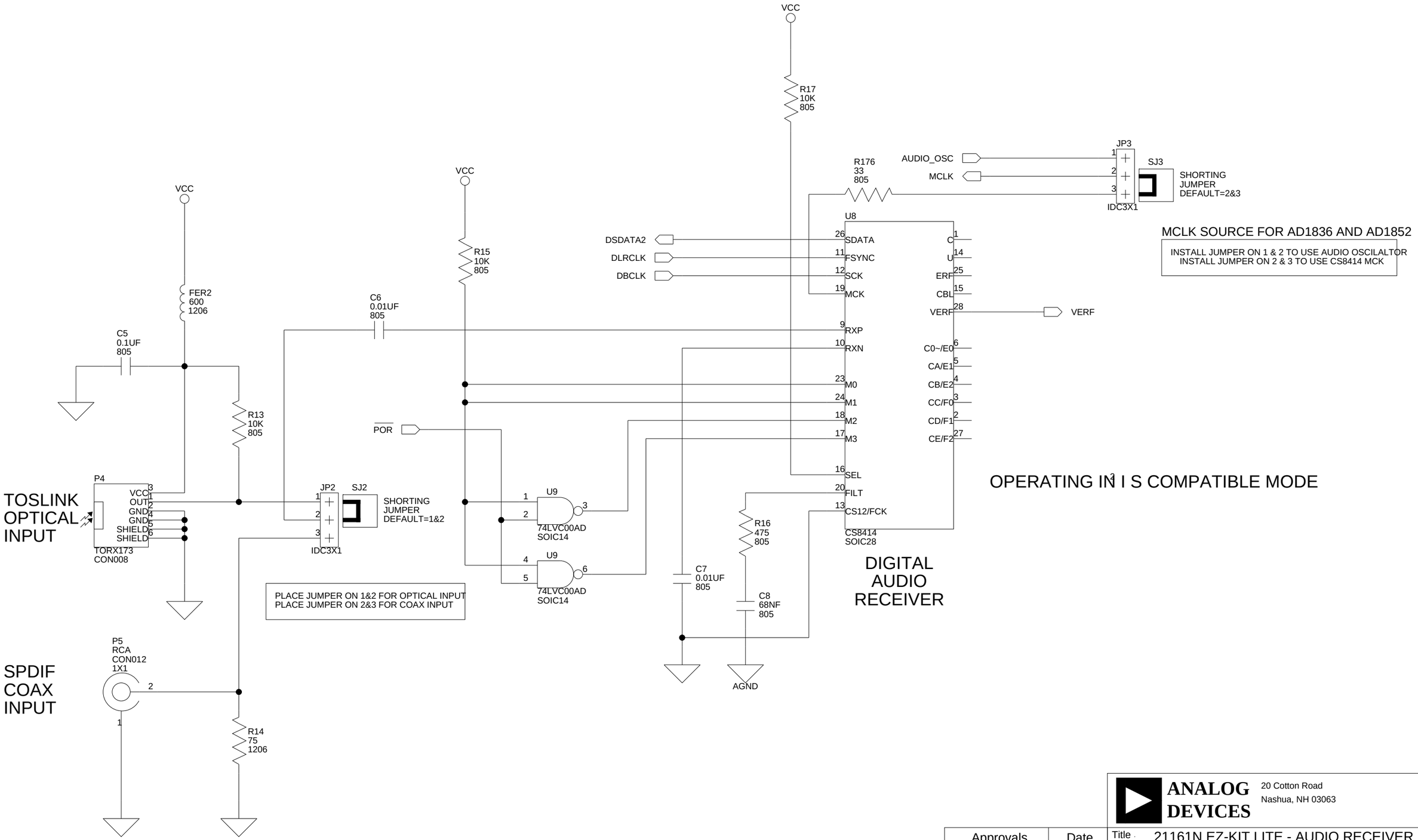
Title 21161N EZ-KIT LITE - JTAG INTERFACE

Size	Board No.	Rev
B	A0157-2000	2.4

Date

Sheet 6 OF 24



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Title: 21161N EZ-KIT LITE - AUDIO RECEIVER

Size	Board No.	Rev
B	A0157-2000	2.4

Date: 12-9-2003_21:30 | Sheet 7 OF 24

INSTALL JUMPER TO CONNECT CODEC TO SPI PORT (JP12 & JP13 NOT INSTALLED)
REMOVE JUMPER TO USE FLAG0 FOR PUSH BUTTON OR EXPANSION HEADER

ODVDD IS CONNECTED TO 3.3V

CODEC

AD1836AAS
MQFP52

AUX DAC

AD1852
SSOP28

ADC1 LEFT
ADC1 RIGHT
ADC2 LEFT
ADC2 RIGHT

DAC1 LEFT
DAC1 RIGHT
DAC2 LEFT
DAC2 RIGHT
DAC3 LEFT
DAC3 RIGHT
DAC4 LEFT
DAC4 RIGHT

SAMPLE FREQUENCY	1&2	3&4
NOT ALLOWED	NOT SHORTED	NOT SHORTED
192kHz (2X INTERPOLATOR)	NOT SHORTED	SHORTED
96kHz (4X INTERPOLATOR)	SHORTED	NOT SHORTED
48kHz (8X INTERPOLATOR)	SHORTED	SHORTED

INSTALL JUMPER TO CONNECT DAC TO SPI PORT (JP12 & JP13 NOT INSTALLED)
REMOVE JUMPER TO USE FLAG1 FOR PUSH BUTTON OR EXPANSION HEADER

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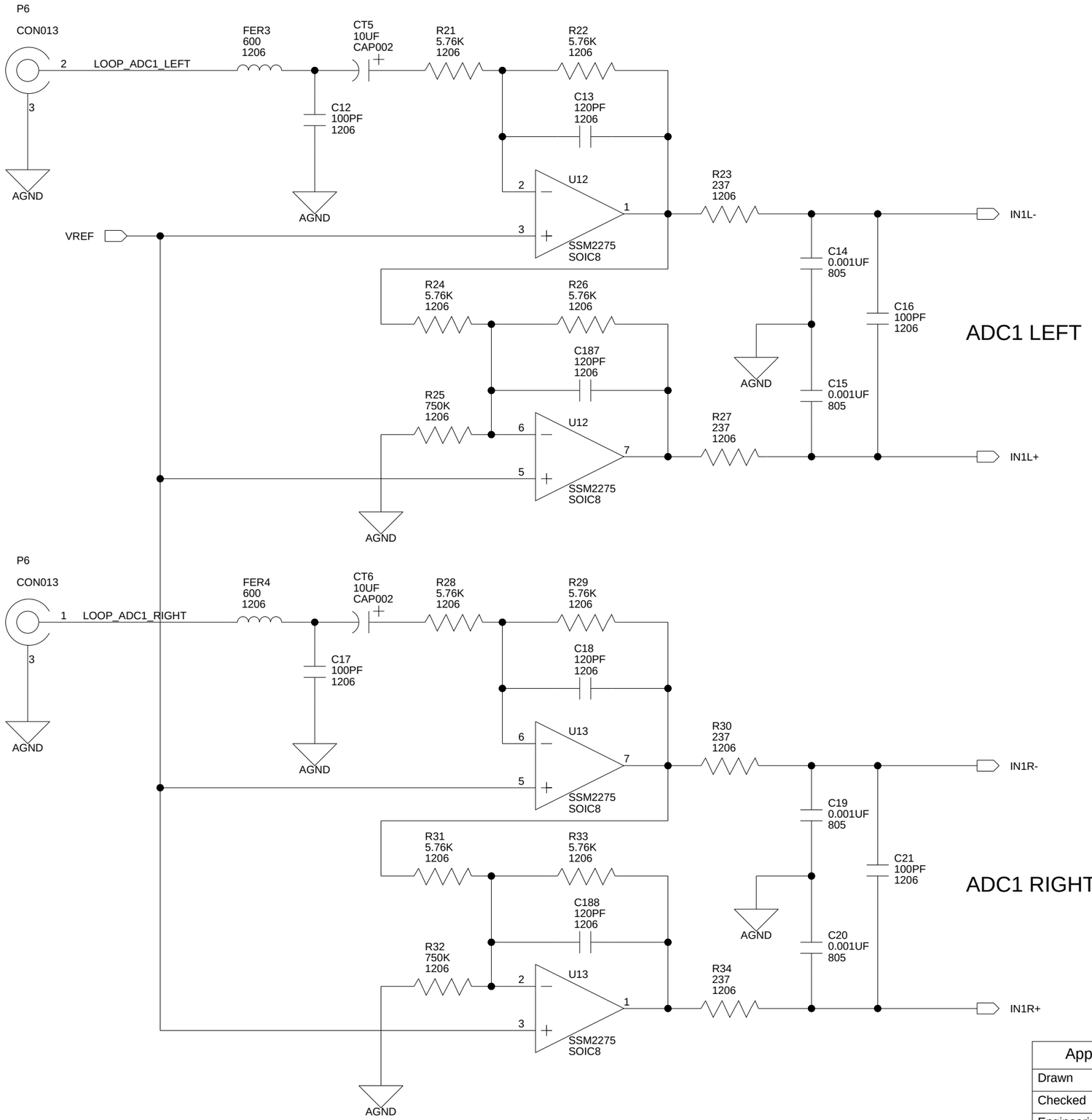
Title: 21161N EZ-KIT LITE - CODEC & DAC

Size	Board No.	Rev
B	A0157-2000	2.4

Date 2-19-2004_14:44 Sheet 8 OF 24



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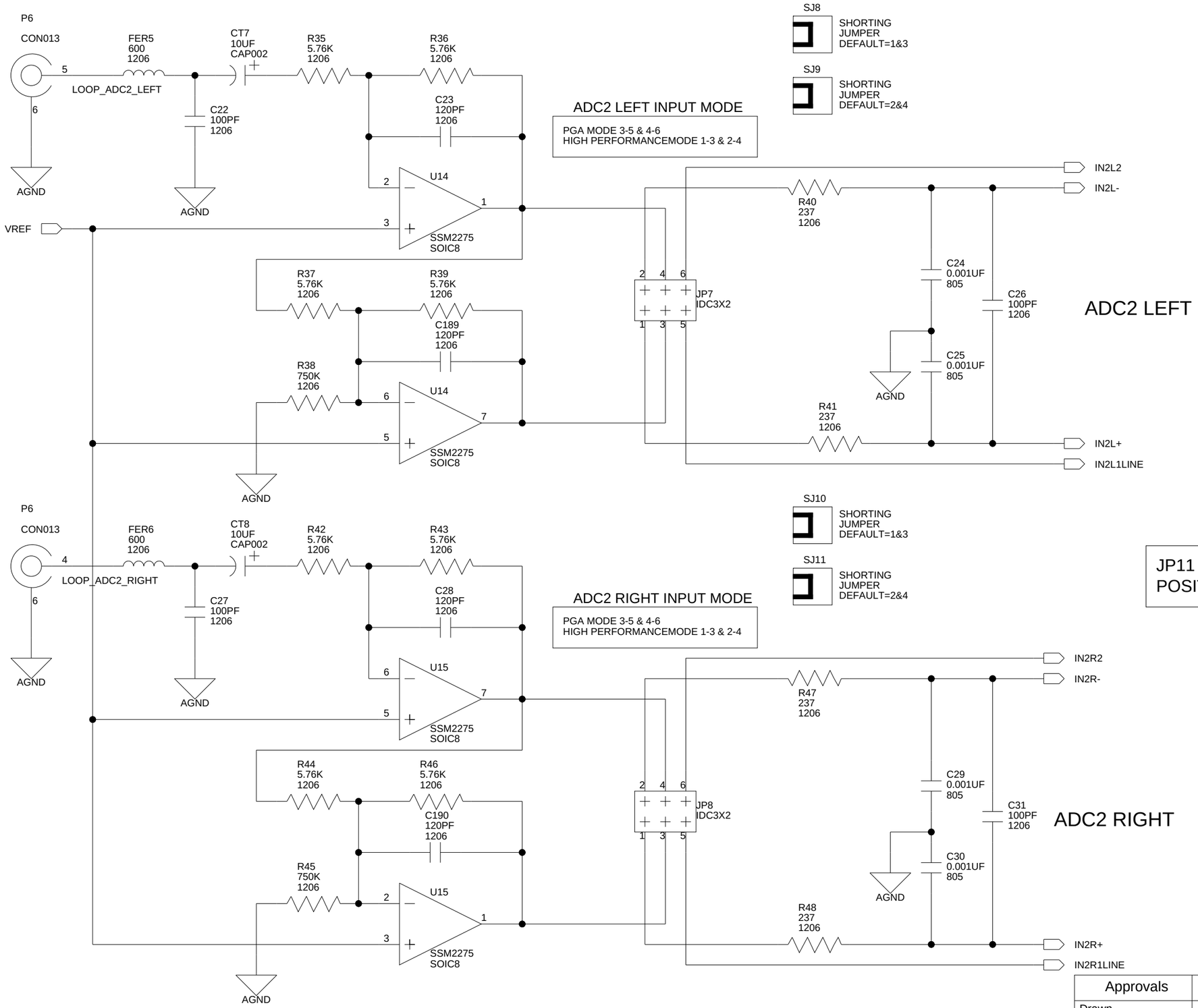
Title: 21161N EZ-KIT LITE - PRIMARY INPUT

Size	Board No.	Rev
B	A0157-2000	2.4

Date: 11-12-2002_17:10 | Sheet 9 OF 24



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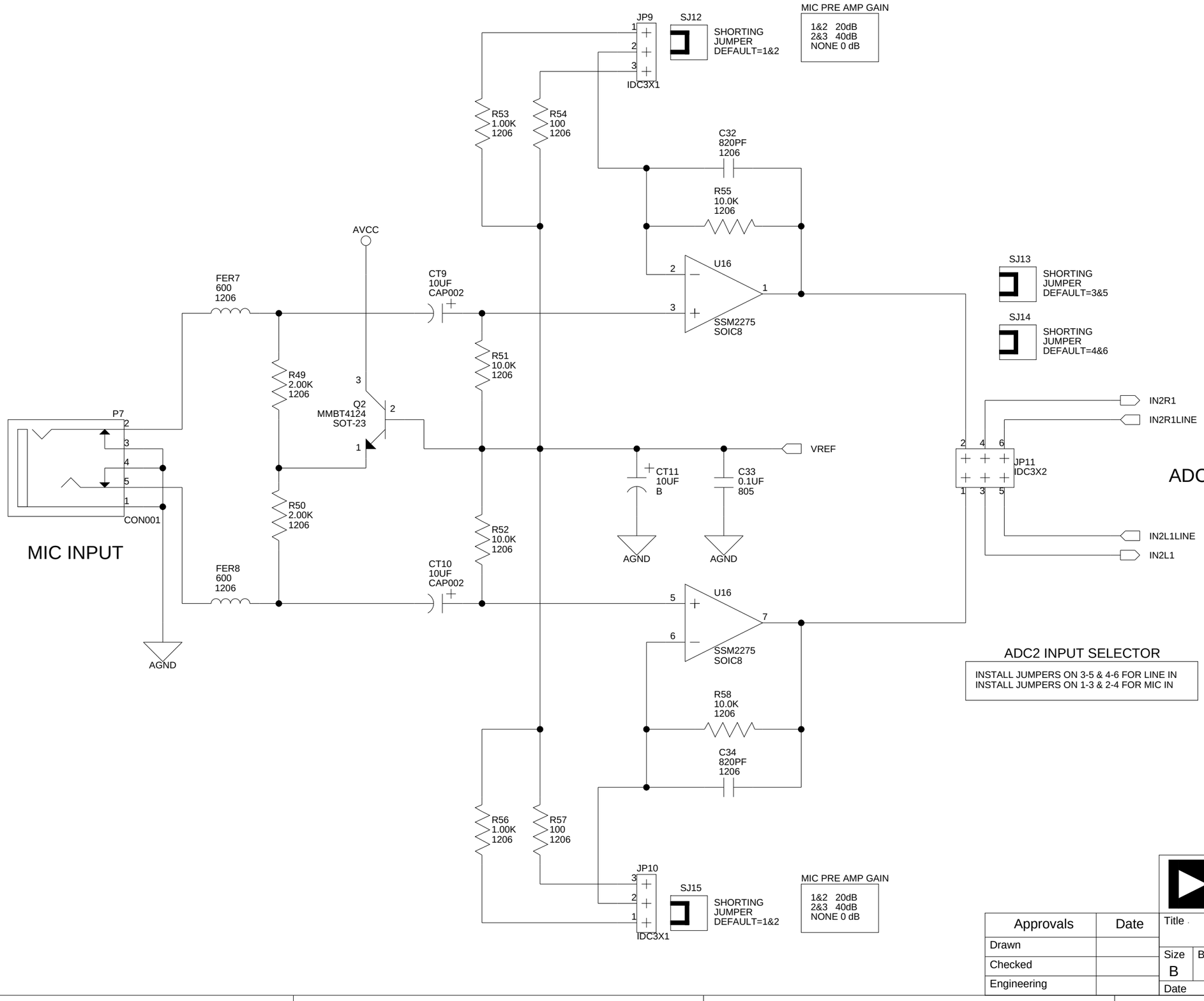
Title · 21161N EZ-KIT LITE - SECONDARY INPUT

Size	Board No.	Rev
B	A0157-2000	2.4

Date 11-12-2002_17:11 Sheet 10 OF 24



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Engineering	

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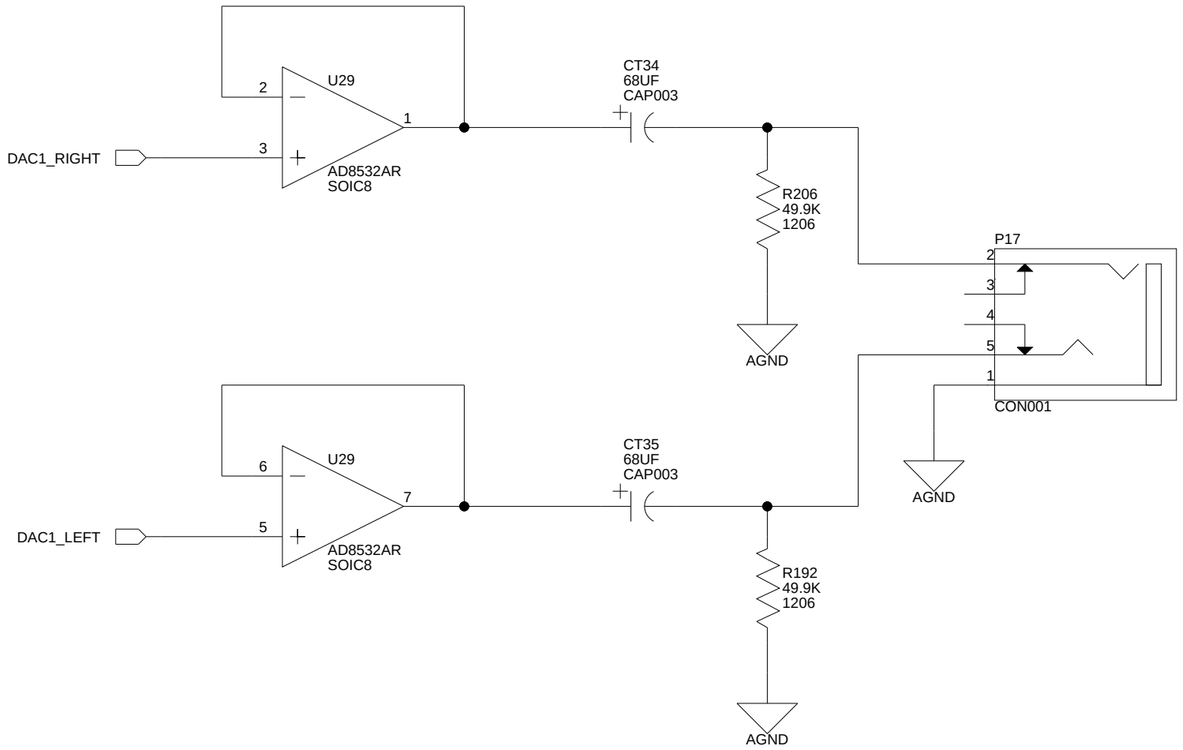
Title: 21161N EZ-KIT LITE - MIC INPUT

Size	Board No.	Rev
B	A0157-2000	2.4

Date 2-19-2004_14:44 Sheet 11 OF 24



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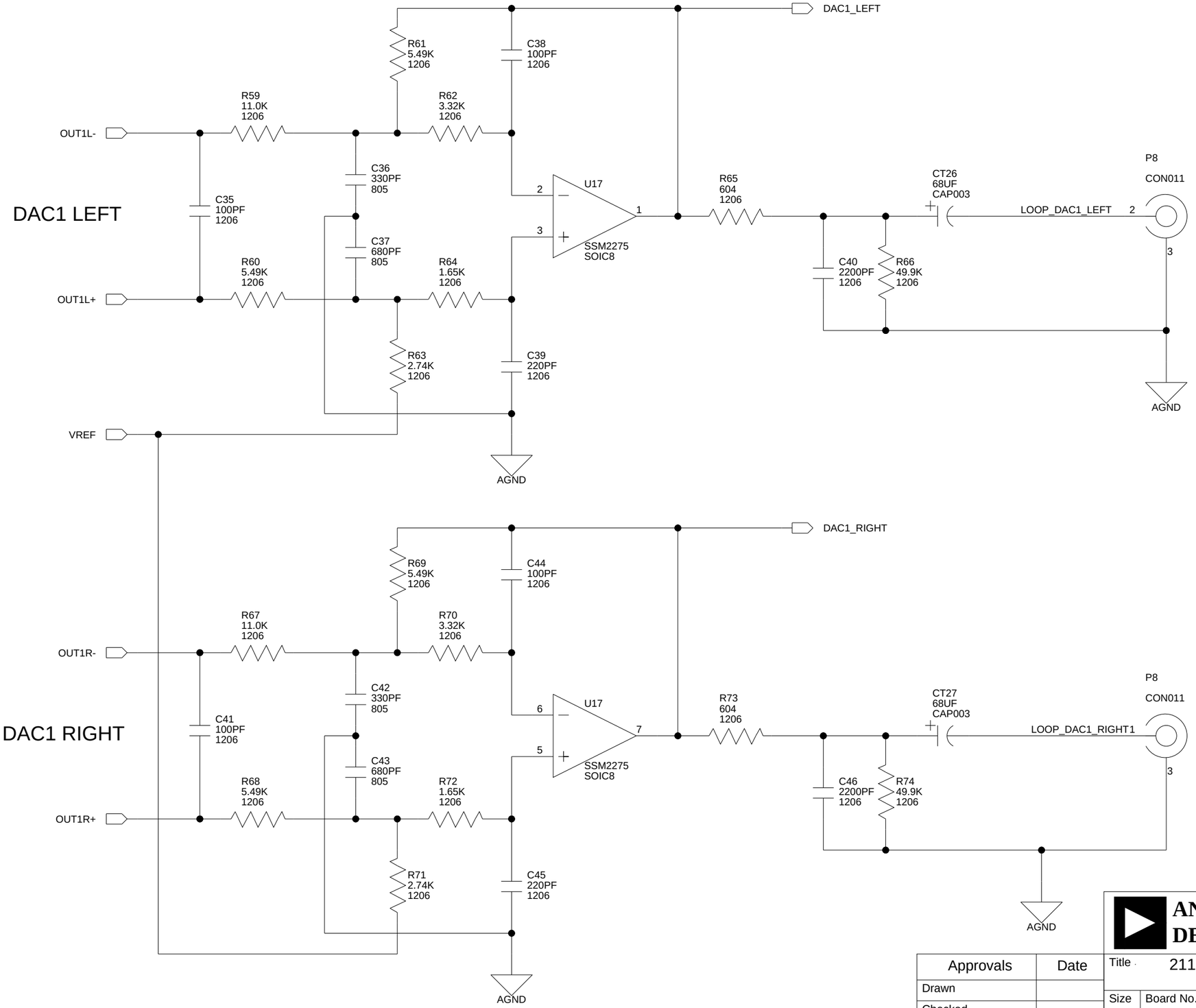
Title: 21161N EZ-KIT LITE - DAC1 OUTPUT-STEREO JACK

Size	Board No.	Rev
B	A0157-2000	2.4

Date | Sheet 12 OF 24



Approvals	Date
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Checked	
Engineering	

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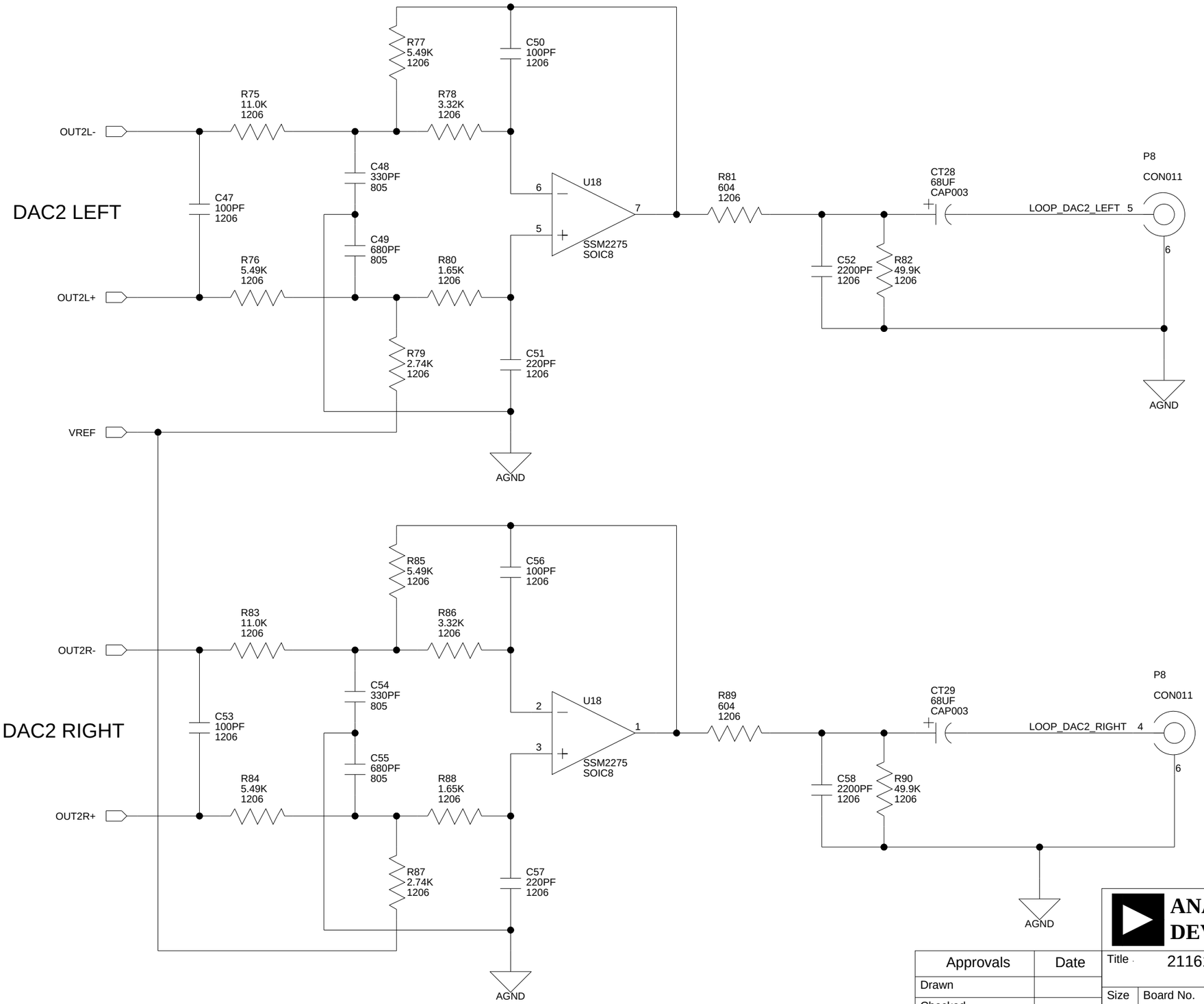
Title	21161N EZ-KIT LITE - DAC1 OUTPUT	
Size B	Board No. A0157-2000	Rev 2.4
Date 11-12-2002_17:12	Sheet 13 OF 24	



Approvals	Date
Drawn	
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Engineering	

ANALOG DEVICES
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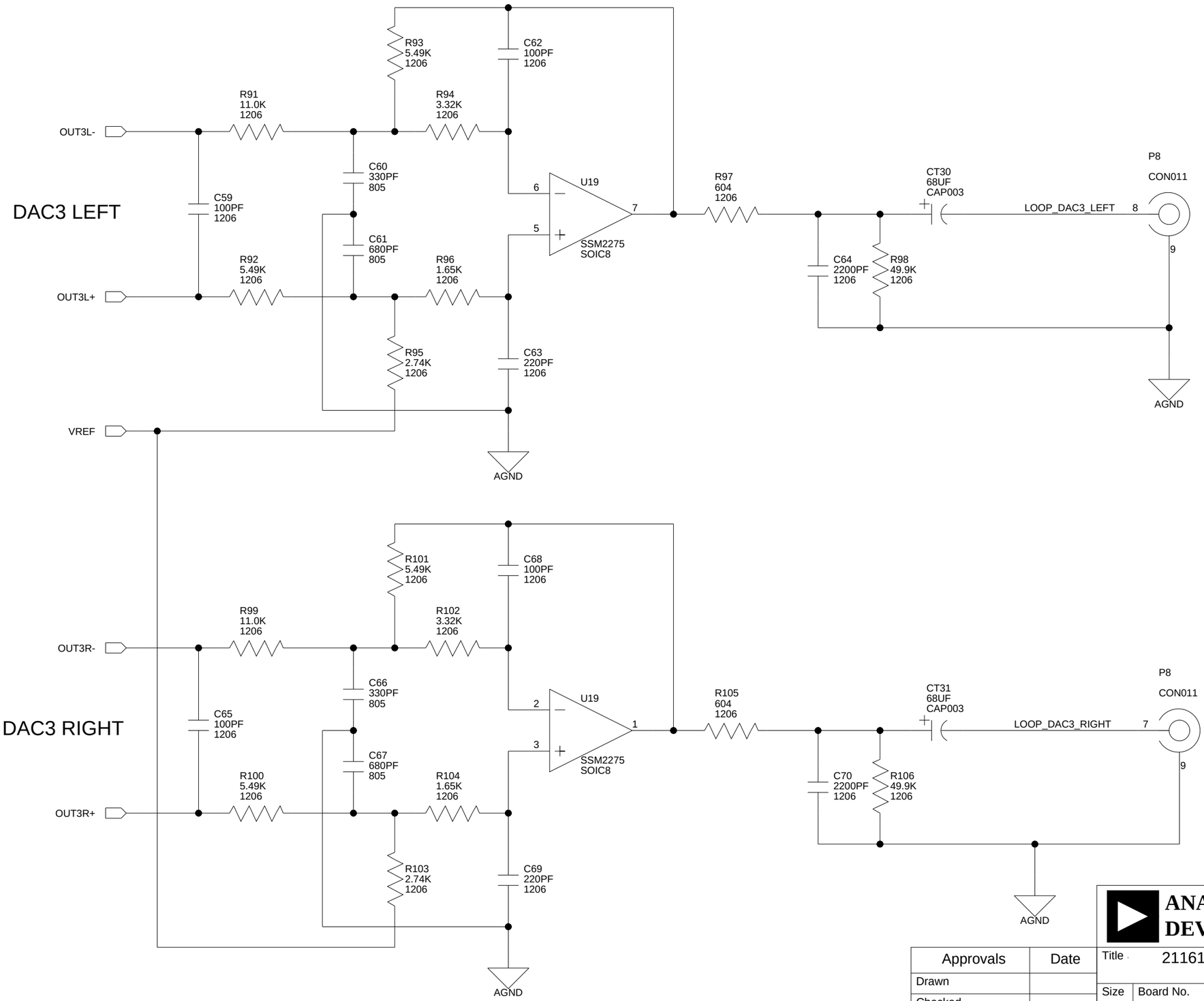
Title: 21161N EZ-KIT LITE - DAC2 OUTPUT

Size	Board No.	Rev
B	A0157-2000	2.4

Date: 11-12-2002_17:12 | Sheet 14 OF 24



Approvals	Date
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Engineering	

ANALOG DEVICES
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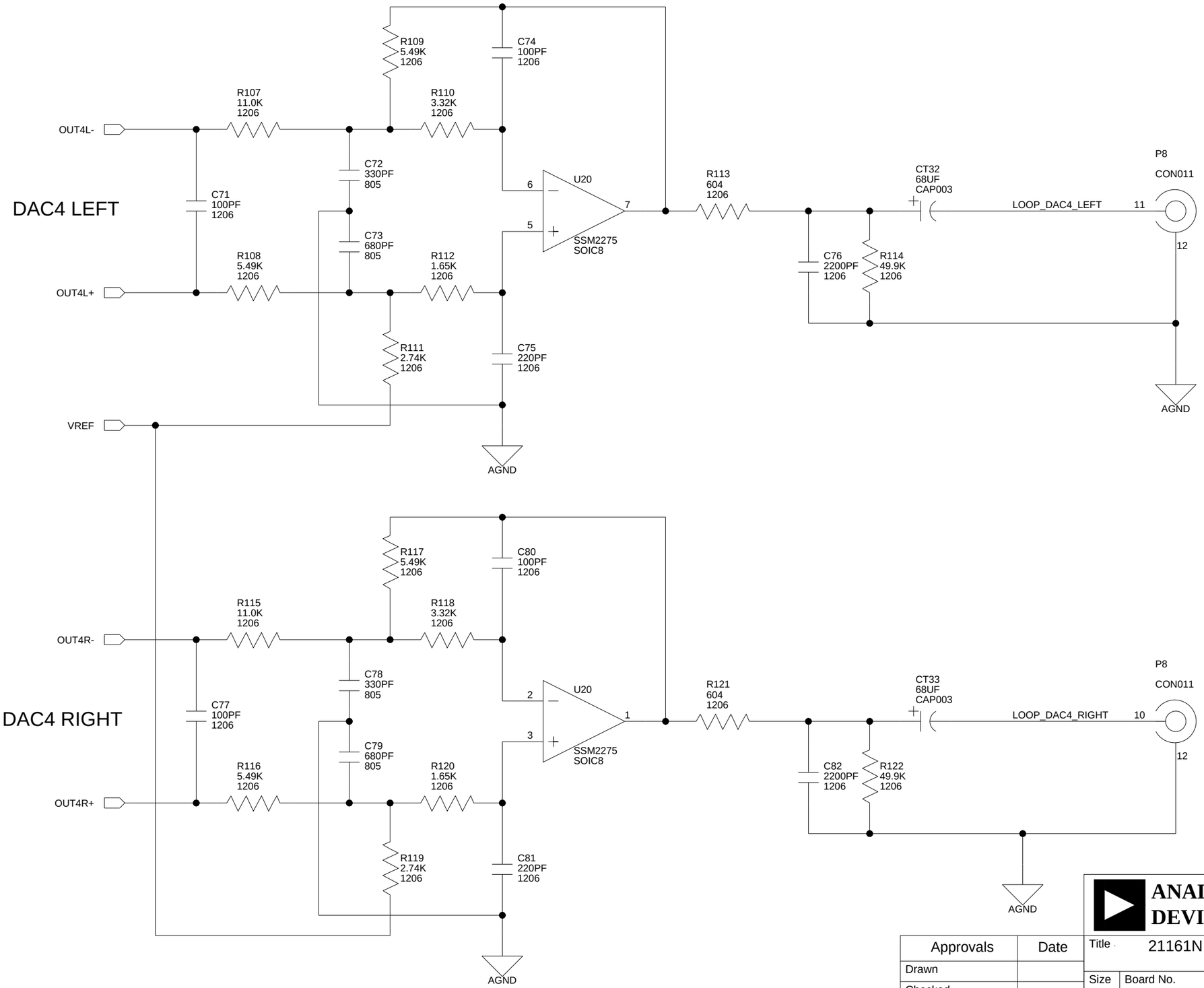
Title: 21161N EZ-KIT LITE - DAC3 OUTPUT

Size	Board No.	Rev
B	A0157-2000	2.4

Date: 11-12-2002_17:12 | Sheet 15 OF 24



Approvals	Date
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Checked	
Engineering	

ANALOG DEVICES
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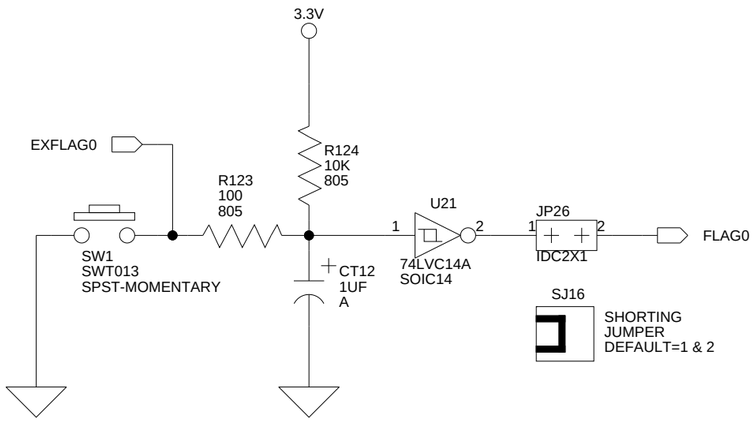
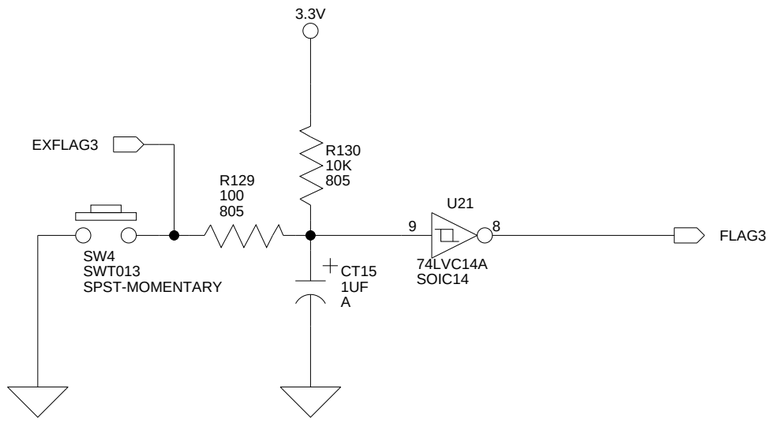
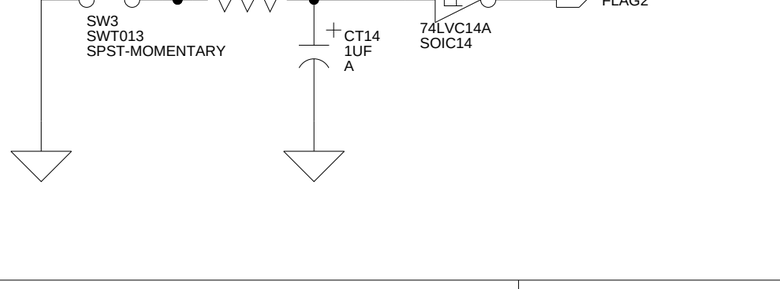
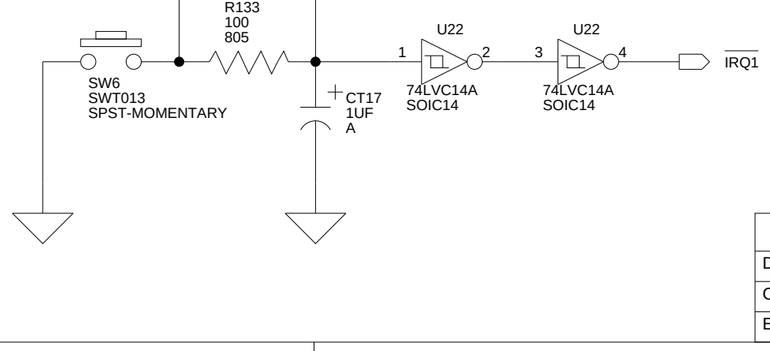
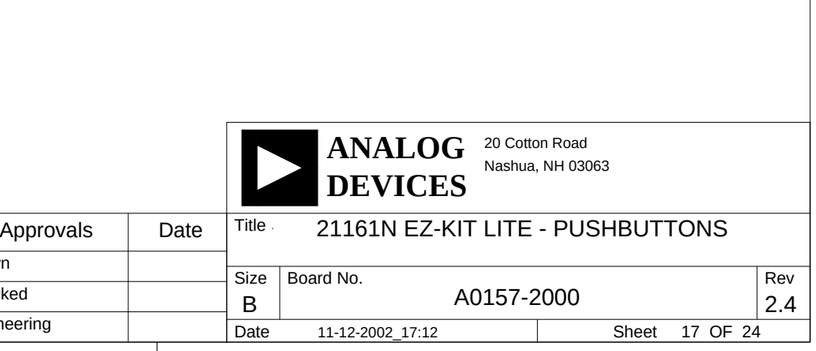
Title: 21161N EZ-KIT LITE - DAC4 OUTPUT		
Size: B	Board No.: A0157-2000	Rev: 2.4
Date: 11-12-2002_17:12	Sheet: 16 OF 24	











Approvals	Date
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Checked	
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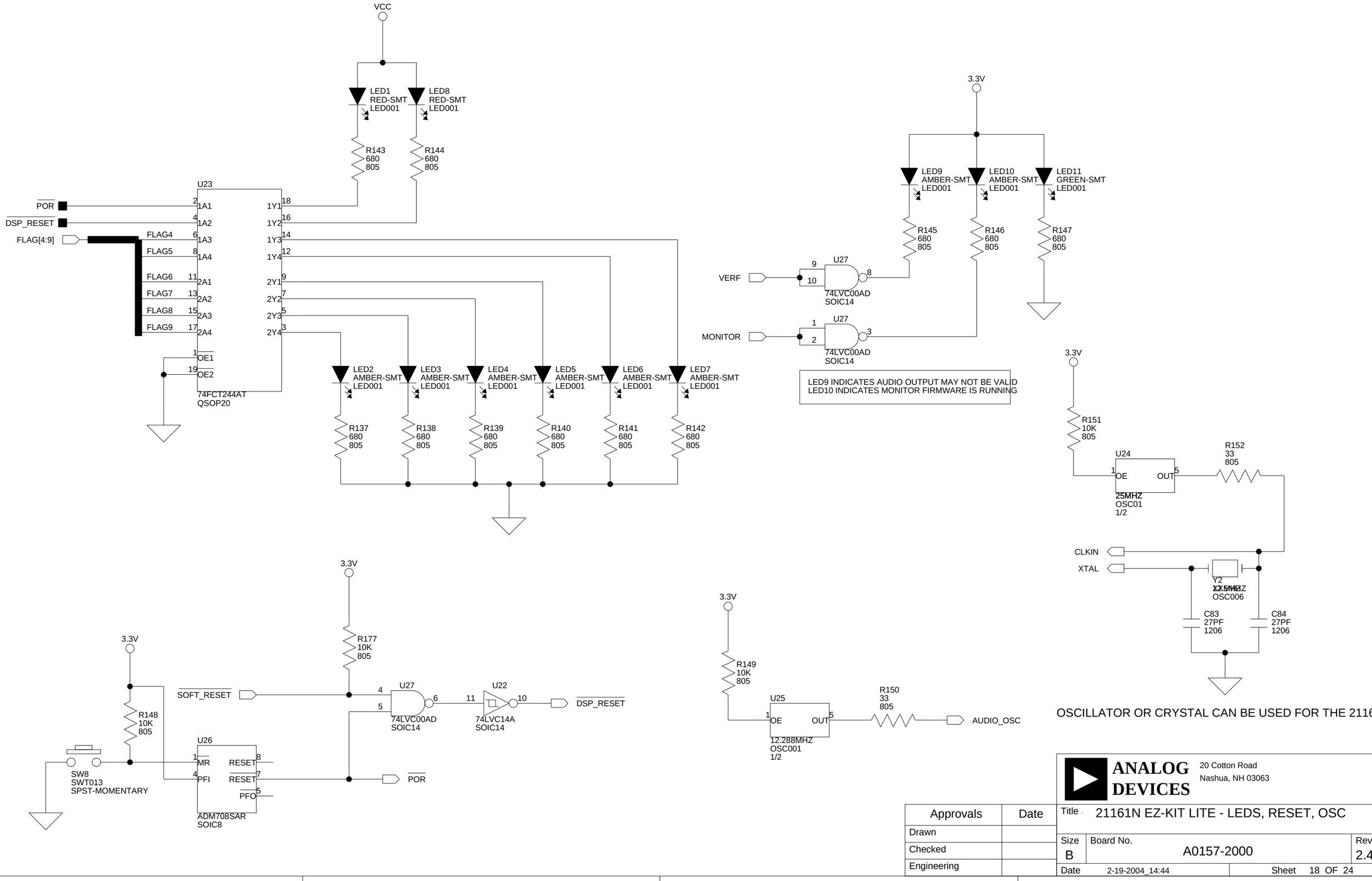
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063

Title: 21161N EZ-KIT LITE - PUSHBUTTONS

Size	Board No.	Rev
B	A0157-2000	2.4

Date 11-12-2002_17:12 Sheet 17 OF 24



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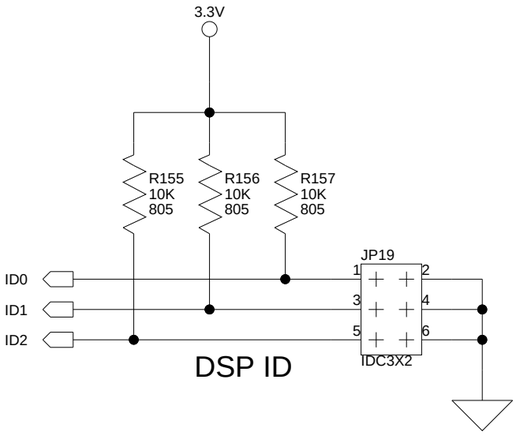
Title · 21161N EZ-KIT LITE - LEDS, RESET, OSC

Size	Board No.	Rev
B	A0157-2000	2.4

Date 2-19-2004_14:44 Sheet 18 OF 24

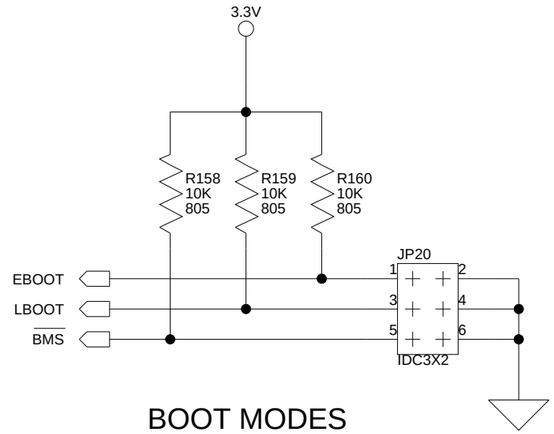


DSP ID

SJ23
SHORTING JUMPER
DEFAULT=1 & 2

SJ24
SHORTING JUMPER
DEFAULT=3 & 4

SJ25
SHORTING JUMPER
DEFAULT=5 & 6



BOOT MODES

	EBOOT	LBOOT	BMS	Booting Mode
*	1	0	Output	EPROM
	0	0	1 (Input)	Host Processor
	0	1	0 (Input)	Serial Boot via SPI
	0	1	1 (Input)	Link Port
	0	0	0 (Input)	No Booting
	1	1	x (Input)	Reserved

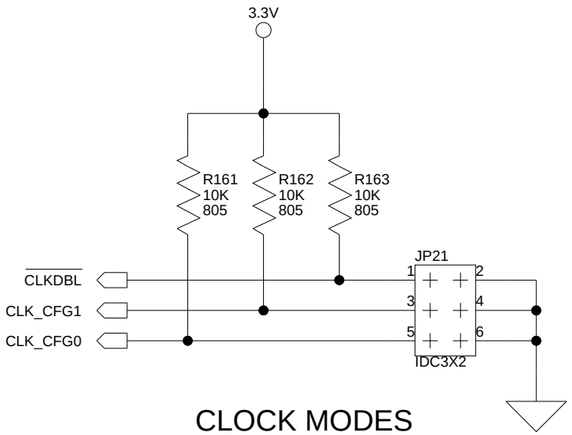
* DENOTES FACTORY DEFAULT

REMOVE JP22 WHEN USING SPI OR NO BOOT MODES (REFER TO SHEET 4)

SJ26
SHORTING JUMPER
DEFAULT=3 & 4

SJ27
SHORTING JUMPER
DEFAULT=NOT INSTALLED

SJ28
SHORTING JUMPER
DEFAULT=NOT INSTALLED



CLOCK MODES

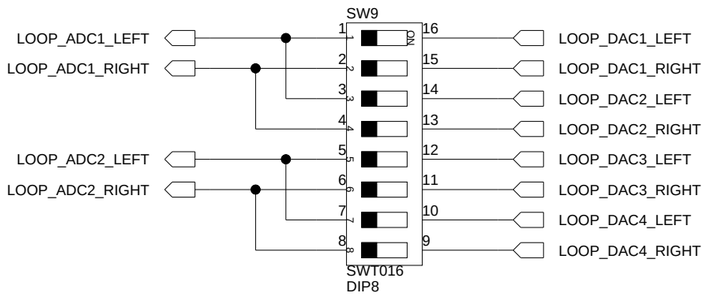
	CLKDBL	CLK_CFG1	CLK_CFG0	Core Clock Ratio	EP Clock Ratio
	1	0	0	2:1	1x
	1	0	1	3:1	1x
*	1	1	0	4:1	1x
	0	0	0	4:1	2x
	0	0	1	6:1	2x
	0	1	0	8:1	2x

* DENOTES FACTORY DEFAULT

SJ29
SHORTING JUMPER
DEFAULT=NOT INSTALLED

SJ30
SHORTING JUMPER
DEFAULT=NOT INSTALLED

SJ31
SHORTING JUMPER
DEFAULT=5 & 6



TURNING THE SWITCHES ON PUTS THE BOARD IN LOOPBACK MODE

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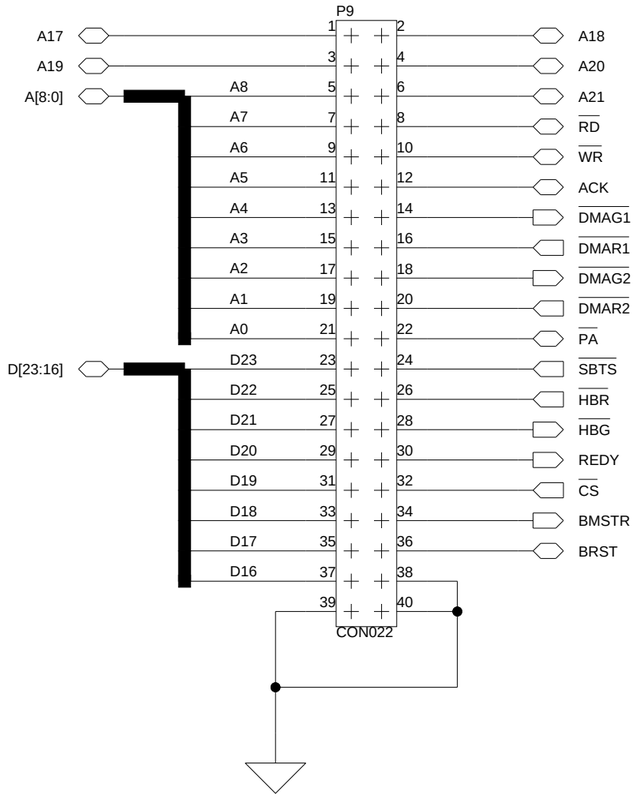
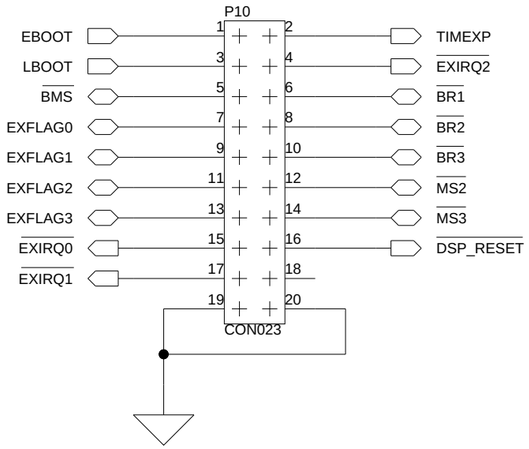
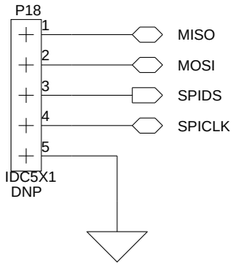
Title · 21161N EZ-KIT LITE - CONFIGURATION

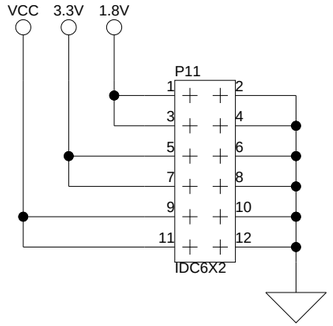
Size	Board No.	Rev
B	A0157-2000	2.4

Date 11-12-2002_17:12 Sheet 19 OF 24









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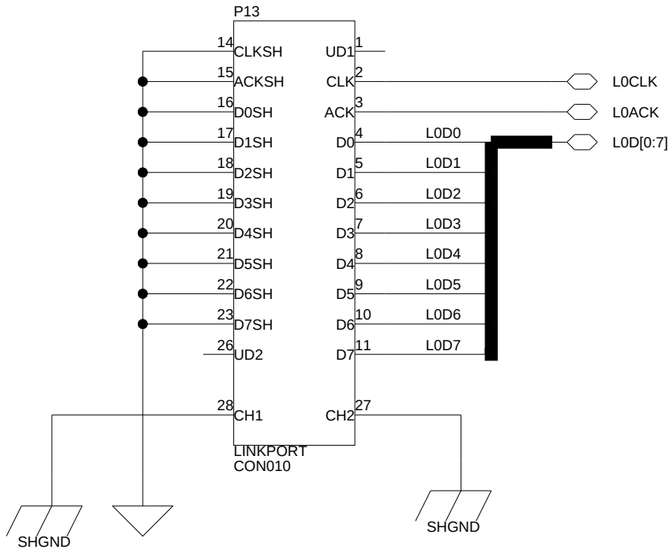
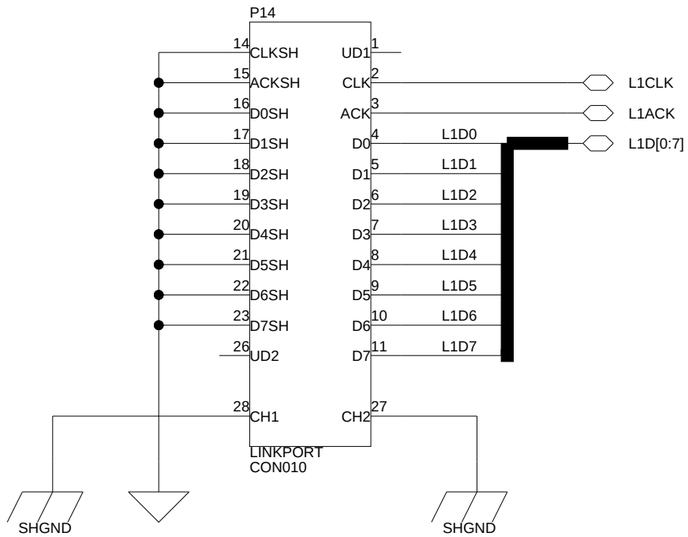
Title 21161N EZ-KIT LITE - EXPANSION HEADERS

Size	Board No.	Rev
B	A0157-2000	2.4

Date	Sheet
11-12-2002_17:12	20 OF 24

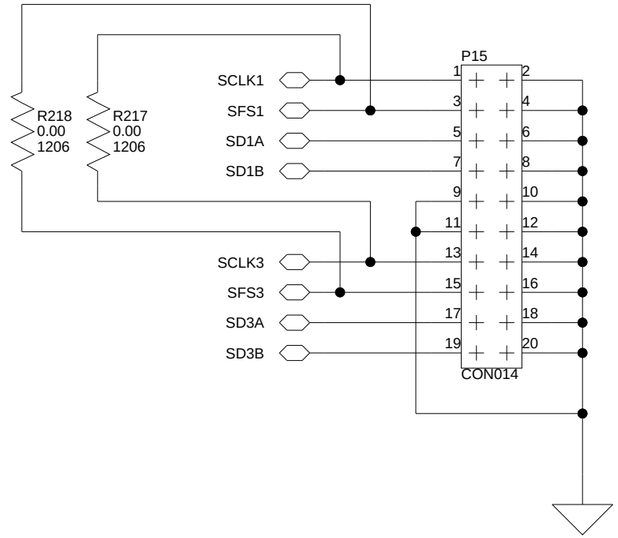
LINK PORT CONNECTORS

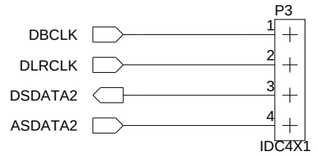




JP1 SHOULD NOT BE INSTALLED WHEN USING THE LINK PORT

SERIAL PORT CONENCTOR





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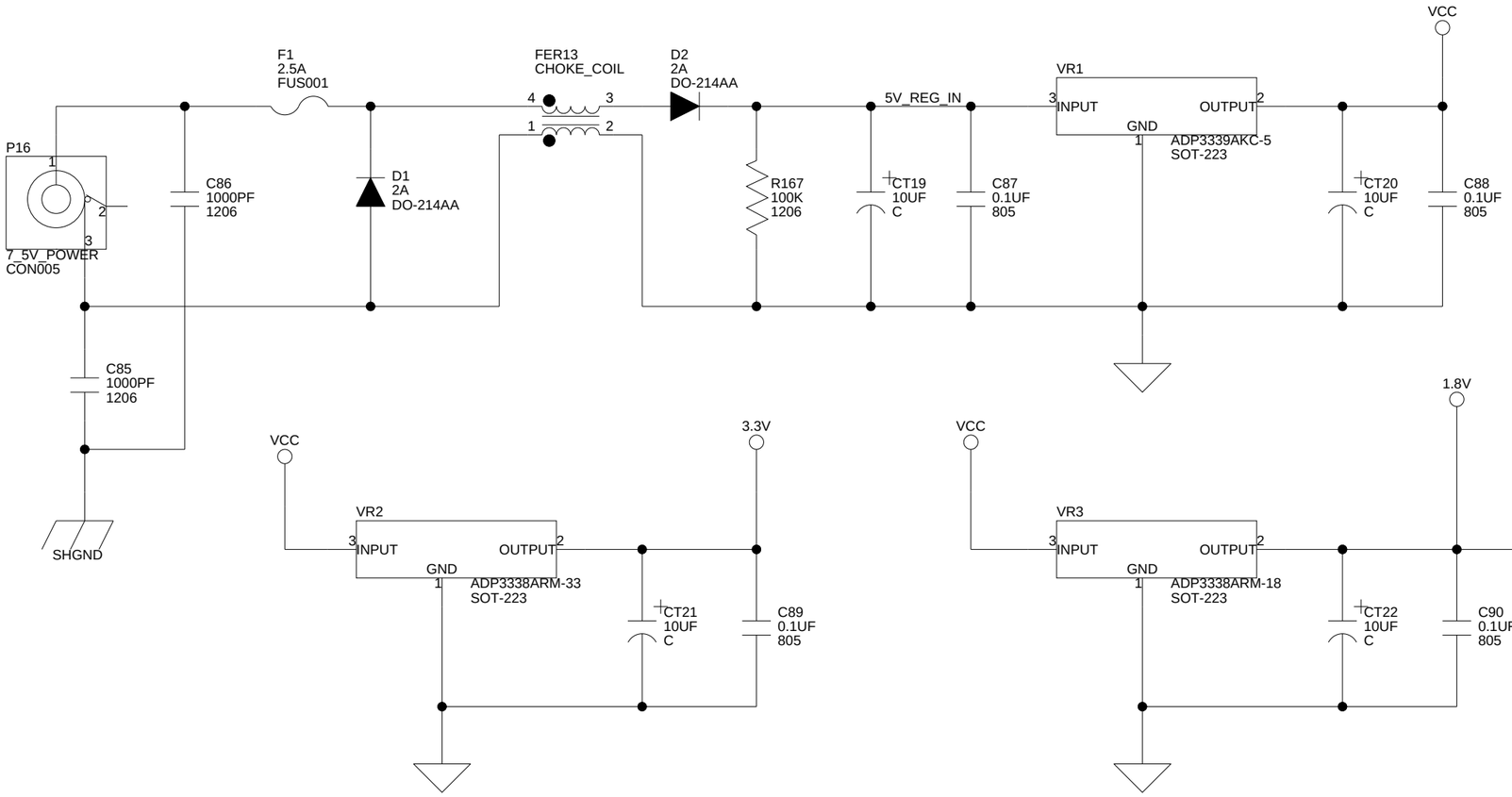
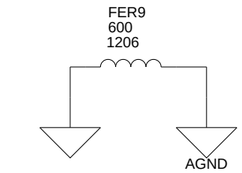
Engineering	

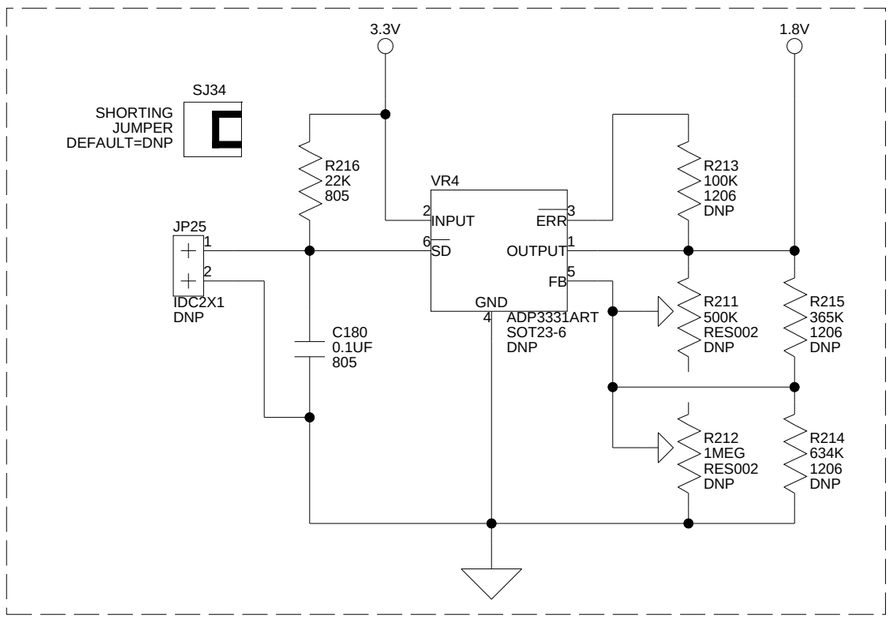
Title 21161N EZ-KIT LITE - LINK PORTS & SPORTS

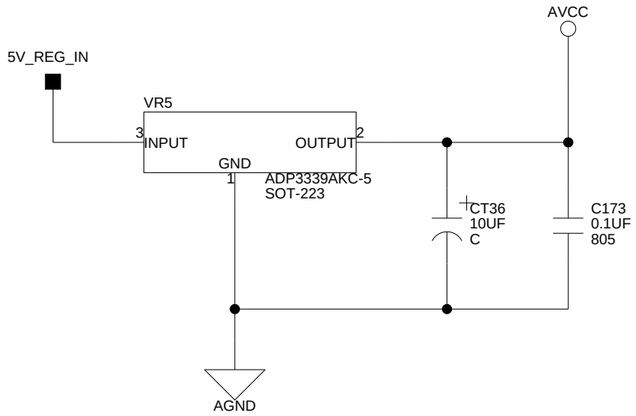
Size	Board No.	Rev
B	A0157-2000	2.4

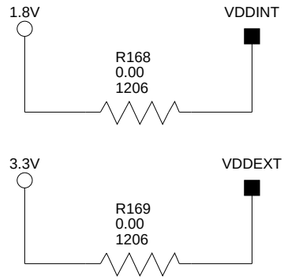
Date	Sheet
11-13-2003_11:39	21 OF 24











R168 & R169 ARE USED TO MEASURE CURRENT DRAW OF THE DSP

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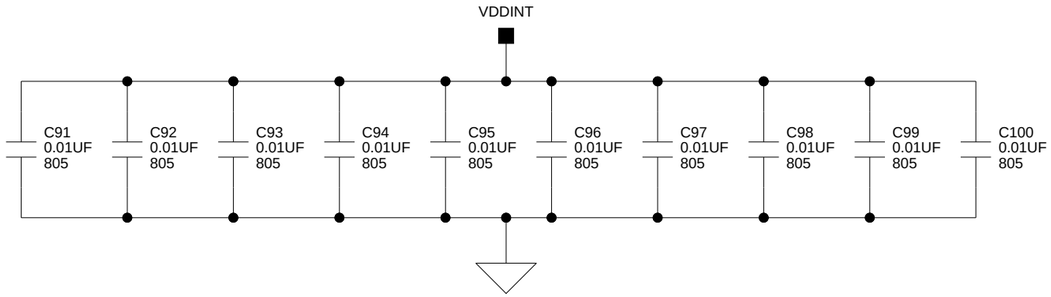
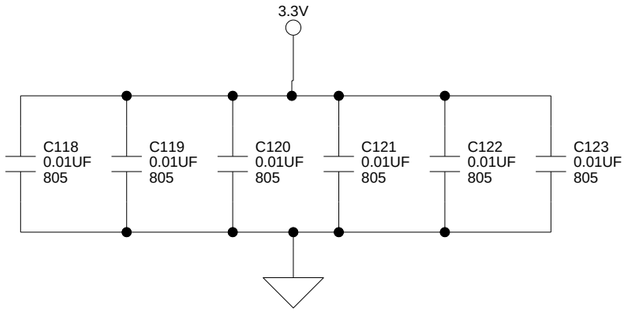
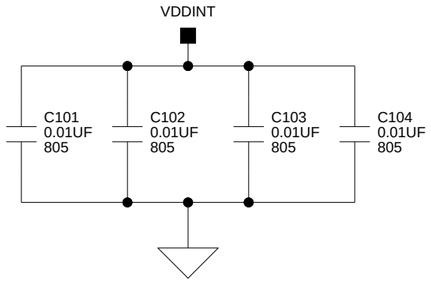
Title: 21161N EZ-KIT LITE - POWER

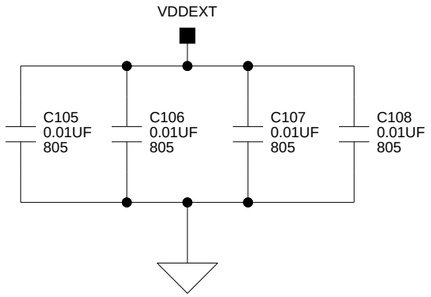
Size	Board No.	Rev
B	A0157-2000	2.4

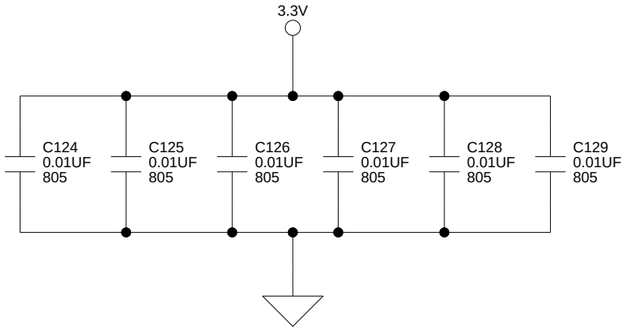
Date 2-19-2004_14:44 Sheet 22 OF 24

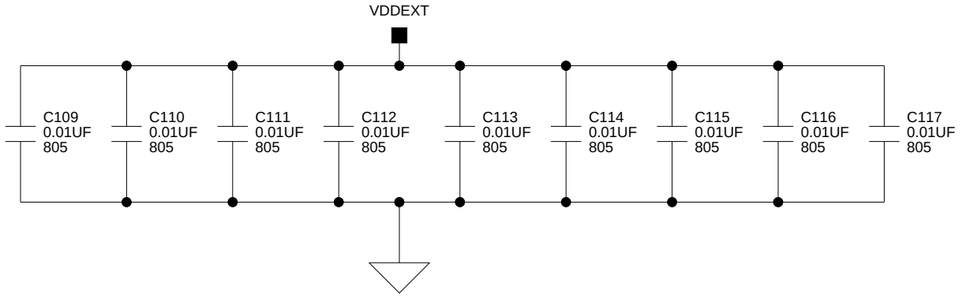




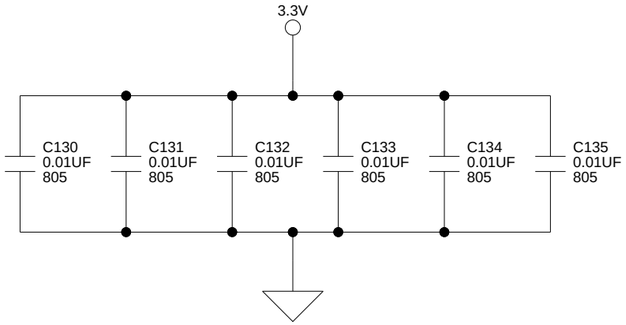




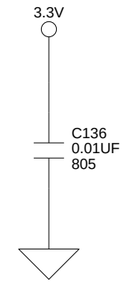




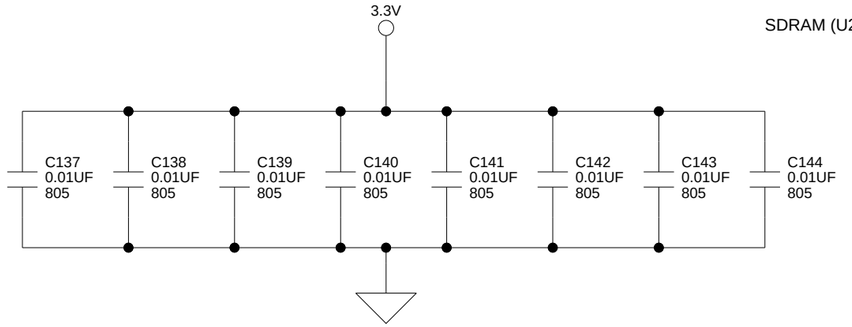
DSP (U1)



SDRAM (U2, U3, U4)



FLASH (U5)



USB INTERFACE (U6)

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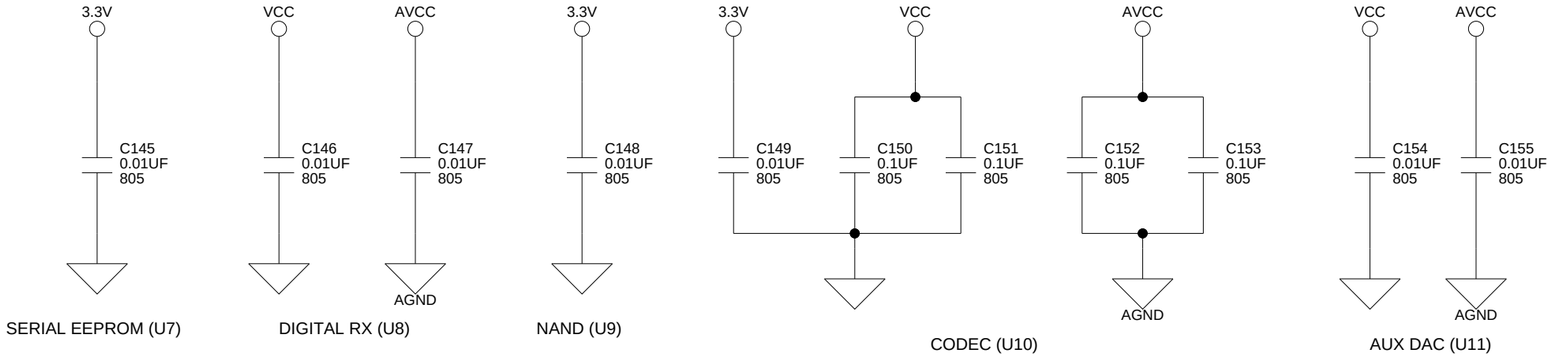
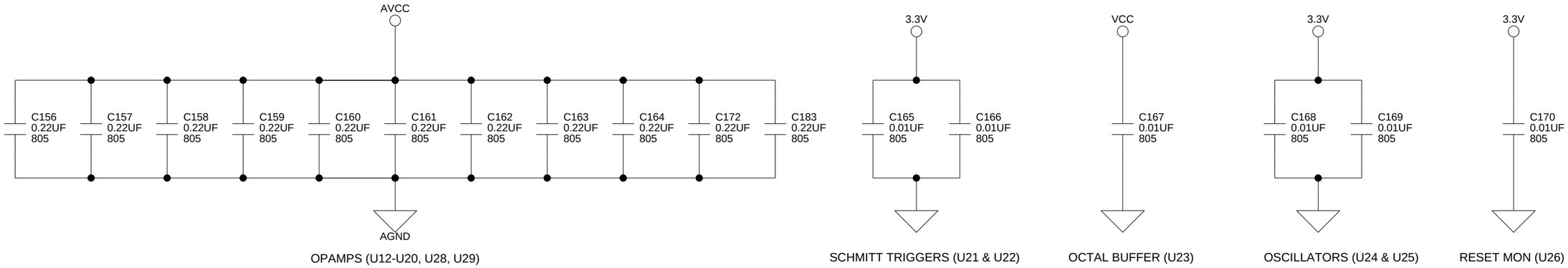
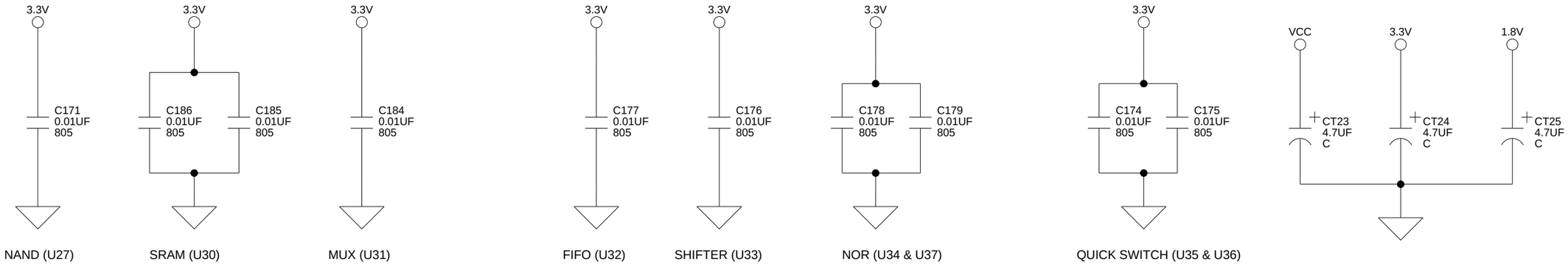
Title: 21161N EZ-KIT LITE - BYPASS CAPS 1

Size	Board No.	Rev
B	A0157-2000	2.4

Date 11-12-2002_17:12 Sheet 23 OF 24







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Title: 21161N EZ-KIT LITE - BYPASS CAPS 2

Size	Board No.	Rev
B	A0157-2000	2.4

Date: 11-12-2002_17:12 Sheet 24 OF 24

I INDEX

Symbols

~BMS, memory select pin, 2-2, 3-3
~MS0, memory select pin, 2-2, 3-3
~MS1, memory select pin, 2-2, 3-3

A

abort, hang operations, 2-12
acknowledge, hang operation, 2-12
AD1836, xii, 2-6, 3-3, 3-4, 3-6
  control registers, 3-12
  MIC1 input channel, 3-4
  SPI port, 2-7
  SPI select pin, 2-5
AD1852, xii, 2-7, 3-4, 3-6
  sampling frequency, 3-7
  SPI port, 2-7
  SPI select pin, 2-5
ADC1 input selector (JP11), 3-9
ADC2 mode selection (JP7, JP8), 3-8
Add New Hardware Wizard, Windows 98, 1-7
ADSP-21161N processor
  boot modes, 3-10
  clock jumper (JP21), 3-11
  core speed, 3-3
  core voltage, 3-2
  external voltage, 3-2
  ID jumper (JP19), 3-10
  internal memory restrictions, 2-2
  interrupt pins, 2-6
  memory map, 2-2
  reset, 2-5
  SPI port, 2-7
analog audio
  input, 2-6
  interface, xii
asynchronous FLAGs, 2-5
audio
  connectors (P4-8, P17), 3-18
  input, 2-6, 3-3
  interface, 2-6
  output, 2-8, 3-3
  stream, 3-14

B

bill of materials, A-1
BMS pin
  enabling (JP22), 3-12
  see ~BMS, select pin
board measurements, 3-21
boot
  code, xiii
  load, 2-9
  memory select pin (~BMS), 3-3, 3-12

memory space, 2-2
mode select (JP20), 3-10
breadboard area, xiii
breakpoints, 2-12

C
clear, hang operations, 2-12
CLK_CFG pins, 3-11
CLKDBL pins, 3-11
clock
frequency, 3-11
mode jumper (JP21), 3-3, 3-11
modes, 3-11
common attributes, hardware breakpoints, 2-13
configuring SDRAM, 2-3
connecting, EZ-KIT Lite board, 1-5
connectors, -xii, 1-5, 3-16
JP11 (analog audio input), 2-6
JP2 (digital audio input), 2-6
P10 (external port), 2-5, 2-6, 3-3, 3-19
P12 (JTAG header), 3-19
P13 (link port), 3-19
P14 (link port), 3-19
P15 (SPORT1, SPORT3), 3-20
P16 (power), 1-5, 3-20
P2 (USB), 1-6, 3-16
P4 (optical input), 2-6, 3-5
P5 (mono jack), 2-6, 3-5
P6 (mono jack), 2-6, 3-4, 3-9
P7 (stereo jack), 2-6, 3-4, 3-9
P9 (external port), 3-3, 3-18
contents, EZ-KIT Lite package, 1-1
conventions, manual, -xxi
converters, 2-7
core
clock ratio, 3-11
hang conditions, 2-11
voltage, 3-21
CS8414 digital receiver, 2-7, 3-5, 3-14
clock signals, 2-7
synchronization signals, 2-7
customer support, xvi

D
data hardware breakpoints, 2-15
Device Manager window, 1-15
digital
audio playback, 2-7
data, 2-7
stereo channels, 2-7
DSP signals, DAI_P, 3-15
DVD formats, 2-7

E
EBOOT pins, 3-10
electrostatic discharge, 1-2
emulator connector, xiii
enable attribute, 2-14
end address, attribute, 2-14
EPROM boot mode, 3-10, 3-12
example programs, 2-8
exclusive, attribute, 2-14
expansion connector footprints, xiii
external
data bus, 3-5
interrupts, 2-6

memory, EZ-KIT Lite, 2-3
port clock ratio, 3-11
port connectors, 3-3
port interface, xiii, 3-3
port signals, 3-18, 3-19
EZ-KIT Lite board
architecture, 3-2
features, xii
specifications, 3-21

F

features, EZ-KIT Lite board, -xii
FLAG
directing, 2-5
pins, 2-5, 3-15
registers, 2-5
FLAG0, 2-5, 3-12, 3-15
enable jumper (JP4), 3-7
FLAG1, 2-5, 3-12, 3-15
enable jumper (JP5), 3-7
FLAG10, 2-5
FLAG11, 2-5
FLAG2, 2-5, 3-15
FLAG3, 2-5, 3-15
FLAG4, 3-14
FLAG4-9, 2-5, 3-14
FLAG5, 3-14
FLAG6, 3-14
FLAG7, 3-14
FLAG8, 3-14
FLAG9, 3-14
flash
memory, xii, 2-2, 3-3, 3-12
programmer, 2-8
Found New Hardware Wizard
Windows 2000, 1-13
frequency jumper (JP6), 3-7

G

general-purpose IO, xiii
global options, hardware breakpoints, 2-13
graphical user interface (GUI), 2-9

H

hard reset, 2-9
hardware breakpoints, 2-12, 2-17, 2-18
dialog box, 2-13
Help, online, xix, 2-8
host
processor booting, 3-10
processor interface, xiii, 3-3
processor interface connector (P10), 3-19
hung conditions, 2-11

I

I2S mode, 2-7
ignore, hang operations, 2-12
input clock, 3-2
installation, summary, 1-3
installing
EZ-KIT Lite USB driver, 1-6
VisualDSP++ and EZ-KIT Lite license, 1-4
VisualDSP++ and EZ-KIT Lite software, 1-4
instruction hardware breakpoints, 2-16

interface connectors, xiii
interfaces
  see graphical user interface (GUI)
internal memory, EZ-KIT Lite, 2-3
interrupt
  pins, 2-6
  push buttons, xiii
  see also push buttons
IO
  input push buttons (SW1-4), 3-15
  pins see FLAGs
  voltage, 3-21
IRQ0-2 pins, 2-6, 3-16

J
JTAG
  connector (P12), 3-19
  emulation port, 3-5
  emulator, 3-19
jumper settings, 1-5
jumpers, 2-7
  JP1 (SDRAM disable), 3-5
  JP10 (microphone), 3-8
  JP11 (audio in), 3-4, 3-9
  JP19 (processor ID), 3-10
  JP2 (SPDIF), 3-5
  JP20 (boot mode), 3-10
  JP21 (clock), 3-11
  JP22 (~BMS), 3-12
  JP26 (SW1 enable), 3-12
  JP27 (SW2 enable), 3-12
  JP3 (MCLK source), 3-6
  JP6 (frequency), 3-7
  JP7 (ADC2), 3-8
  JP8 (ADC2), 3-8
  JP9 (microphone), 3-8

L
latency, 2-18
LBOOT pins, 3-10
LEDs, xiii, 1-5, 2-5, 3-13, 3-14
  LED1 (reset), 1-5, 3-14
  LED10 (USB monitor), 1-15, 1-16, 3-15
  LED11 (power), 1-5, 3-15
  LED2 (FLAG9), 3-14
  LED2-LED7 (FLAGs), 3-14
  LED3 (FLAG8), 3-14
  LED4 (FLAG7), 3-14
  LED5 (FLAG6), 3-14
  LED6 (FLAG5), 3-14
  LED7 (FLAG4), 3-14
  LED8 (DSP reset), 1-5, 1-14, 3-14
  LED9 (VERF), 2-8, 3-14
line-in
  input channel, 3-4
  jacks, 2-7
line-out jacks, 2-8
link port, 3-5, 3-10
  booting, 3-11
  connectors, 3-19

M
MCLK, selecting (JP3), 3-6
measurements, EZ-KIT Lite, 3-21
memory
  restrictions, 2-2
  select pins, 3-3

microphone
  circuit, 3-8
  jacks, 2-7
mode, attribute, 2-14
MODE2 register, 2-5

N
no-boot mode, 3-11, 3-12

O
oscillator, 3-11
  surface-mount, 3-2
  through-hole, 3-2
  through-hole crystal, 3-2

P
package contents, 1-1
PC configuration, 1-3
power
  connector (P16), 3-20
  LED (LED11), 3-15
  specifications, 3-21
  supply, 3-21
processor external memory, see
    ADSP-21161N processor
programmable FLAGs
  see FLAGs
push buttons, xiii, 2-6, 3-13, 3-15
  SW1 (FLAG0), 3-15
  SW2 (FLAG1), 3-15
  SW3 (FLAG2), 3-15
  SW4 (FLAG3), 3-15
  SW5 (IRQ0), 3-15
  SW6 (IRQ1), 3-15
  SW7 (IRQ2), 3-15
  SW8 (reset), 3-16

R
RCA jacks, 2-7, 3-3
registering, this product, 1-2, 1-4
reset
  board, 2-9
  hang operation, 2-12
  processor, 3-14
  push button (SW8), 3-16
retry, hang operation, 2-12

S
sample frequencies, 2-7
SDRAM
  configuration, 2-3
  control registers, 2-3
  disabling (JP1), 3-5
  memory, 2-2, 2-3, 3-3
semiconductor receiver, xii
serial booting, 3-10, 3-12
setting
  breakpoints, 2-18
  EZ-KIT Lite hardware, 1-5
  target options, 2-9
SMT footprints, xiii
SPDIF
  connectors, 3-14
  modes, 3-7
  selecting (JP2), 3-5
specifications, 3-21
SPI
  audio interface, 3-4

port, 3-4, 3-12
select pin, 2-5
SPORT
audio interface, 3-3
connectors, 3-3
SPORT0, xiii
SPORT1, xiii, 3-12, 3-20
SPORT2, xiii
SPORT3, xiii, 3-20
SRAM memory, 2-2
start address, attribute, 2-14
starting VisualDSP++, 1-16
stereo
jack (P7), 2-6, 3-3
output channels, 2-6
SW1 (FLAG0) push button, 2-5
SW1 (JP26) enable push button, 3-12
SW2 (FLAG1) push button, 2-5
SW3 (FLAG2) push button, 2-5
SW4 (FLAG3) push button, 2-5
SW5 (interrupt) push button, 2-6, 3-16
SW6 (interrupt) push button, 2-6, 3-16
SW7 (interrupt) push button, 2-6, 3-16
SW8 (reset) push button, 1-14
system
architecture, EZ-KIT Lite board, 3-2
requirements, PC, 1-3

T

target options
dialog box, 2-9
miscellaneous, 2-10
on emulator exit, 2-10
while target is halted, 2-10

U

UART, 3-11
USB
cable, 1-2
connector (P2), 3-16
debug interface, 3-19
driver installation, Windows 2000, 1-11
driver installation, Windows 98, 1-7
driver installation, Windows XP, 1-12
interface, 3-14, 3-16
monitor LED (LED10), 3-15
user
input, 2-5
output, 2-5

V

VERF flag (LED9), 2-8, 3-14
verifying USB driver installation, 1-14
VisualDSP++
documentation, xix
installation, 1-4
license, 1-4
online Help, xix
requirements, 1-3
starting, 1-16
voltage regulators, xiii