Mixed-Signal Control Processor with ARM Cortex-M4 and 16-Bit ADCs

Silicon Anomaly List

ADSP-CM402F/CM403F/CM407F/CM408F/CM409F

ABOUT ADSP-CM402F/CM403F/CM407F/CM408F/CM409F SILICON ANOMALIES

These anomalies represent the currently known differences between revisions of the ADSP-CM402F/CM403F/CM407F/CM408F/CM409F product(s) and the functionality specified in the ADSP-CM402F/CM403F/CM407F/CM408F/CM409F data sheet(s) and the Hardware Reference book(s).

PRODUCT REVISIONS

A product revision letter with the form "-x" is branded on all parts. The implementation field bits <31:28> of the JTAG0_IDCODE register can be used to differentiate the revisions as shown below.

Product REVISION	JTAG0_IDCODE<31:28>	Analog Front End (AFE) ID*
H	0x2	0x3

*= The adi_adcc_ReadAFEID API software driver can be used to read Analog Front End ID

ANOMALY LIST REVISION HISTORY

The following revision history lists the anomaly list revisions and major changes for each anomaly list revision.

Date	Anomaly List Revision	Data Sheet Revision	Additions and Changes
08/03/2020	I	Rev A	Modified Anomaly: 17000089
02/26/2020	H	Rev A	Added Anomaly: 17000089
12/08/2015	G	Rev A	Added Anomalies: 17000033, 17000051, 17000052, 17000053, 17000054, 17000056
05/19/2015	F	PrG	Added Anomalies: 17000029, 17000030, 17000031
04/02/2015	E	PrG	Added Anomalies: 17000027, 17000028
12/15/2014	D	PrF	Added Anomalies: 17000026
10/7/2014	C	PrF	Added Anomalies: 17000025
08/26/2014	B	PrF	Added Anomalies: 17000004, 17000013, 17000015, 17000019, 17000020, 17000021, 17000022, 17000023, 17000024
09/17/2013	A	PrE	Initial Version

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SUMMARY OF SILICON ANOMALIES

The following table provides a summary of ADSP-CM402F/CM403F/CM407F/CM408F/CM409F anomalies and the applicable product revision(s) for each anomaly.

No.	ID	Description	Rev H
1	17000013	Setup Time of USB0_ID Signal Deviates from All Other System Input Specifications	x
2	17000015	ADCC Collision Status Is Indicated for Only One ADC in Simultaneous Sampling Mode	x
3	17000021	SPI Slave Enable Output Not Driven Properly When Controlled by Software	x
4	17000025	TIMER_DATA_ILAT Bit Is Set in EXTCLK Mode When TIMER_TMRn_CNT Rolls Over to 1	x
5	17000027	RCU0_SRRQSTAT Register Is Not Affected by TRU's System Reset Request	x
6	17000028	ECC Logic in Analog Front End Does Not Trigger a Fault	x
7	17000029	SPI Data Pins Are Internally Pulled High in Open-Drain Mode	x
8	17000031	SPORT May Drive Data Pins During Inactive Channels in Multi-Channel Mode	x
9	17000033	SMC Byte Enable Signals Tri-State during Read Operations	x
10	17000056	Slave Boot Modes Do Not Support Flash Bulk Erase Requests	x
11	17000089	Internal Voltage Regulator Does Not Regulate VDD_INT to Specified Voltage	x

Key: x = anomaly exists in revision
. = Not applicable

DETAILED LIST OF SILICON ANOMALIES

The following list details all known silicon anomalies for the ADSP-CM402F/CM403F/CM407F/CM408F/CM409F including a description, workaround, and identification of applicable product revisions.

1. 17000013 - Setup Time of USB0_ID Signal Deviates from All Other System Input Specifications:

DESCRIPTION:
The tSSYS (System Inputs Setup before TCK High) timing parameter for the **USB0_ID** signal is 30 ns, as opposed to the 12 ns specification given for all system inputs. As the **USB0_ID** pin is statically controlled (connected to GND in host mode and left floating in device mode), the long setup requirement does not have any implications.

WORKAROUND:
None.

APPLIES TO REVISION(S):
H

2. 17000015 - ADCC Collision Status Is Indicated for Only One ADC in Simultaneous Sampling Mode:

DESCRIPTION:
When in simultaneous sampling mode, if one event undergoes a collision (indicating the event is delayed), its paired event is also delayed. Ideally, the collision status should be reflected for both the paired events.

However, the collision status is reflected only for the event which initiated the collision when all the following conditions are true:

1. TIMER1 initiates a pair of simultaneous sampling events.
2. A TIMER0 event occurs at the same time as that of the paired events.
3. The ADCs are not actively sampling.
4. The pending FIFO is empty.

WORKAROUND:
None.

APPLIES TO REVISION(S):
H

3. 17000021 - SPI Slave Enable Output Not Driven Properly When Controlled by Software:

DESCRIPTION:
The SPI Slave Enable signal can be controlled via software by setting the required value in the Slave Select Register. However, this value is not driven on the SPI Slave Enable Signal when the Slave Select Register is written.

WORKAROUND:
Perform two back-to-back writes to the Slave Select Register to drive the signal to the required level.

APPLIES TO REVISION(S):
H

4. 17000025 - TIMER_DATA_ILAT Bit Is Set in EXTCLK Mode When TIMER_TMRn_CNT Rolls Over to 1:

DESCRIPTION:
When the timer is configured in External Clock mode and the **TIMER_TMRn_CNT** register reaches the value programmed in the **TIMER_TMRn_PER** register, the corresponding **TIMER_DATA_ILAT** bit should be set along with a trigger/interrupt being generated. However, the **TIMER_DATA_ILAT** bit is set after the **TIMER_TMRn_CNT** register rolls over to 1.

For example, if the **TIMER_TMRn_PER** register is configured to a value **n**, the first interrupt/trigger occurs after the timer receives **n+1** edges externally. After the first interrupt, subsequent interrupts correctly occur every **n** edges.

WORKAROUND:
For interrupts/triggers to occur at every **n** edges of the external clock, the **TIMER_TMRn_PER** register must be configured to **n-1** for the initial event and then reconfigured to **n** for subsequent events, as shown in the following pseudo-code:

```
TIMER_TMRn_PER = n-1;   // Configure PERIOD register with n-1
TIMER_RUN_SET = 1;      // Run the timer
TIMER_TMRn_PER = n;     // Configure PERIOD register with n
```

APPLIES TO REVISION(S):
H

5. 17000027 - RCU0_SRRQSTAT Register Is Not Affected by TRU's System Reset Request:

DESCRIPTION:
If a system reset request input from the TRU is active for only one SCLK period, then the corresponding status bits in the **RCU0_SRRQSTAT** register may not be set.

WORKAROUND:
None.

APPLIES TO REVISION(S):
H

6. 17000028 - ECC Logic in Analog Front End Does Not Trigger a Fault:

DESCRIPTION:
The hardware trigger of a fault is not implemented for Analog Front End Non-Volatile Configuration ECC errors.

WORKAROUND:
The following code checks the Analog Front End Non-Volatile Configuration ECC status:

```
*pREG_ADCC0_CTL = 0x0000;
while(*pREG_ADCC0_CFG & 0x01);
*pREG_SPU0_CTL = (uint32_t) (0x00000000);
*((volatile  uint32_t *) 0x40027010) = (uint32_t) (0x1e7b1c96);
*((volatile  uint32_t *) 0x40027010) = (uint32_t) (0xdff0c3b2);
__ISB();

*pREG_ADCC0_CTL  = (uint32_t) 0x00000001;

*((volatile  uint32_t *) 0x4000E404) = (uint32_t) (0x08000000);
while ((*((volatile  uint32_t *) 0x4000E404) & 0x00000001) != 0);
__ISB();
while ((*((volatile  uint32_t *) 0x4000E404) & 0xFF000000)!= 0x08000000);
int CFG_Reg = (*((volatile  uint32_t *) 0x4000E404) >> 1) & 0xFFFFFF;
if(CFG_Reg & 0x007F)
{
   "ECC error is detected, generate Fault"
}

*((volatile  uint32_t *) 0x40027010) = (uint32_t) 0x00000000;
*((volatile  uint32_t *) 0x40027010) = (uint32_t) 0x00000000;
__ISB();

*pREG_ADCC0_CTL  = 0x00;
while(*pREG_ADCC0_CFG & 0x01);
```

Run this code after Analog Front End initialization to trigger a fault if an ECC error has been detected.

APPLIES TO REVISION(S):
H

7. 17000029 - SPI Data Pins Are Internally Pulled High in Open-Drain Mode:

DESCRIPTION:
In open-drain mode, the SPI port is supposed to tri-state the output pins when the output data is logic high. However, due to internal pull-up resistors, the data pins are pulled high.

WORKAROUND:
None.

APPLIES TO REVISION(S):
H

8. 17000031 - SPORT May Drive Data Pins During Inactive Channels in Multi-Channel Mode:

DESCRIPTION:
When a SPORT operates in multi-channel mode, the transmitter tri-states the data pins during the inactive channels. When SPMUX functionality is enabled, under specific conditions, one SPORT half may continue to drive on the inactive channels when all the following conditions are true:

1. SPORT half "x" is configured as a transmitter (**SPORT_CTL_x.SPTRAN = 1**).
2. The frame sync is internally imported from the pairing half SPORT (**SPORT_CTL2_x.FSMUXSEL = 1**).
3. Multi-channel frame delay is zero (**SPORT_MCTL_x.MFD = 0**).
4. Window offset is zero (**SPORT_MCTL_x.OFFSET = 0**).
5. Channel0 of the multi-channel frame is enabled for transmit (**SPORT_CS0_x.CH0 = 1**).
6. Frame sync is active low (**SPORT_xCTL.LFS = 1**).
7. Frame sync edge detect bit is 0 (**SPORT_CTL_x.FSED = 0**).

When this exact configuration is used, the SPORT half transmitter drives the first bit of the next word to be transmitted once the number of channels specified in WSIZE expires. Therefore, the SPORT half may drive on inactive channels, which can cause contention when other transmitters are configured to drive on these inactive channels.

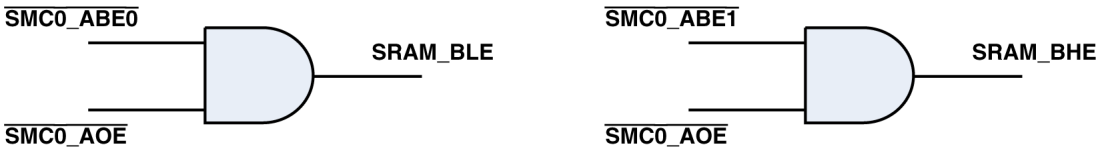
WORKAROUND:
If any of the listed conditions is false, the anomaly is avoided. As long as the system design can tolerate it, the least invasive configuration change with regards to timing would be to set the frame sync edge detect bit (**SPORT_CTL_x.FSED = 1**).

APPLIES TO REVISION(S):
H

9. 17000033 - SMC Byte Enable Signals Tri-State during Read Operations:

DESCRIPTION:
During SMC read operations, the byte enable signals (**$\overline{\text{SMC0\_ABE0}}$** and **$\overline{\text{SMC0\_ABE1}}$**) are tri-stated instead of being driven low. Therefore, when an 8-bit SMC write access is followed by a 16-bit or 32-bit read access, the read access may fail if the device requires active low byte enable signals during read operations.

WORKAROUND:
While interfacing with the external SRAM, the SRAM byte enable signals can be driven low during read operations using external logic as shown in the figure.



For SMC read operations, the **$\overline{\text{SMC0\_AOE}}$** signal is low. This drives the **$\overline{\text{SRAM\_BHE}}$** and **$\overline{\text{SRAM\_BLE}}$** signals low.
This external logic does not affect the SMC write operations, as the **$\overline{\text{SMC0\_AOE}}$** signal is high during write operations.

APPLIES TO REVISION(S):
H

10. 17000056 - Slave Boot Modes Do Not Support Flash Bulk Erase Requests:

DESCRIPTION:
When the security header is corrupted with the key field being the default key, debug access is not granted due to the detection of an invalid header. However, slave boot modes detect a valid header with the default key and expect a non-secure boot instead of a mass erase request.

This locks out the debugger, and the device cannot be recovered through bulk erase via slave boot mode. However, in this event, slave boot mode is a non-secured boot, as the default key settings allow a new application to be booted and loaded to the flash.

When the security header is corrupted with the key field being the user key, the slave boot modes detect an invalid header and expect a bulk erase command, allowing flash recovery.

WORKAROUND:
To recover the flash:
1. Boot an application via the slave boot mode to SRAM to erase the flash.
2. Load a new application to the flash using the supported flash programmer utility that contains a valid security header. This indirectly erases the corrupt security header and loads the correct header.

APPLIES TO REVISION(S):
H

11. 17000089 - Internal Voltage Regulator Does Not Regulate VDD_INT to Specified Voltage:

DESCRIPTION:
The internal LDO voltage regulator is designed to provide a nominal VDD_INT voltage of 1.20V. Transient bursts of activity during run time can cause the internally regulated VDD_INT level to violate the minimum VDD_INT datasheet specification, thus leading to unreliable operation. The voltage level to which VDD_INT drops is unpredictable and depends on the level of core, memory, and peripheral activity.

This anomaly applies to all packages.

WORKAROUND:
Use an external voltage regulator to supply VDD_INT.

APPLIES TO REVISION(S):
H