

How to Easily Achieve Superior Audio Performance with Plug and Play Digital Input Class D Amplifiers

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Abstract

This article introduces a family of plug and play Class D amplifiers that simplifies a system design by eliminating the usual need for I²C programming, low jitter sample clocks, logic level shifters, careful board design, or EMI filtering. It will explain how to deliver high performance audio while saving on board space, cost, and effort.

Introduction

A new generation of plug and play digital input Class D audio amplifiers achieves audio performance that is far superior to traditional analog Class D amplifiers. More importantly, digital input Class D amplifiers provide additional benefits of reduced power, complexity, noise, and system cost.

Electronics vendors commonly use high efficiency, filterless, analog input Class D amplifiers to manage the power requirements of portable audio speakers found in cell phones, tablet computers, home monitoring, and smart speakers. These Class D amplifiers allow direct connection to a battery that minimizes losses and reduces component count. The amplifiers also achieve >80 dB PSRR performance, which is important to avoid audible buzzing with 217 Hz demodulated GSM signals.

Analog input Class D amplifiers normally require a DAC and line driver amp on the application processor (Figure 1), and this adds die cost, power, and noise to the speaker output. These Class D amplifiers also require careful board design to avoid degradation because of signals coupling onto the analog board routes.

Digital input Class D audio amplifiers are immune to most board design issues. Single-channel Class D amplifiers can be placed at remote locations on a board to minimize the routing of the high current battery and speaker load connections. These amplifiers do not need the DAC and line driver amp of analog input Class D designs. Thus, the space and system costs drop, and designs are simpler.

Simplified System Design

Most digital input amplifiers accept pulse-code modulated (PCM) or I²S data, which requires three wires: BCLK, LRCLK, and DIN. The PCM data format does not require a modulator or upsampling of the data on the application processor (Figure 2). Some older implementations of PCM input amplifiers also require a clean master clock (MCLK) to derive a jitter-free sampling clock. Newer PCM input amplifiers like the [MAX98357](#), [MAX98360](#), and [MAX98365](#) no longer require the MCLK input so the pin count, power consumption, and board complexity are all reduced.

Older digital input amplifiers offer adjustable sample rate and/or bit depth that, in some cases, require complex programming of the amplifier. Newer generations of digital input amplifiers automatically detect a wide range of sample rates and bit depths to self-configure without any programming.

In a multichannel implementation, the digital input Class D audio amplifier reduces the number of external capacitors and routed lines on the board. Only BCLK, LRCLK, and DIN lines are needed for PCM inputs to provide stereo or 8-channel TDM data. As a comparison, a stereo analog input Class D amplifier will normally require two differential input signals (four wires) to be routed with AC-coupling capacitors (see figures 1 and 2).

Most digital input amplifiers require both a low digital-supply voltage (1.8 V) and a high speaker-supply voltage (2.5 V to 5.5 V). Now the board design and component count can be simplified by using a single-supply Class D amplifier like the [MAX98357](#) and [MAX98360](#). The [MAX98365](#) can run from a single 3.0 V to 5.5 V supply or one supply at 1.8 V to 5.5 V and the other at 3.0 V to 14.0 V. The digital input logic voltage is independent of the supply voltages on these parts. The input logic can be anywhere from 1.2 V to 5.5 V, which eliminates any need for logic level shifters.

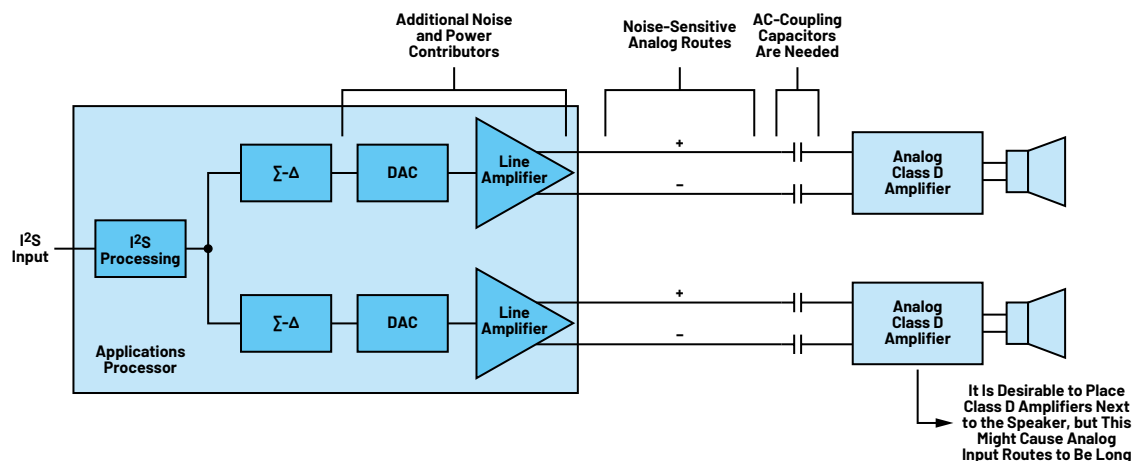


Figure 1. A conventional system with analog input Class D speaker amps. The DAC and line driver amp on the application processor add die cost, power, and noise to the speaker output.

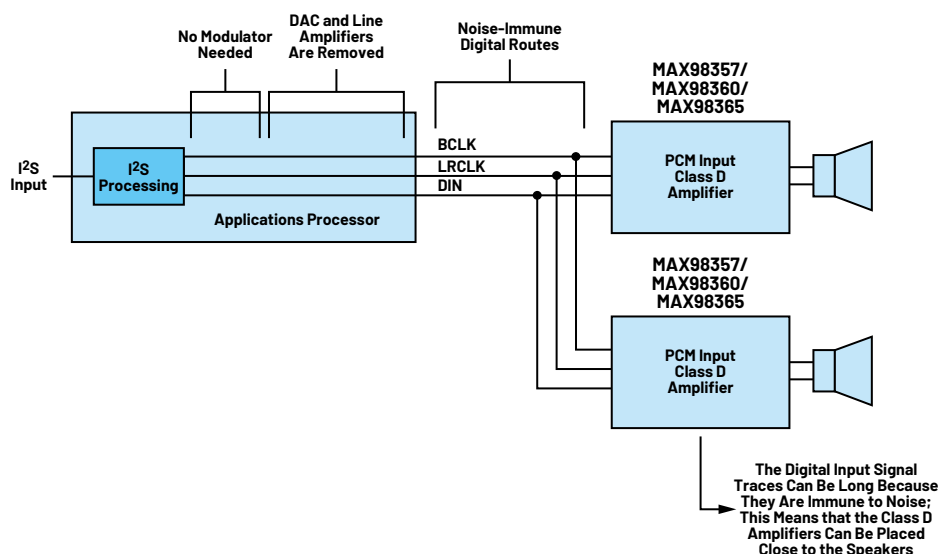


Figure 2. A system with a PCM input Class D speaker amp uses three wires but does not require a modulator or upsampling of the data on the application processor.

Jitter Tolerance and Clock Generation

Digital input Class D audio amplifiers usually present a new challenge for clock jitter. For good audio quality, most digital input amplifiers require fairly low levels of jitter on BCLK or MCLK. The jitter tolerance is often not quoted in the data sheet; when jitter tolerance is quoted, the typical specification is ~200 ps of rms jitter. High levels of clock jitter will typically degrade either the amplifier's dynamic range or the full-scale THD + N performance.

In many systems, the reference oscillator for the application processor is not a convenient multiple of the BCLK, so providing a low jitter clock for the amplifier is not easy. For example, 13 MHz is a common crystal frequency used for GSM phones and 27 MHz is commonly used in video solutions. Neither of these reference

frequencies is a convenient multiple of the 44.1 kSPS or 48 kSPS audio sample rates. These systems will, therefore, often implement a complicated fractional-N PLL to create the clock for the audio. In some cases, the solution will require a separate audio reference oscillator, which increases complexity and bill of materials (BOM).

An alternative and preferable solution is a digital input amplifier that can tolerate high clock jitter without degrading the audio performance. Such an amplifier will reduce system complexity. In the simplest case, a cycle-skipping clock can be used to generate BCLK, but this generates extraordinarily high jitter. If a 13 MHz reference clock is cycle skipped to create a 6.144 MHz BCLK (48 kSPS × 128 OSR), then the peak jitter will be 38.4 ns and the rms jitter will be 22.2 ns (Figure 3). This represents two orders of magnitude higher jitter than most DACs can tolerate.

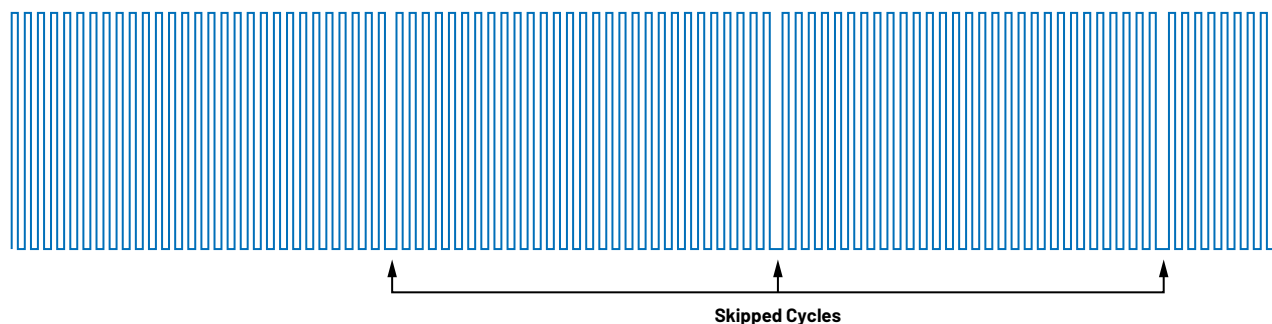


Figure 3. A 12.288 MHz MCLK from a cycle-skipped 25 MHz clock.

These new Class D audio amps, however, still produce >103 dB dynamic range performance with this amount of clock jitter. A cycle-skipped clock can be created with a small number of digital gates on the application processor. The new devices do not need the oscillator or a loop filter that would otherwise be required in a PLL solution. See Figure 4.

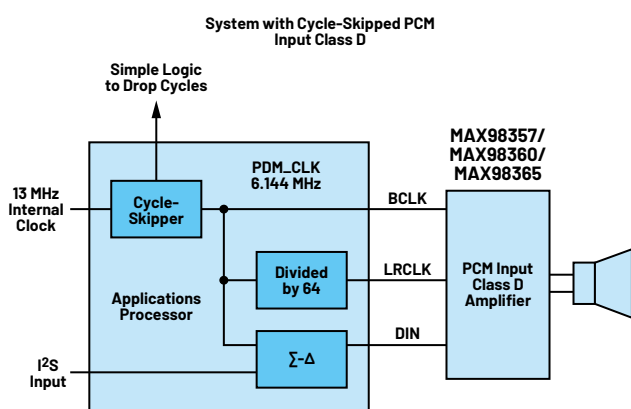


Figure 4. Fractional-N PLL vs. cycle-skipped clock implementations.

Jitter Tolerance Test Results

Test results show that the MAX98357, MAX98360, and MAX98365 dynamic range does not degrade with the cycle-skipped jittered clock. These parts outperform the 120 dB DAC by more than 20 dB with the jittered clock. Further details on jitter tolerance in sigma-delta DACs can be found in a companion article.¹



About the Author

Matt Felder joined Analog Devices in 2009 as an analog design engineer. His work includes audio DACs, audio ADCs, multichannel SAR ADCs, audio amps, a video DAC, an FM radio receiver, and a multiformat battery charger. Matt is a senior member of the IEEE and has 47 issued patents. He has a B.S.E.E. from Texas A&M and an M.S.E.E. from UT Austin.

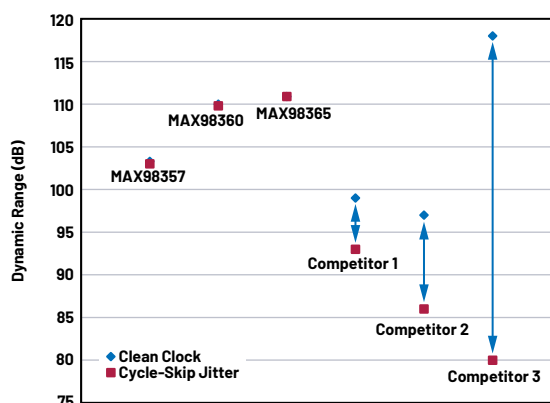


Figure 5. Dynamic range degradation with 11.5 ns rms cycle-skipped clock jitter.

Conclusion

Digital input filterless Class D audio amplifiers allow simple board-level implementation with no I²C, no MCLK, no level shifting, and no EMI filtering. They provide high efficiency, low EMI, and high output power. The MAX98357 and MAX98360 are available in a WLP or QFN package and can produce 3.2 W of output power. The MAX98365 is available in a WLP package and can produce 17.6 W of output power.

Reference

¹Matt Felder, Patrick Gallagher, and Brian Donoghue. "Analyzing Audio DAC Jitter Sensitivity." EDN Network, September, 2012.