

# What Are the Most Important Timing Factors for Low Power Precision Signal Chain Applications? Part 1

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## Abstract

This article explains timing factors and solutions for reducing power while maintaining precision in low power systems, as required for measurement and monitoring applications. It explores analog front-end timing, ADC timing, and digital interface timing. It will also give examples of analysis control evaluation (ACE) timing tools to aid system designers and software engineers visualize impacts or settings on measurement timing. Part 1 begins with an overview of the two main ADC types, and it will focus primarily on sigma-delta architecture. Considerations related to SAR ADC architecture will be covered in Part 2.

## Introduction

"Time is of the essence"—an old idiom that could be applied to any field but, when applied to the sampling of real-world signals, it is a pillar of our engineering discipline. When attempting to lower power, meet timing targets, and maintain performance requirements, consideration must be given to the type of ADC architecture chosen in measurement signal chains, sigma-delta, or successive approximation register (SAR). Once a particular architecture is chosen, system designers create the circuit needed to obtain the necessary system performance. At this point, designers need to consider the most important timing factors for their low power precision signal chain.

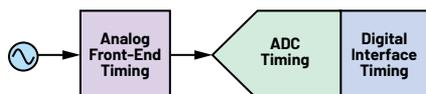


Figure 1. The signal chain timing considerations.

## The Need for Speed: SAR or Sigma-Delta for Low Power Signal Chains?

We will be focusing on precision low power measurements and signals (such as temperature, pressure, and flow) with measurement bandwidths of below 10 kHz (see [Precision Low Power](#) for more details), although a lot of the topics covered in this article can be applied for wider bandwidth measurement systems.

When exploring low power systems, historically, a designer would choose sigma-delta ADCs for higher precision measurements of slow moving signals. SARs were seen as more useful for higher speed measurements where more channels were converted but new SARs such as the [AD4630-24](#) are entering the high precision space traditionally associated with sigma-delta ADCs, so it is not a hard and fast rule. To give real-world examples of the ADCs' architectures, let us look at two low power offerings when considering the timing associated with ADC signal chain architectures, the [AD4130-8](#) sigma-delta ADC and the [AD4696](#) SAR ADC shown in Table 1.

Table 1. Ultra Low Power ADCs

	AD4130-8	AD4696
Architecture	Sigma-delta ADC	SAR ADC
Channels	16	16
Resolution	24-bit	16-bit
Max Speed	2.4 kSPS	1 MSPS
Current Consumption	Converting: 32 $\mu$ A at 2.4 kSPS Standby: 0.5 $\mu$ A	Converting: 58 $\mu$ A at 10 kSPS Standby: 2 $\mu$ A
Low Power Features	Duty cycling FIFO	Dual-SDO autocycling

## Sample Frequency or Output Data Rate?

SAR converters take a sample of the input and capture the signal level at a known point in time. After the initial sample (and hold) phase, there is a conversion phase. The time it takes to reach the result is largely based on the sampling frequency.

Sigma-delta converters take samples at a modulator frequency. The modulator oversamples and the sample rate is much higher than the Nyquist frequency of the input signal. The additional frequency span allows the noise to be shifted to higher frequency. The ADC then uses a process called decimation on the modulator output where it reduces the sample rate in exchange for higher precision. It is done through digital low-pass filters, equivalent to averaging in the time domain.

As there is a difference in the way that the technologies reach the conversion result, the SAR-based documentation will refer to the sample frequency ( $f_{\text{SAMPLE}}$ ) while sigma-delta data sheets will concentrate on the output data rate (ODR). We will guide the reader with the distinction between both as we discuss the architectures in more detail with respect to time.

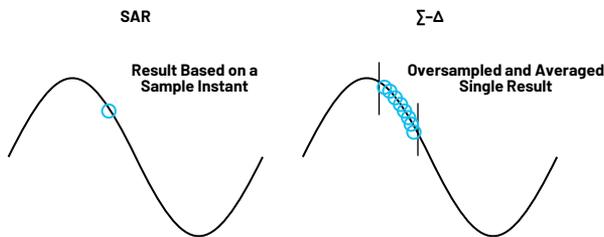


Figure 2. A SAR ( $f_{\text{SAMPLE}}$ ) vs. sigma-delta (ODR).

With multiplexed ADCs that perform one conversion on multiple channels, the amount of time it takes to perform conversions on all the channels (including setup times, etc.) is referred to as the throughput rate.

The first timing consideration for a signal chain is the time it takes to bias/excite the sensor and power up the signal chain. Voltage and current sources will have to turn on, sensors biased, and start-up time specifications considered. The turn on settling time for the AD4130-8 on-chip reference is 280  $\mu\text{s}$  for a specific load capacitance on the reference pin, for example. The on-chip bias voltage, which can be used to excite sensors, has an associated start-up time of 3.7  $\mu\text{s}$  per nF but this is dependent on the amount of capacitance attached to the analog input pins.

After power-up times in the signal chain are investigated, we need to look at timing considerations that apply depending on the ADC architecture. We will begin the next section of the article by focusing on measurement signal chains that have sigma-delta ADC at their core when used in an ultra low power applications and the important timing considerations associated with this type of ADC. There will

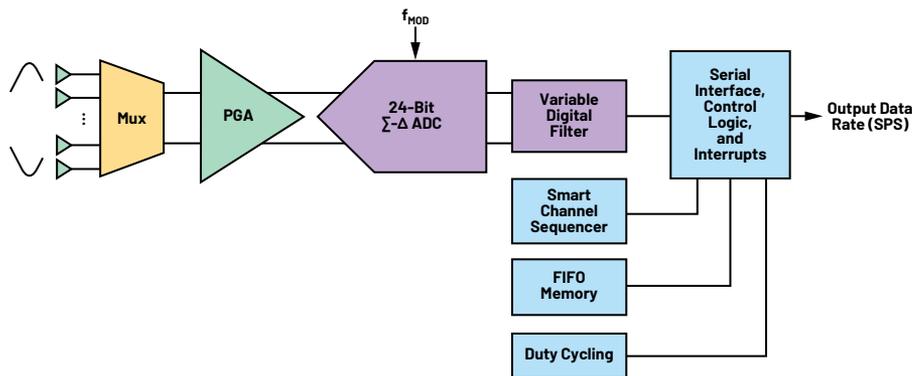


Figure 4. The AD4130 sigma-delta simplified system blocks.

be some overlap between SAR and sigma-delta signal chains that impact timing such as using techniques that look at minimizing the microcontroller interaction time to achieve system level power consumption improvements. These will be highlighted when we move onto the SAR ADC signal chains.

## Signal Chain Timing Considerations When Using Sigma-Delta ADCs

If the ADC of choice is a sigma-delta as opposed to a SAR, there will be a particular set of timing considerations that need to be taken into account. The principal areas to explore when looking at a signal chain are the analog front-end timing, ADC timing, and the digital interface timing shown in Figure 1.

### Analog Front-End Timing Considerations

We will focus on the three blocks independently starting with the analog front end (AFE). The AFE can vary depending on what type of design but there are some common aspects that can apply to most circuits.

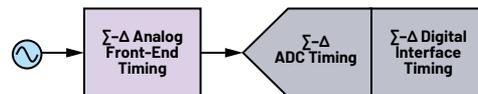


Figure 3. The AFE sigma-delta timing considerations.

The AD4130-8 is part of the precision low power group of signal chain products and is specifically designed with rich features set to reduce power while still achieving a high level of performance. Some of these features include an on-board FIFO, a smart channel sequencer, and duty cycling.

The AD4130-8 is Analog Devices' lowest power sigma-delta ADC. Considering it contains many key signal chain building blocks on chip such as an on-chip voltage reference, a programmable gain amplifier (PGA), a multiplexer as well as a sensor excitation current or sensor bias voltage, the ultralow current is impressive.

When we consider the AFE of this device, it consists of an on-chip PGA minimizing the analog input current and this removes the need for external amplifiers to drive the inputs. Oversampling followed by a digital filter ensures that the bandwidth is dominated by the digital filter. The AD4130-8 offers a number of on-chip sinc3 and sinc4 filters as well as filters designed to reject 50 Hz and 60 Hz noise. The sinc3 and sinc4 digital filters require supplementary external antialiasing filter. The purpose of this antialiasing filter is to limit the amount of bandwidth of the input signal. This is to ensure that noise, for example, with a rate of change at  $f_{\text{MOD}}$  (the modulator frequency) does not alias into the pass band and into the conversion result.

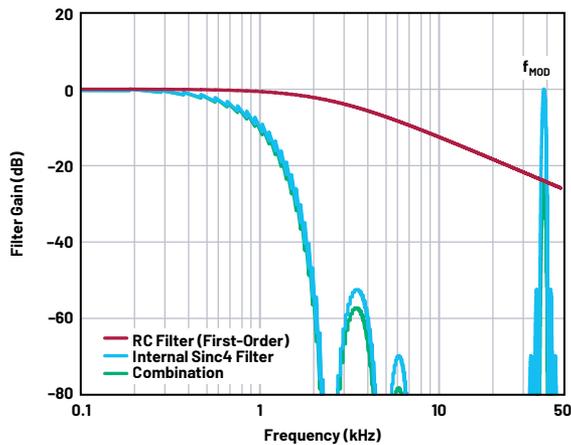


Figure 5. A simulation of combined external and internal filtering.

## Antialiasing Filter

Higher order antialiasing filters can be used but first-order, single-pole, low-pass filters are typically used to satisfy requirements. Filters are designed based on sampling the signal of interest with Equation 1 dictating the filter 3 dB BW:

$$f_{3\text{ dB}} = \frac{1}{2 \times \pi \times RC} \quad (1)$$

When selecting the capacitor values and resistance values, a higher resistance is more desirable but may increase noise while the lower capacitor values reach a limit after which the ratio of the pin capacitance to the external capacitance becomes relevant.

It is important to know the time it will take the circuit to charge based on the maximum voltage step that could be seen across this capacitor.

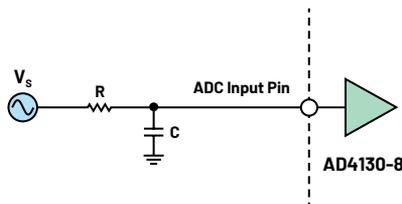


Figure 6. A first-order low-pass antialiasing filter.

The voltage seen at the capacitor will change with respect to time at rate of change of

$$V_C = V_S \left( 1 - e^{-\frac{t}{RC}} \right) \quad (2)$$

$V_C$  = Voltage across the capacitor at a point in time

$V_S$  = Supply voltage applied

$t$  = Time

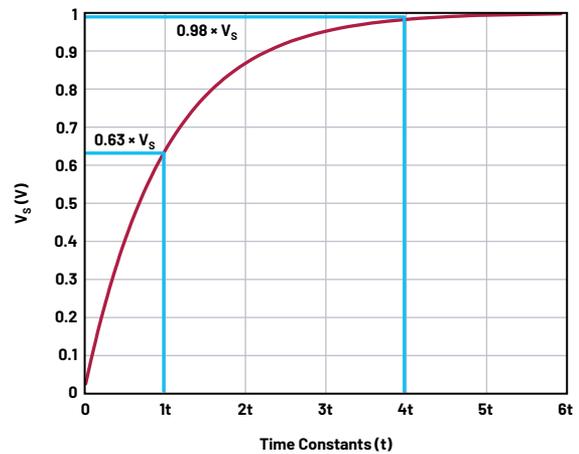


Figure 7. First-order low-pass filter settling time in response to a 1 V full-scale step change.

On power-up,  $V_S$ , the step size could be equal to the full input voltage range of the ADC ( $\pm V_{REF}/\text{gain}$ ).

Figure 7 shows that after 4-time constants ( $\tau = R \times C$ ) the signal has reached  $0.98 \times V_S$ . The number of time constants required can be calculated from the natural logarithm of the ratio of the step size,  $V_S$ .

$$N_T = \ln \left( \frac{V_S}{V_{\text{HALF\_LSB}}} \right) \quad (3)$$

$N_T$  is the number of time constants to wait for if the input is to settle to within half of an LSB ( $V_{\text{HALF\_LSB}}$ ) of the ADC's input voltage span. The  $V_{\text{HALF\_LSB}}$  in the previous formula can be substituted based on the voltage accuracy required. If the system designer wishes to resolve to within half an LSB, for a bipolar input ADC with  $N$  bits of resolution and with internal PGA gain = 1, this will be:

$$V_{\text{HALF\_LSB}} = \left( \frac{2 \times V_{\text{REF}}/\text{Gain}}{2^N + 1} \right) \quad (4)$$

The time that it takes to resolve to the real input voltage  $t_{ACQ}$  becomes the number of time constants multiplied by  $\tau$ , which is equal to  $RC$ :

$$t_{ACQ} = \tau \times N_T \quad (5)$$

Traditionally, when switching between channels on multiplexed ADCs, a large voltage swing (one channel at negative full scale, the next channel at positive full scale) between channels would require the similar calculation. The AD4130-8 solves this problem by implementing a low power on-chip precharge buffer that turns on when switching between channels. This ensures that at the fastest data rates, the first conversion after switching channels will be converted correctly. There is also an on-chip PGA designed to allow a full common-mode input range and this gives system designers a greater margin for widely varying common-mode voltages. This is useful for measuring signals, but in the worst case, one channel could be at negative full scale, while the next channel could be at positive full scale.

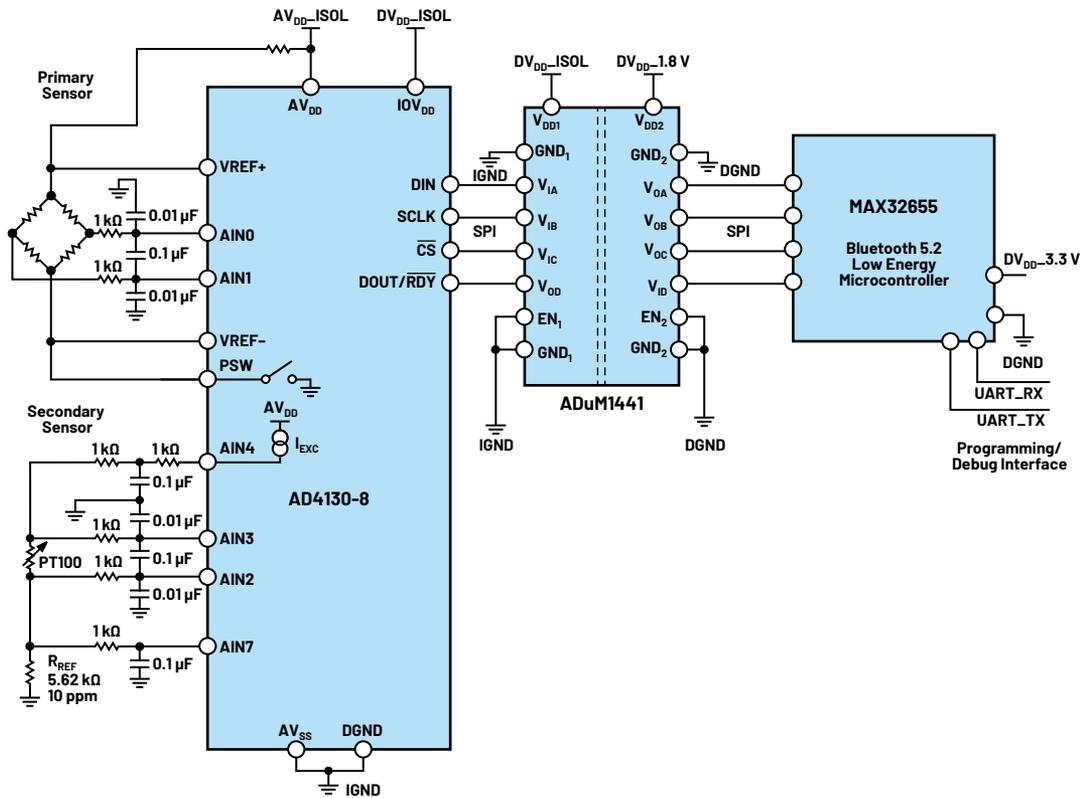


Figure 8. An isolated AD4130-8 circuit with a low-pass filter shown.

### Example: Analog Front-End Low-Pass Filter

The example in Figure 8 shows a Wheatstone bridge sensor with a -3 dB filtering for a 24-bit ADC just below 16 kHz.

$R = 1 \text{ k}\Omega$ ,  $C = 0.01 \text{ }\mu\text{F}$  with  $V_{REF} = 2.5 \text{ V}$  and the PGA gain set to 1:

The single-ended filters in Figure 8 show the primary sensor  $R = 1 \text{ k}\Omega$  and  $C = 0.01 \text{ }\mu\text{F}$ :

$$\tau = 10 \text{ }\mu\text{s} \quad (6)$$

The differential signal filter in Figure 8 shows the primary sensor  $R = 1 \text{ k}\Omega$  and  $C = 0.1 \text{ }\mu\text{F}$ . For more information on the formula, see [MT-070](#):

$$\tau = 50 \text{ }\mu\text{s} \quad (1 \text{ k}\Omega \times 0.1 \text{ }\mu\text{F}/2) \quad (7)$$

$$V_{HALF\_LSB} = 298 \text{ nV}$$

As the differential sensor time constant dominates the single-ended values, it will dictate the overall system calculation:

$$N_T = 16\tau \quad (\text{if } V_{STEP} = 5 \text{ V}) \quad (8)$$

$$t_{ACQ} = 0.8 \text{ ms}$$

This is the time a system designer would need to allow for the filter to settle externally before gathering a sample on power-up. This can be done in the digital domain by discarding samples or the sample instant can be delayed to account for this charging.

When designing a filter, the resistor and capacitor values may be different to what is shown earlier. System designers can model the filter together with the AD4130-8 using LTspice®. LTspice can also be used to model a system or signal chains as shown in Figure 9 where we are simulating an RTD behavior by varying R2.

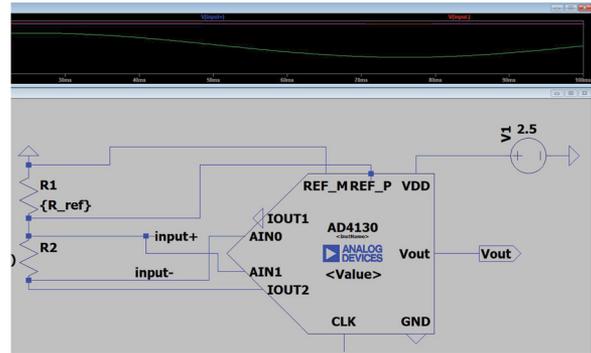


Figure 9. A simulation of an RTD (R2) circuit in LTspice.

### ADC Timing Considerations

Recalling that output data rates are how sigma-delta ADCs timing are referred to, let's examine the internal timing associated with this type of ADC.

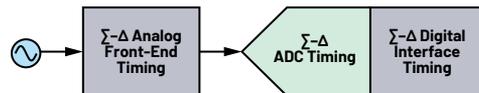


Figure 10. The sigma-delta ADC timing considerations.

This type of converter digitizes an analog signal with a low resolution (1 bit) ADC at a high sampling rate. By using oversampling techniques in conjunction with noise shaping and digital filtering, the effective resolution is increased.

An SPI write to a digital register allows users to control the oversampling and decimation rate of the AD4130-8. The modulator sample rate ( $f_{MOD}$ ) is fixed. The FS value essentially changes the number of samples (in increments of 16 for the AD4130-8) used by the digital filter to reach a result. Varying the FS word changes the number of oversampled modulations clocks per ADC result.

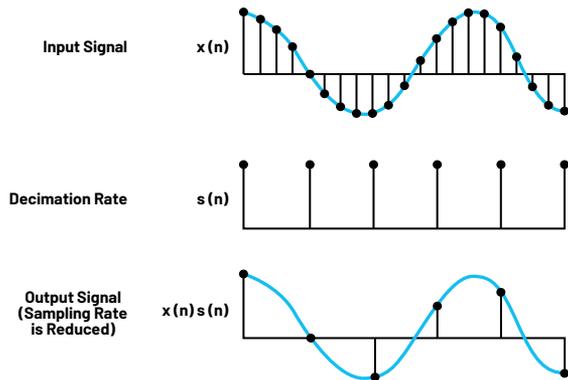


Figure 11. Decimation.

As decimation reduces the effective sampling rate at the ADC output, it achieves higher accuracy. Decimation can be viewed as the method by which the redundant signal information introduced by the oversampling process is removed. The more decimation used (the more samples that are included in the digital filter calculation), the more accuracy is achieved by the said digital filter but the slower the output data rate.

$$f_{ADC} = \frac{f_{MOD}}{16 \times FS} \quad (9)$$

where:

$f_{ADC}$  is the output data rate

$f_{MOD}$  is the master clock frequency

FS is the multiplier used to control the decimation ratio

## Filter Latency

When more than one channel is enabled, the link between the data sheet output data rate or ODR ( $f_{ADC}$ ) and the data throughput rate is more complex. This is due to the latency of the digital filter when switching channels. The time needed for the digital filters to settle depends on the sinc filter type. Figure 12 shows that the first conversion of sinc3 filter will take three conversion cycles until the digital equivalent to the analog input is reached. The first conversion of a sinc4 filter will take four conversion cycles. The  $t_{SETTLE}$  is the user programmable settle time that considers the mux switching. The higher the filter order, the lower the noise, but the downside is the number of conversion cycles needed for the filter to settle.

## Digital Interface Timing Considerations

To aid in the understanding of the digital interface timing in sigma-delta ADCs like the AD4130, a model is available via ADI software tool, ACE. The timing tools are part of several software tools integrated into the ACE software. There is a sequencer timing diagram and a FIFO timing diagram to aid in the understanding of these configurations.

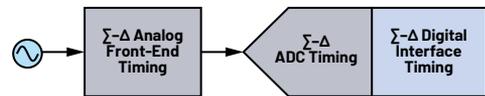


Figure 13. AFE sigma-delta digital interface timing considerations.

The AD4130-8 sequencer allows different input channels to have different digital filter and settling configurations and timing. The timing tool simplifies the process of calculating when data will be available to read.

When more than one channel is enabled, the user should not make the mistake of reading a settled channel ODR and dividing by the number of channels enabled to calculate the throughput rate because this does not consider digital filter latency. The filter latency should be taken into account when calculating the throughput rate (effective ODR vs. data sheet ODR). When more than one channel is enabled, the initial settling ( $t_{SETTLE}$ ) needs to be calculated, as well as the number of internal conversion cycles ( $t_{1st\_CONV\_IDEAL}$ ), as shown in Figure 14.

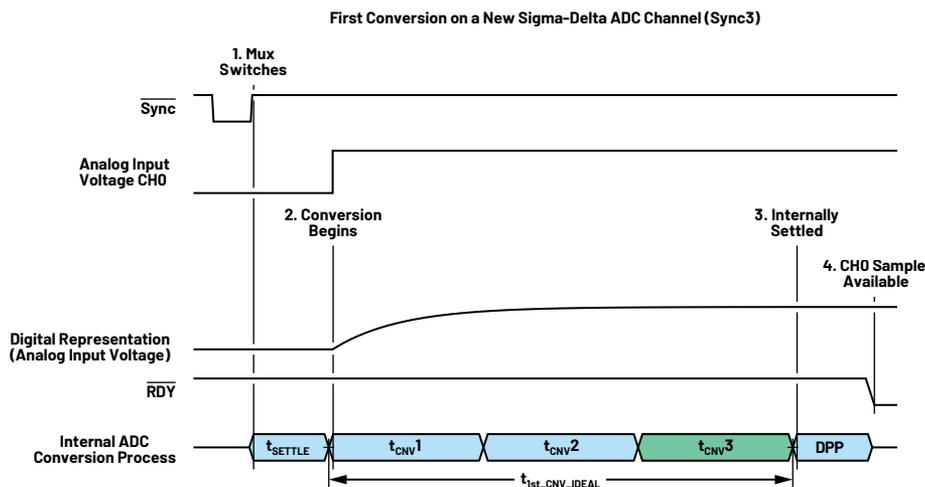


Figure 12. Filter latency.

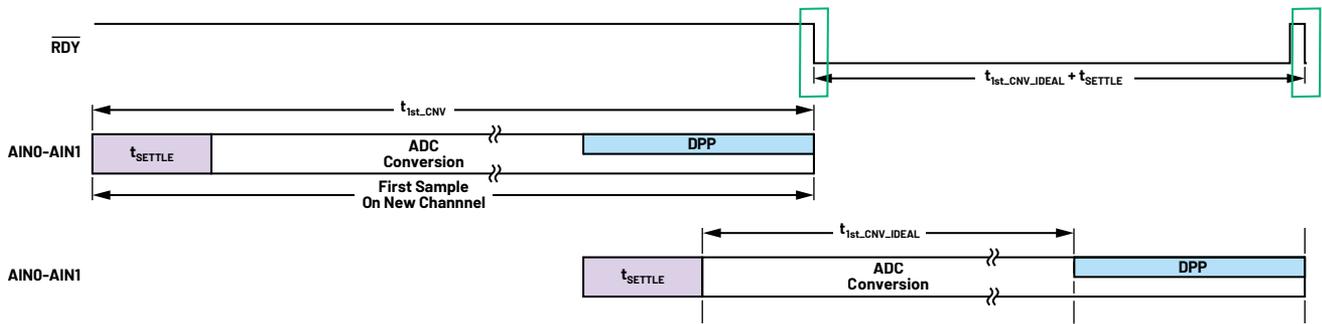


Figure 14. The first conversion output data rate including filter latency.

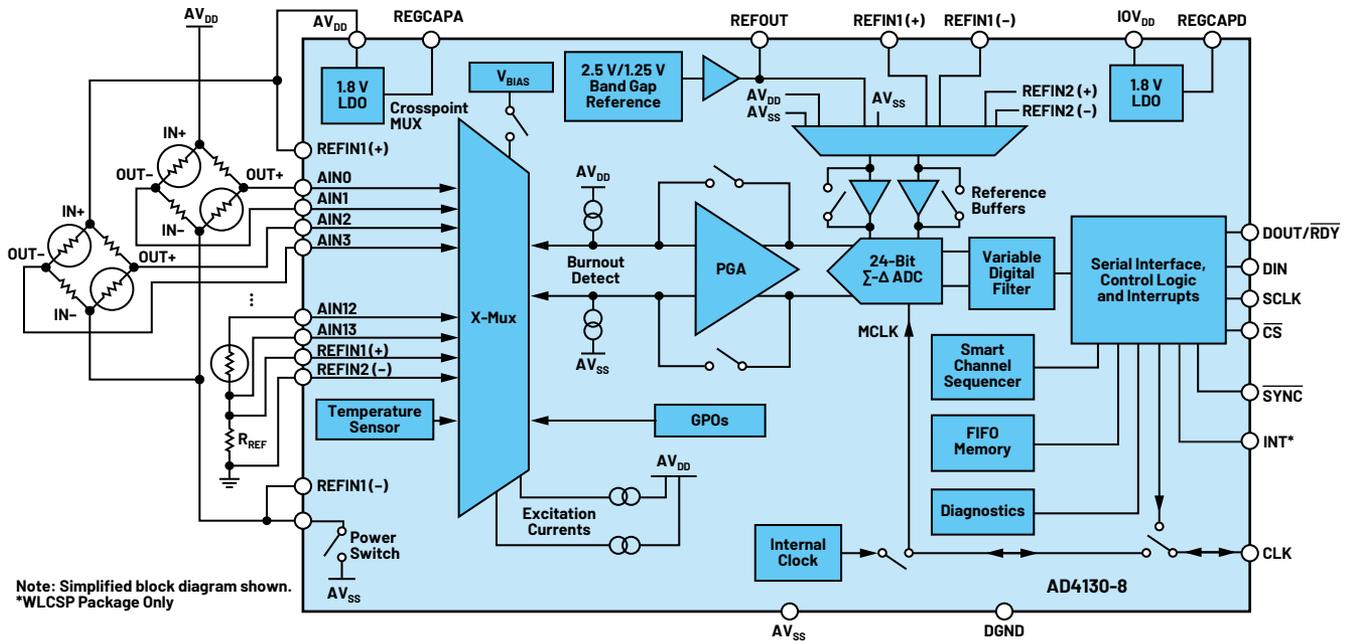


Figure 15. A simplified pressure sensor system block diagram.

If all channels have the same filter plus settling configuration and there are no repeat conversions on any channels, the throughput rate of a system becomes:

$$\text{Throughput Rate} = \frac{1}{(t_{1st\_CNV\_IDEAL} + t_{SETTLE})} \div CHs \quad (10)$$

(SPS)

where

CHs = is the number of channels enabled

$t_{1st\_CNV\_IDEAL}$  = is the conversion time including the filter latency

$t_{SETTLE}$  = a digitally controlled timing parameter that can be extended but with a minimum programmable time to account for the mux settling

The throughput rate can be calculated by looking at the sum of the  $1CNV\_ODR$  times, which is the time shown between the green squares in Figure 14.

$$t_{1CNV\_ODR} = t_{1st\_CNV\_IDEAL} + t_{SETTLE}$$

$$\text{Throughput Rate} = \frac{1}{(\sum t_{1CNV\_ODR})} \quad (11)$$

(SPS)

## Example: Pressure Sensor Signal Chain Timing

If we want to design a system with multiple pressure sensors, represented by the pressure sensors in Figure 15, accompanied by a temperature sensor:

**Question A:** How many pressure sensors per AD4130-8 can be deployed in the system?

**Question B:** What resolution can we expect if the voltage output range from the pressure sensor is 3 mV/V?

**Question C:** If a line in the plant needs at least 14 bits of effective resolution to meet the dynamic range system demands, how many load cells form the system?

### Part A

#### Step 1: Choose the gain

$$AV_{DD} = 1.8 \text{ V. } REF_{IN+} \text{ to } REF_{IN-} = 1.8 \text{ V}$$

The 1.8 V excitation of the load cell at 3 mV/V will lead to a 5.4 mV maximum output of each load cell.

The maximum gain on the PGA = 128.

The ADC input will see  $5.4 \text{ mV} \times 128 = 0.7 \text{ V}$  across its inputs, well within the 1.8 V range. A PGA gain of 128 is the correct gain to use.

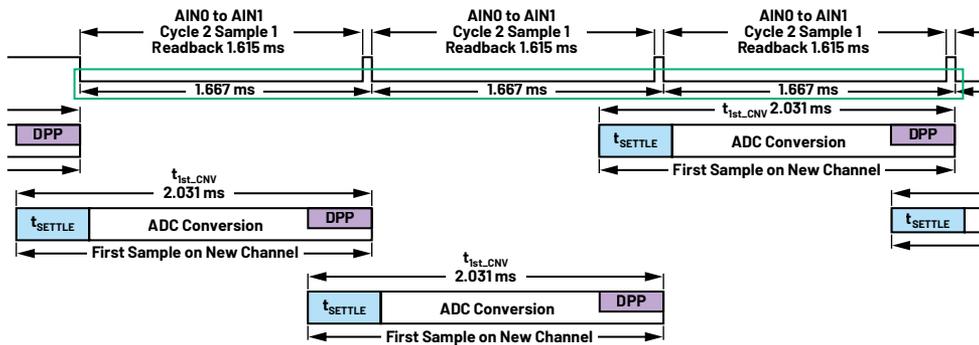


Figure 16. Calculating the sum of  $t_{1st.CNV\_ODR}$  using the timing tool.

Table 35. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
30	21.82	21.1 (18.3)	20.7 (18)	20.8 (18.1)	20.2 (17.4)	19.2 (16.5)	18.7 (16)	18 (15.3)	17.4 (14.7)
6	36.36	20.9 (18.1)	20.5 (17.8)	20 (17.3)	19.7 (17)	18.9 (16.2)	18.1 (15.4)	17.4 (14.7)	17.1 (14.4)
5	47.04	20.7 (18)	20.2 (17.5)	20.3 (17.5)	19.6 (16.8)	18.8 (16.1)	18.1 (15.4)	17.3 (14.5)	16.7 (13.9)
2	709.1	20 (17.3)	19.6 (16.8)	19.2 (16.5)	18.8 (16.1)	18 (15.3)	17.2 (14.5)	16.6 (13.8)	16.1 (13.4)
1	2187.16	18.8 (16.9)	18.6 (16.9)	18.3 (16.9)	17.9 (16.1)	17 (14.9)	16.2 (13.9)	15.7 (13.2)	15.3 (12.6)

Figure 17. FS word vs. gain.

### Step 2: Choose the FS value

We want to choose the fastest settings that are with a sinc3 filter and FS = 1.

### Step 3: Use the throughput rate for one channel to calculate the number of channels in the system

$$1CNV\_ODR = (1/1.667\text{ ms}) 600\text{ SPS}$$

$$\text{Throughput rate} = 600\text{ SPS}/N_{ch}$$

$1CNV\_ODR = \text{Throughput rate}$  for a single channel in a multichannel system with the same configurations and no repeat conversions

10 channels can be sampled at 60 SPS.

Answer A: Nine load cells per system

### Step 4: Use the data sheet effective resolution tables

Another point to consider is that when looking at noise and effective resolution tables, the calculations need to be based on the FS filter value and not the throughput rate. The ODR listed here is the settled channel ODR on a single channel.

System designers need to be careful when interpreting the data sheet. When more than one channel is enabled, the throughput rate in SPS decreases. There is a danger that readers might incorrectly interpret the resolution tables in the data sheet and think that a higher resolution is achievable. With settled channel ODR, the change in FS leads to an increase of oversampling and decimation that slows down the system in order to achieve higher accuracy. In the case when more than one channel is enabled, the decrease on the speed of reading from each ADC channel in SPS (throughput) is due to sampling on more than one channel. It is not caused by an increase in oversampling; hence, there is no increase in the resolution.

Table 29. Effective Resolution (Peak-to-Peak Resolution) vs. Gain Bits

FS (Dec.)	ODR (SPS)	Gain = 64	Gain = 128
2047	1.17	21.2 (18.5)	2 (17.3)
480	5	19.8 (17)	18.4 (15.7)
240	10	18.7 (16)	17.9 (15.2)
160	15	18.3 (15.6)	17.6 (14.9)
80	30	17.9 (15.2)	17.1 (14.4)
48	50	17.4 (14.7)	16.7 (14)
40	60	17.3 (14.6)	16.6 (13.9)
20	120	16.6 (13.9)	16 (13.3)
10	240	16.3 (13.5)	15.5 (12.7)
5	480	15.4 (12.7)	14.7 (12)
3	800	14.7 (12)	14 (11.3)
2	1200	13.9 (11.2)	13.2 (10.5)
1	2400	12.1 (9.41)	11.7 (8.94)

Figure 18. A resolution vs. gain data sheet table.

### Part B

If we look at the table in the data sheet, we see that the effective resolution is 11.7 bits for FS = 1 and gain = 128.

Answer B: 11.7 bits.

### Part C

To solve for C, we need to return to a couple steps from Part A:

### Step 2: Choose the FS value

This time, we choose the FS value based on the resolution requirement. In order to achieve an effective resolution of 14 bits, an FS of 3 should be chosen.

### Step 3: Use the throughput rate for one channel to calculate the number of channels in the system

We can use the timing AFM to achieve the resolution needed (1/4.167  $\mu\text{s}$ )

$$240\text{ SPS}/N_{ch} = \text{Throughput rate.}$$

We can use four channels at this data rate.

Answer C: Three channels.

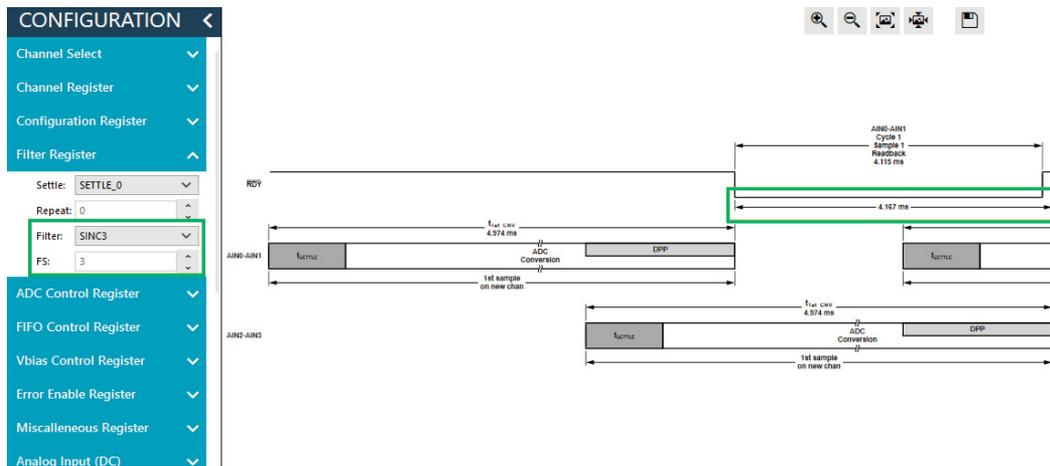


Figure 19. Using the timing tool to change the filter type and FS value and read the output data rate of the first conversion that includes filter latency.

## Duty Cycling

There are systems with lower throughput rates and higher output data rates such as health monitoring devices where the host controller would put the system in standby mode for the majority of the time and convert periodically. Duty cycling is available on the AD4130-8, and this allows the user to continuously convert with the part entering standby mode for 3/4 or 15/16 of the duty cycle while the part converts for 1/4 or 1/16 of the duty cycle. Active time and standby time are functions of the settings chosen by the user.

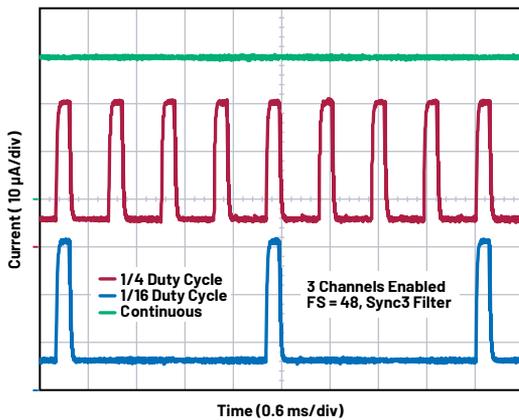


Figure 20. Duty cycling.

The AD4130-8 also incorporates a  $\overline{\text{SYNC}}$  pin that allows the user to deterministically control when conversions take place on a preselected number of channels. The part can also be configured to work in a reduced current standby mode, initiate a conversion sequence, leave the reduced current state, convert on a number of channels, and return to standby mode when the conversions have been completed.

## Example: Enabling Duty Cycling

Taking the same settings as the previous pressure sensor signal chain example and the throughput rate = 600 SPS/Nch, enabling two channels, the ODR becomes 300 SPS while the average current would be 28.7  $\mu\text{A}$  on average with a 3 V supply (see Figure 21).

After enabling duty cycling 1/16, the throughput rate becomes 24.489 SPS while the average current becomes 4.088  $\mu\text{A}$  over that period (40.834 ms; see Figure 22).

## FIFO

The AD4130-8 includes an on-board FIFO. A FIFO reduces system power by buffering the conversions and providing the opportunity for a microcontroller or host controller to enter a low power state while waiting for conversions. The biggest timing consideration here is to ensure the host reads back the FIFO quickly enough while continuously converting to avoid missed conversions.

The user can periodically read the FIFO when a specified number of samples (also known as watermark) has been gathered. When a desired number of samples is reached, an interrupt is available, and the host reads back the FIFO. The FIFO needs to be emptied to clear the interrupt. The user has a predefined period of time to read back data from the FIFO. The SCLK frequency used will determine how much data one can read without missing conversions.

The ACE software timing tool allows the user to vary the SCLK frequency or use a gated clock to inform the user when they need to reduce their watermark level while designing their system. For example, the FIFO readback.

Taking the example of a continuous single-channel measurement running at the maximum ODR of 2400 kSPS. If the watermark level is set to 256 and we attempt to read back, we have 729.2  $\mu\text{s}$  to read back the FIFO without missing a conversion. The user needs to read back 4112 bits. The tool informs the user that in order to read the FIFO back and not miss a conversion, then 5.64 MHz of a host SPI clock frequency is needed. This breaks the 5 MHz maximum specification for the part and an error appears allowing the user to modify their watermark to avoid breaking specification.

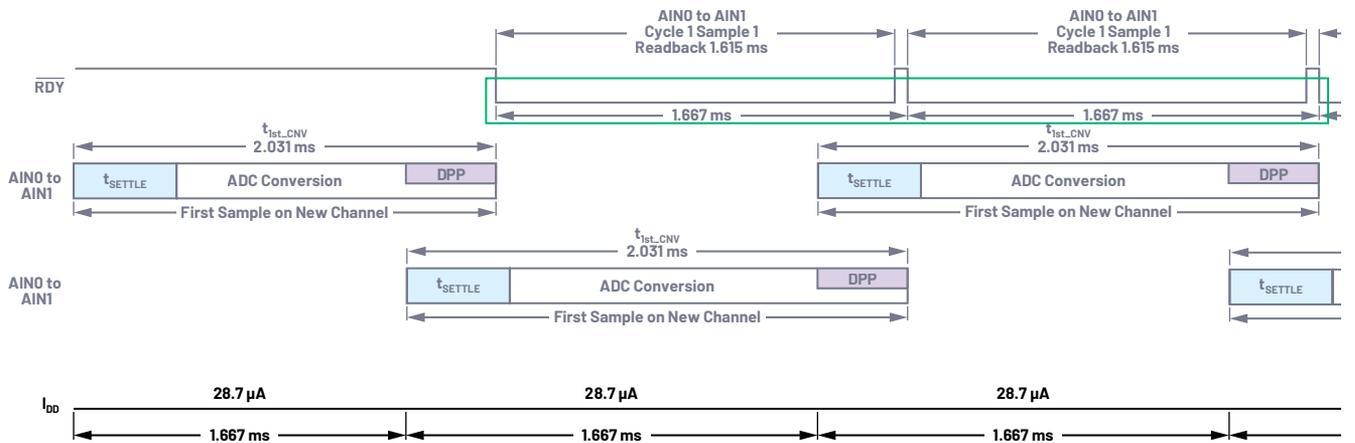


Figure 21. The throughput time and current before enabling duty cycling.

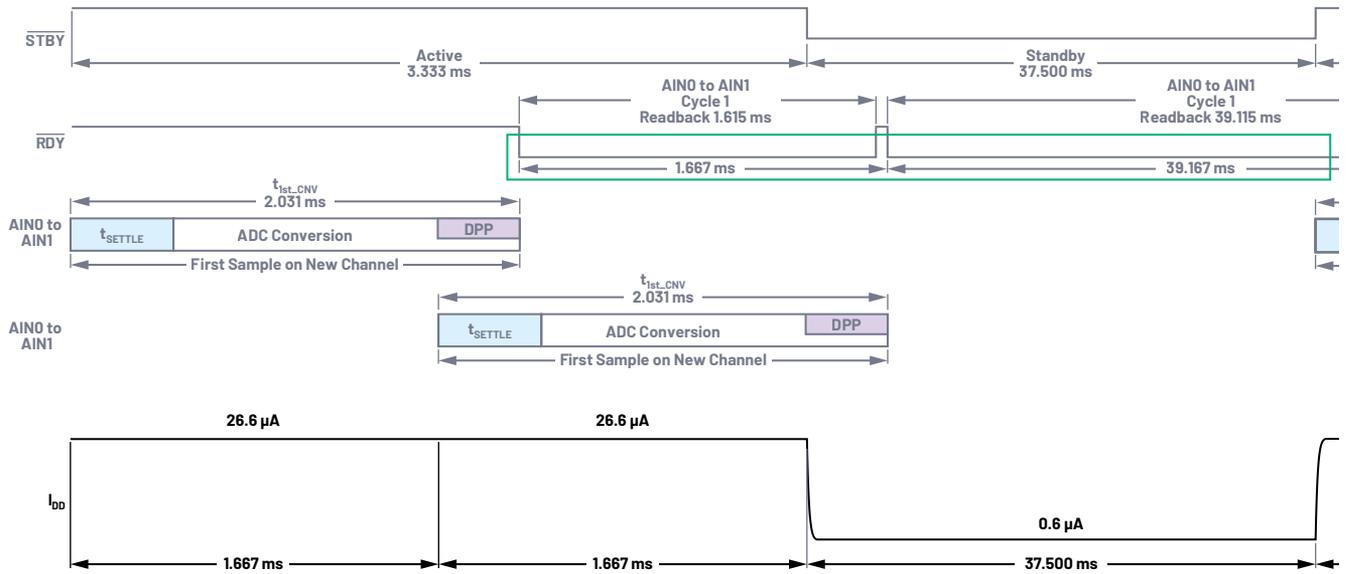


Figure 22. The throughput time and current after enabling duty cycling.

SCLK Freq. (min) 11.213 MHz  
 SCLK minimum frequency to readback FIFO samples, 11.213 MHz (ungated), exceeds specified SCLK frequency, 5 MHz. Reduce the watermark level to avoid missed conversions.

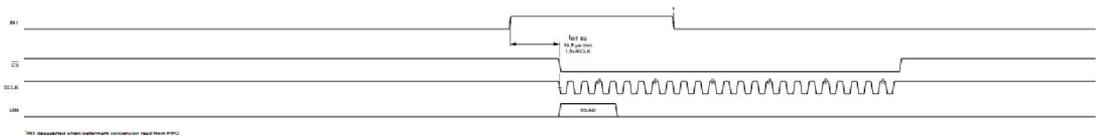


Figure 23. The AD4i30-8 ACE software FIFO readback window and alert.

**Table 3. Sigma-Delta Summary**

Topic	Timing Impact	Low Power Signal Chain Impact
Signal Chain Power-Up	Delays powering up each block	Applies to all signal chains
Antialias Filtering	Delays can exist that impact the conversion result(s)	AD4130-8 precharges filter when switching channels
Sinc Filter Latency	Throughput rates on multiplexed systems are impacted	Multiplexing allows for improved power savings ( $\mu\text{A}/\text{Ch}$ )
Duty Cycling	Throughput rates are reduced while duty cycling	Average current decreases proportionally
FIFO	Care needed to avoid missed conversions	Host controller can enter a low power state

When a sigma-delta ADC is used, we can see that there are plenty of trade-offs, timing factors, and features to consider. Part 2 of this article will examine the SAR ADC technology as well as the factors and features that impact timing in SAR ADC-based systems.



### About the Author

Padraic O'Reilly is an electronic test and measurement applications engineer who is focused on low power precision converter signal chains. Padraic enjoys architecting signal chains that combine technologies from multiple product lines. In the past, Padraic has held various measurement and applications roles. He has expertise in both RF microwave (PLLs, radar, radio transceivers) and precision mixed signal converter systems (DACs, ADCs, ASICs). Padraic holds a bachelor's degree in electronic engineering from the University of Limerick.

### References

- Maithil Pachchigar. "Design Trade-Offs of Using Precision SAR and Sigma-Delta Converters for Multiplexed Data Acquisition Systems." Analog Devices, Inc., April 2016.
- Walt Kester. "Which ADC Architecture Is Right for Your Application?" *Analog Dialogue*, Vo. 39, No. 9, June 2005.
- Albert O'Grady. "Transducer/Sensor Excitation and Measurement Techniques." *Analog Dialogue*, Vo. 34, No. 5, 2000.
- Alan Walsh. "Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter." *Analog Dialogue*, Vo. 46, No. 12, December 2012.
- Steven Xie. "Practical Filter Design Challenges and Considerations for Precision ADCs." *Analog Dialogue*, Vo. 50, No. 4, April 2016.
- Walt Kester. "MT-021: ADC Architectures II: Successive Approximation ADCs." Analog Devices, Inc., 2009.
- Ke Li and Colm Slattery. "Electromagnetic Flow Meters: Design Considerations." *Analog Dialogue*, Vo. 50, No. 6, June 2016.
- "SPICE Model for a Platinum RTD Sensor." Analog Devices, Inc., 2022.
- "MT-070 Tutorial: In-Amp Input RFI Protection." Analog Devices, Inc., 2009.