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Transceiver with Scalable Power and Performance: A Solution to Mission Critical Communications

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Abstract

This article discusses the ADRV9001, Analog Devices' newest generation software-defined radio (SDR) transceiver monolithic integrated circuit (IC) designed to provide scalable power and performance for many satellite, military, land mobile, utility infrastructure, and cellular mission critical communications. It first introduces three user-defined power saving options within the ADRV9001 from the component level, channel level, and IC system level. Then it further discusses a unique system feature called monitor mode, which not only saves power for the ADRV9001 itself but also enables the user to reduce the baseband integrated circuit (BBIC) operating power so that the best overall system power saving target can be achieved. This article also demonstrates power consumption savings for each power saving option and provides a detailed explanation of the associated performance trade-offs. By thoroughly understanding those trade-offs, the best system power saving strategy can be determined to achieve the optimal power consumption with satisfactory system performance.

Introduction

The ADRV9001 is part of a highly agile, user-configurable, new generation SDR IC transceiver family. It provides state-of-the-art RF performance with a set of advanced system features such as multichip synchronization (MCS), digital predistortion (DPD), dynamic profile switching (DPS), and fast frequency hopping (FFH). The IC supports both frequency division duplex (FDD) and time division duplex (TDD) operations with a wide range of RF frequency from 30 MHz to 6 GHz, which covers the ultrahigh frequency (UHF); very high frequency (VHF); industrial, scientific, and medical (ISM); and cellular frequency bands. It can handle both narrow-band (down to 12 kHz) and wideband (up to 40 MHz) signals with an almost continuous sample rate from 24 kSPS to 61.44 MSPS.

Empowered with all these capabilities, it is ideally suited as a platform for use across many different mission critical applications. Several general-purpose system on modules (SOMs) have already been developed from ADI partners, such as Alciom, Epiq Solutions, NextGen RF Design, and Vanteon Wireless Solutions. The SOM products target mission critical communications, including industrial automation and advanced metering applications. They share the same attributes of achieving a perfect balance between performance, power, size, and cost made possible by this IC. Figure 1 showcases the major power saving options provided at the component, channel, and system levels. Note: different transceiver variants in the ADRV9001 family could have different numbers of channels and different system features, which are simplified in Figure 1.

As shown in Figure 1, the component-level power saving options, highlighted in purple, mainly involve components such as the analog-to-digital converter (ADC), RF PLL, baseband (BB) PLL, analog transmit low-pass filter (Tx LPF), and receive low-pass filter (Rx LPF). Unlike most traditional transceivers, the ADRV9001 provides a pair of high performance (HP) and low power (LP) ADCs for both I and Q datapaths that users can select. For each component, multiple power saving options are provided. The channel-level power saving options are highlighted in red for a pair of transmit and receive channels. This is designed specifically for TDD applications, in which the transmit and receive operations are time multiplexing with each other. Therefore, while one channel is operating, the other channel is idle, which could be powered down. Different levels of channel power saving schemes are provided by requiring different wake-up times to resume operation. The system-level power saving options are highlighted in green; these can be employed to achieve more power savings for some applications expecting longer periods of inactivity, such as digital mobile radio (DMR) handset systems.[1]

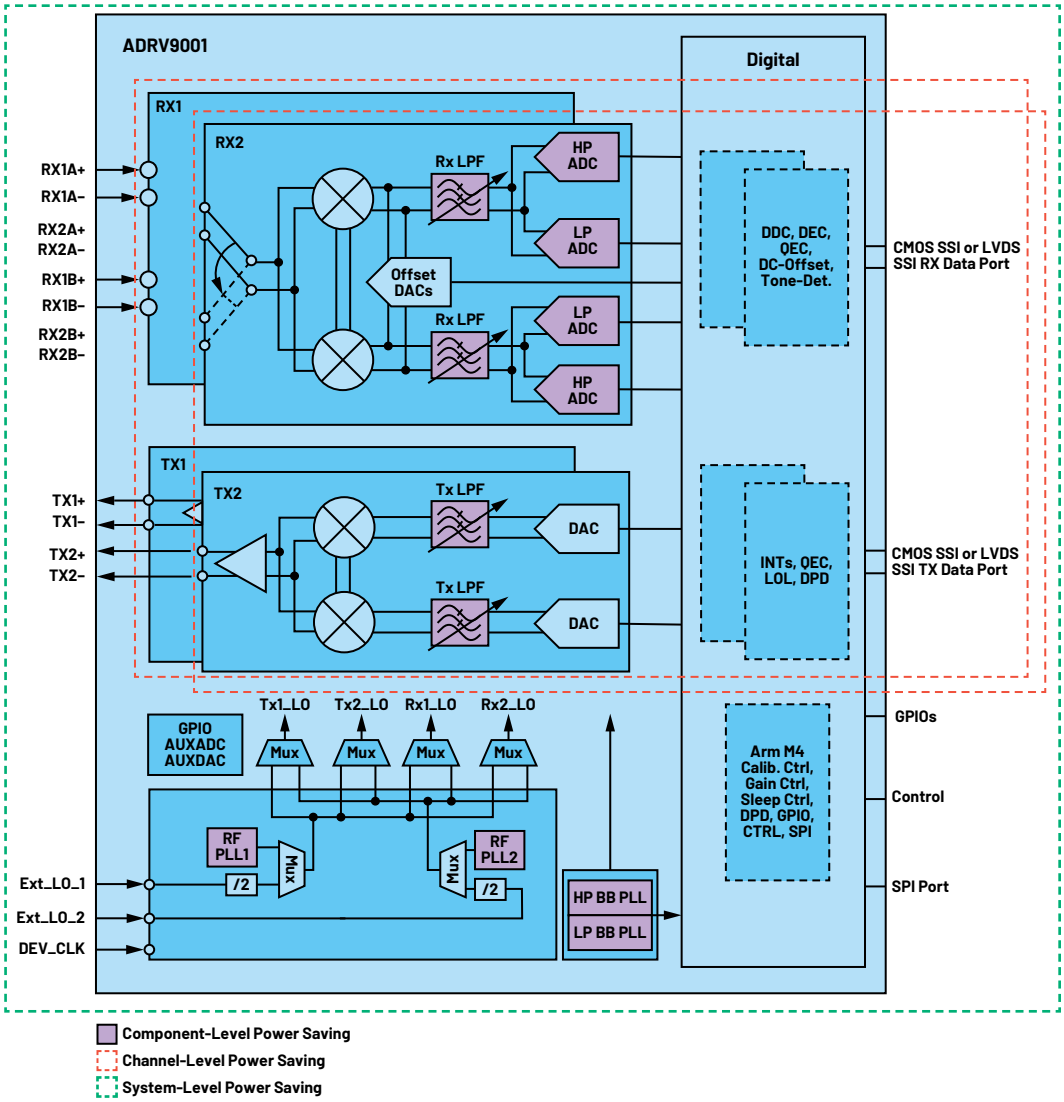

Figure 1. A high level diagram of the ADRV9001 power saving options at three different levels.

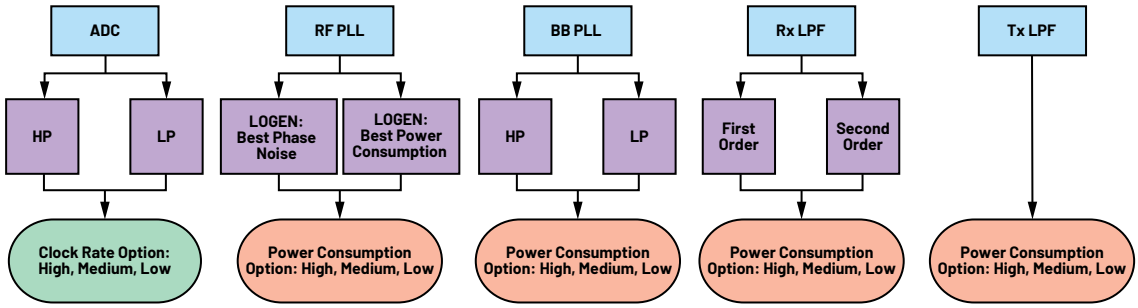

Figure 2. ADRV9001 component-level power saving options.

Besides all those power saving options, the transceiver features a monitor mode that allows both the ADRV9001 and the BBIC to go to sleep during the system idle time period. During sleep, the ADRV9001 can periodically wake up one receive channel to perform signal detection. Therefore, it could offload signal detection responsibility from the BBIC and allow it to sleep through the entire idle time period to achieve the best overall system power saving target.

In the following sections, all the power saving options and the monitor mode will be discussed in depth. By thoroughly understanding the associated performance trade-offs, a design engineer can explore all the potential power saving possibilities to keep the power consumption under control while guaranteeing a satisfactory system performance.

Component-Level Power Saving

Component-level power saving can be easily achieved by configuring individual hardware components through application programming interfaces (APIs) provided by the software development kit (SDK) during the device initialization stage. Figure 2 presents the major hardware components that offer multiple power saving options, including the ADC, RF PLL, BB PLL, receive LPF, and transmit LPF. To properly configure those components, it is crucial to understand the performance trade-offs.

The ADRV9001 provides an option to select between the HP ADC and the LP ADC. The HP ADC is based on continuous-time sigma-delta (CTSD) architecture and is 5 bits wide. The LP ADC is based on voltage-controlled oscillator (VCO) architecture and is 16 bits wide. The HP and LP ADCs provide a similar performance of dynamic range (full scale to thermal noise) but a different performance in linearity.[2] Figure 3 compares the input third-order intercept point (IIP3) and input second-order intercept point (IIP2) performance of the HP ADC and the LP ADC. It is measured with two continuous wave (CW) tones (with 1 MHz frequency spacing) using a wideband profile under room temperature and maximum receiver gain. Note: the x-axis stands for the baseband frequency for the first tone (lower frequency), and the second tone frequency is 1 MHz higher than the first tone.

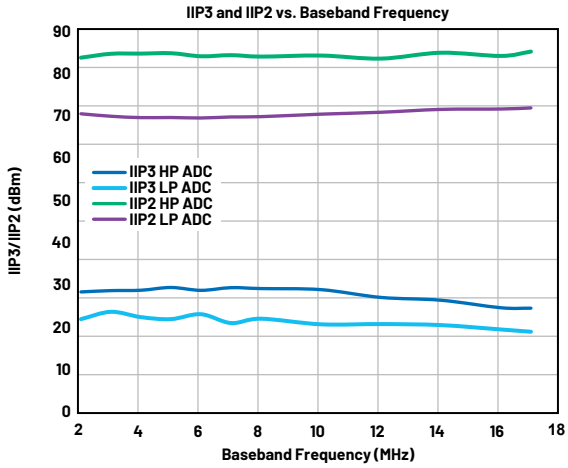

Figure 3. ADRV9001 linearity performance comparison between its HP ADC and its LP ADC.

As shown in Figure 3, both the HP ADC and the LP ADC demonstrate a high linearity performance. The HP ADC can achieve about 12 dB better performance with IIP2 and 6 dB better performance with IIP3 than the LP ADC by consuming more power. For both HP ADC and LP ADC, the user could further choose a high, medium, or low ADC sample rate. Choosing a higher sample rate improves the noise performance; in addition, it mitigates the requirement on transition band sharpness in the antialiasing filter design at the expense of consuming more power to process data at a faster rate.

The transceiver contains two RF PLLs, each driving its own local oscillator (LO) generator. Two options of LO generators are provided to achieve the best phase noise performance or the best power consumption performance. The best power consumption mode consumes less power by slightly sacrificing the phase noise performance. Note: the best phase noise performance option is only available for an LO frequency less than 1 GHz. For each mode, three different power consumption options are provided with different LO output swing levels. A higher swing level results in better phase noise performance but consumes more power.

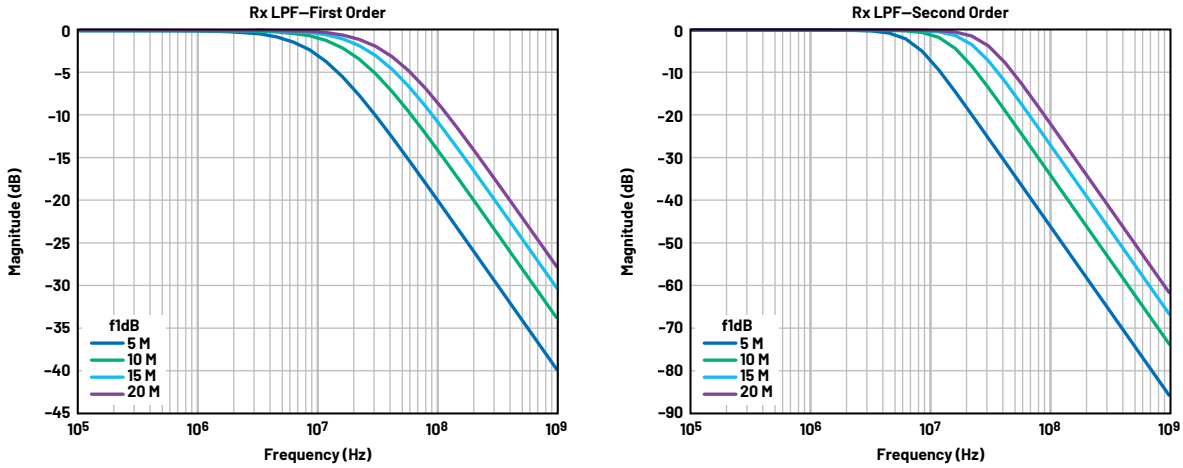

Figure 4. First-order and second-order Rx LPF frequency response at different LPF f1dB configurations.

The BB PLL generates all baseband and data port related clocks. Similar to the ADC, both HP BB PLL and LP BB PLL options are provided. The HP BB PLL has a programmable frequency range of 7.2 GHz to 8.8 GHz, while the LP BB PLL has a programmable range of 3.3 GHz to 5 GHz. The HP BB PLL offers greater flexibility in generating clocks to support a wider range of sample rates. When the signal sample rate is greater than 53.33 MHz, the HP CLK PLL must be used. The LP BB PLL has a limitation in supporting certain sample rates but consumes less power.

The receive LPF attenuates out-of-band signals by supporting a variable bandwidth from 5 MHz to 50 MHz. It also converts the baseband signal current to voltage. It could be configured in transimpedance amplifier (TIA) mode as a first-order single-pole filter, or in bi-quad (BIQ) mode as a second-order filter with two complex poles in the transfer function. While the in-band performance of both modes is similar, the second-order BIQ mode achieves additional out-of-band attenuation compared with the first-order TIA mode. Figure 4 compares the simulated frequency response at different f1dB configurations between these two filters. The selection of the second-order LPF consumes more power than the first-order mode. In addition to that, the in-band noise of the second-order LPF is around 2.5 dB higher than the first-order LPF. For both first-order and second-order modes, the user can further select three different power consumption levels at high, medium, or low by sacrificing the noise and linearity performance.

The transmit LPF is a second-order Butterworth filter used to attenuate the sampling images of the digital-to-analog converter (DAC). It also converts the current from the DAC to a voltage and reconstructs the analog spectrum by low-pass filtering the output. Similar to the receive LPF, it provides three options of power consumption levels at high, medium, or low at a cost of linearity performance.

Usually, the best performance could be achieved by configuring all the components at its highest power consumption option. For an FDD 1T1R LTE 20 MHz profile, by configuring the highest power consumption option when both transmit and receive channels are active, the total power consumption of the ADRV9001 is measured at about 1800 mW. Note: even with the same configurations, measurement results might vary depending on hardware and temperature. Table 1 presents the amount of power saving achieved through configuring different power saving options. In this 1T1R LTE 20 MHz profile, both Receive Channel 1 and Transmit Channel 1 are enabled and the LO is configured at 900 MHz. Note: the numbers in each row of Table 1 show the relative amount of power saving in mW by only enabling this single power saving option. For example, using HP ADC with Medium Clock Rate saves about 72 mW compared against the highest power consumption around 1800 mW with all the highest power consumption options enabled.

Table 1. ADRV9001 Component-Level Power Saving Measurement

ADC		Power Saving (mW)
HP	Medium Clock Rate	–72
	Low Clock Rate	–41
LP	High Clock Rate	–100
	Medium Clock Rate	–177
	Low Clock Rate	–158
RF PLL		
Best Phase Noise	Medium Power Consumption	–44
	Low Power Consumption	–84
Best Power Consumption	High Power Consumption	–50
	Medium Power Consumption	–80
	Low Power Consumption	–108
BB PLL		
HP	Medium Power Consumption	–5
	Low Power Consumption	–10
LP	High Power Consumption	–45
	Medium Power Consumption	–47
	Low Power Consumption	–49
Rx LPF		
Second Order	Medium Power Consumption	–26
	Low Power Consumption	–40
First Order	High Power Consumption	–77
	Medium Power Consumption	–101
	Low Power Consumption	–116
Tx LPF		
Medium Power Consumption		–29
Low Power Consumption		–47

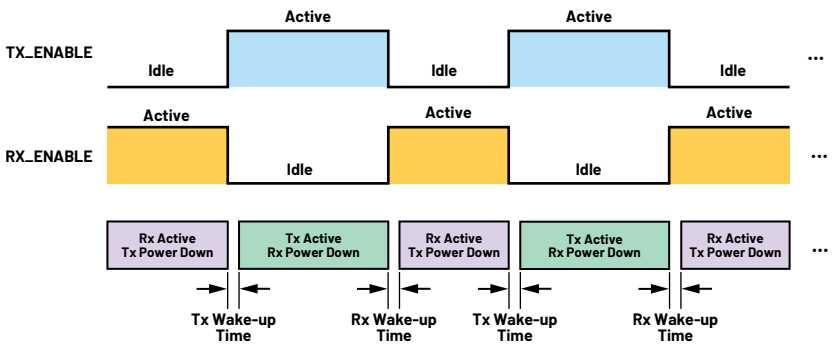

Figure 5. Channel-level power saving in a general TDD operation.

Based on Table 1, if an application has a relaxed performance requirement, by selecting the lowest power consumption option for each component, a total power saving of about 480 mW could possibly be achieved with this profile. Note: the component-level power saving options are mainly static, which means once configured during the device initialization stage, they could not be changed dynamically on-the-fly. One exception is the selection between the HP ADC or the LP ADC, which allows changing on-the-fly through an API command.

Another static power saving option worth mentioning is related to the configuration of one of its power domains. The ADRV9001 requires five different power supply domains: 1 V digital (VDD_1P0), 1.8 V digital (VDD_1P8), 1 V analog (VDDA_1P0), 1.3 V analog (VDDA_1P3), and 1.8 V analog (VDDA_1P8). Among them, the VDDA_1P0, which is used to power all the transmit and receive channel LO circuits, is optional. This domain can be powered using internal low dropout (LDO) regulators, which generate the 1 V required. Alternatively, it can be powered externally by bypassing some of the ADRV9001 internal LDO regulators, which is desirable to achieve more power saving by turning off the LDO regulators and applying a higher efficiency external power source.[3] Note: all the measurements performed in this article use internal LDO regulators to power up the VDDA_1P0 power domain.

Channel-Level Power Saving

Different from the static component-level power saving, channel-level power saving is dynamic. It is designed for TDD operations specifically. As shown in Figure 5, in TDD, transmit and receive operations are time multiplexing with each other. While one channel is active, the other channel is idle; therefore, it could be powered down to reduce power consumption. Different from component-level power saving, it does not result in any performance penalty by powering down the idle channel, but it takes more time to wake up to resume the normal operation.

One method to power up and down channels is to use the channel enable signal (TX_ENBALE/RX_ENABLE) rising and falling edge, respectively. As shown in Figure 5, the channel being powered down starts to wake up at the corresponding enable signal rising edge and it takes some time to become fully operational. If more channel components are powered down, then more wake-up time is required. The user should evaluate if the required wake-up time can satisfy the transmit and receive channel transition timing requirement in their TDD applications.

Three different modes of channel-level power saving are provided: Mode 0, Mode 1, and Mode 2. Each higher mode powers down additional channel-associated components by requiring a longer wake-up time. Table 2 summarizes these three modes along with the required approximate wake-up time at different RF PLL calibration modes and RF PLL reference clock rates.

Table 2. Channel-Level Power Saving Modes and the Required Wake-Up Time

Channel Components Powered Down		Mode 0	Mode 1	Mode 2
Transmit	Analog and Digital Data Path	X	X	X
	Tx Internal PLLs		X	X
	Tx PLL LDOs and Channel LDOs			X
Receive	Analog and Digital Data Path	X	X	X
	Rx Internal PLLs		X	X
	Rx PLL LDOs and Channel LDOs			X
Wake-Up Time at Different Configurations		**Mode 0**	**Mode 1**	**Mode 2**
Approximate Power-Up Time (µs) with RF PLL Normal Calibration Mode and Different RF PLL REF CLK Rates	RF PLL REF CLK = 30 MHz	4.5	350	500
	RF PLL REF CLK = 50 MHz		180	380
	RF PLL REF CLK = 100 MHz		170	370
Approximate Power-Up Time (µs) with RF PLL Fast Calibration Mode and Different RF PLL REF CLK Rates	RF PLL REF CLK = 30 MHz		100	300
	RF PLL REF CLK = 50 MHz		60	260
	RF PLL REF CLK = 100 MHz		40	240

As shown in Table 2, a higher channel-level power saving mode powers down additional channel components at the expense of longer wake-up time. By default, the channel power saving Mode 0 is always enabled if the user does not configure other modes. It powers down analog and digital datapath components such as mixers, converters, filters, etc. when the channel is idle. In Mode 0, only the RX_ENABLE and TX_ENABLE signals can be employed to trigger the power-up and

power-down. The wake-up time is short—around 4.5 µs. The channel power saving Mode 1 further powers down the channel's internal PLL. When the PLL is powering up, recalibration is mandatory, so the PLL wake-up time includes PLL power-up time and PLL calibration time. The ADRV9001 provides two PLL calibration modes: normal mode and fast mode. The fast mode does not guarantee a lock over the entire temperature range as the normal mode does, but it is more suitable when the channel stays at a particular frequency for a short period of time. As shown in Table 2, fast mode takes less calibration time than the normal mode; therefore, the PLL can wake up more quickly. In addition, a higher RF PLL reference clock rate also reduces the PLL calibration time. The channel-level power saving Mode 2 further powers down PLL LDO regulators and channel LDO regulators. It adds a fixed amount of wake-up time to turn on the LDO regulators. Note: the measurement of wake-up time displayed in Table 2 is performed at the ADRV9001 standard system clock rate of 184.32 MHz. When a custom profile with arbitrary sample rate is used, the system clock rate could change, which scales the PLL power-up time accordingly (lower system clock rate will increase the required PLL power-up time). The user could retrieve the system clock information from the ADRV9001 transceiver evaluation software (TES).

Modes 1 and 2 can be triggered by the RX_ENABLE and TX_ENABLE signal rising edge the same as Mode 0. In the case that a pair of transmit and receive channels shares the same internal PLL and its LDO regulators, the power saving achieved by modes 1 and 2 is limited when one channel is active, since the PLL and its LDO regulators must be powered up. Higher power saving can be achieved when both channels are idle. Different from Mode 0, Mode 1 and Mode 2 can also be triggered by a pre-assigned digital general-purpose input/output (DGPIO) pin. However, one DGPIO pin powers up and down both channels. Therefore, the DGPIO pin method can only be used when both transmit and receive channels are idle.

Figure 6 shows an example of using a DGPIO pin to trigger power saving Mode 1 or Mode 2. In this example, the entire TDD time period is divided into multiple time frames and each of them consists of four time slots. The first one is a transmit time slot, followed by two idle time slots, and the last one is a receive time slot. By default, Mode 0 is always enabled, which powers down the idle channel. However, during the idle time slots 2 and 3, both transmit and receive channels are idle; therefore, the DGPIO pin method could be used to trigger power saving Mode 1 or Mode 2, which achieves additional power saving than Mode 0 only.

It is important to emphasize that the DGPIO pin method should always trigger higher channel-level power saving modes than RX_ENABLE and TX_ENABLE signals as in the example shown in Figure 6. The DGPIO pin method helps to achieve more power saving in the scenario when Mode 1 and Mode 2 could not be triggered by RX_ENABLE and TX_ENABLE signals due to insufficient transmit and receive channel transition time.

In some TDD applications, one channel might be initialized but not used for a long period of time. In that case, an API command to power down the unused channel similar to Mode 2 (powering down its datapath, PLL, and LDO regulators) is provided for the user. This moves the unused channel to the hibernate state. Before the channel starts to operate, the user could power it up by using another API command. This ensures the best channel-level power saving for the unused channel is achieved. More discussions about channel/system states will be presented in later sections.

To demonstrate the power saving achieved through three different channel-level power saving modes, a DMR profile with 24 kSPS is employed. In DMR handset systems, the battery life is one of the key factors to decide the user experience. After powering up, the DMR handset is switched among three different states: transmit, receive, and idle. A typical cycle case is denoted as 5-5-90, which means the handset spends approximately 5% of the time on transmit, 5% of the time on receive, and 90% of the time on idle. Usually, the battery life data with the 5-5-90 cycle case needs to be published in the DMR handset data sheet as an important system parameter.[1]

Since power consumption is critical for DMR applications, the best power saving options are adopted at the component level. In addition, for a pair of transmit and receive channels, only one PLL is employed. Since the ADRV9001 receiver uses intermediate frequency (IF) mode and the transmitter uses zero-IF mode, the PLL is retuned when one channel is switching to the other channel. Figure 7

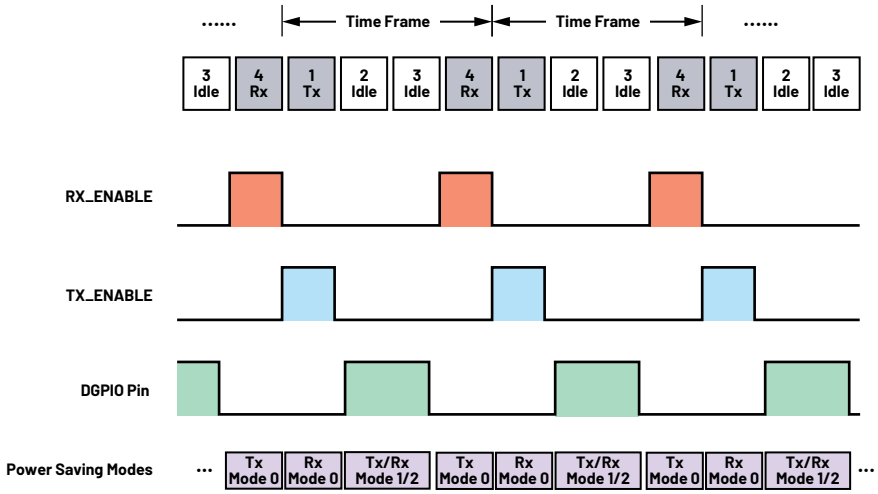

Figure 6. An example of using DGPIO to trigger channel-level power saving using Mode 1 or Mode 2.

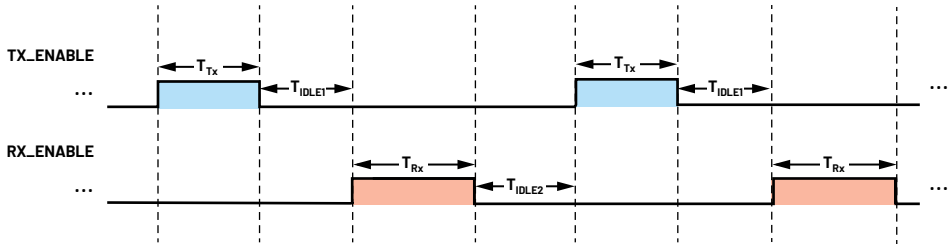

Figure 7. A general DMR TDD timing configuration for power consumption measurement using channel-level power saving modes.

describes a general TDD timing configuration. T_{TX} and T_{RX} stand for the transmit and receive active time, respectively. T_{IDLE1} and T_{IDLE2} stand for the idle time. For simplicity, wake-up time is not indicated since in general it is much shorter compared with the channel active and idle time; therefore, it is insignificant in power consumption calculation.

Table 3 presents the power consumption measured during T_{TX}, T_{RX}, and idle time (T_{IDLE1} /T_{IDLE2}) with the channel-level power saving modes 0, 1, and 2. In this measurement, the LO is configured at 900 MHz.

Table 3. Power Consumption During Different Time Periods for a TDD DMR Profile Using Channel-Level Power Saving Modes 0, 1, and 2

Channel-Level Power Saving Mode	Power Consumption (mW)		
	P_{TX} (Transmit Only)	P_{RX} (Receive Only)	P_{IDLE} (Idle)
Mode 0	580	525	368
Mode 1	580	509	205
Mode 2	580	502	173

By knowing the power consumption during different time periods, the average power consumption could be further calculated as:

$$P_{AVG} = P_{TX} \times \left(\frac{T_{TX}}{T_{TOTAL}}\right) + P_{RX} \times \left(\frac{T_{RX}}{T_{TOTAL}}\right) + P_{IDLE} \times \left(\frac{T_{IDLE1} + T_{IDLE2}}{T_{TOTAL}}\right) \quad (1)$$

$$T_{TOTAL} = T_{TX} + T_{RX} + T_{IDLE1} + T_{IDLE2}$$

Considering the typical 5-5-90 DMR use case, the average power consumption by using Mode 2 can be calculated as 580 × 5% + 502 × 5% + 173 × 90%, which is about 210 mW.

As shown in Table 3, Mode 1 and Mode 2 save more power during the idle time period since the PLL and its related LDO regulators can be powered down. But during the channel active time (either transmit or receive), the PLL and its LDO regulator can't be powered down since they are shared between both channels; therefore, the power saving is very limited by only powering down idle channel related components such as the channel LDO regulators.

System-Level Power Saving

As discussed in the previous section, channel-level power saving modes power down channel-associated components such as the datapath, RF PLL, and LDO regulators. In the case both transmit and receive channels are idle, such as in the scenario described in Figure 6, the system-level components could be further powered down to achieve additional power saving. Those system-level components include clock PLL, converter LDO regulators, clock PLL LDO regulators, and the Arm® processor and its memories. Similar to the channel-level power saving modes, three system-level power saving modes are provided, with the higher number modes powering down additional system components, which are summarized in Table 4.

Table 4. System-Level Power Saving Modes and the Required Wake-Up Times

Channel and System Components Powered Down		Mode 3	Mode 4	Mode 5
Tx	Analog and Digital Data Path	X	X	X
	Tx Internal PLLs	X	X	X
	PLL LDOs and Tx LDOs		X	X
Rx	Analog and Digital Data Path	X	X	X
	Rx Internal PLLs	X	X	X
	PLL LDOs and Rx LDOs		X	X
System	CLK PLL	X	X	X
	Converter LDOs and CLK PLL LDOs		X	X
	Arm + Memories			X
Wake-Up Time at Different Configurations		**Mode 3**	**Mode 4**	**Mode 5**
Approximate Power-Up Time (µs)		250	650	3200

As shown in Table 4, Mode 3 powers down the CLK PLL in addition to Mode 1, Mode 4 powers down the CLK PLL, converter LDO regulators and CLK PLL LDO regulators in addition to Mode 2. Mode 5 further powers down the Arm device and its memories in addition to Mode 4. Similarly, powering down more components causes longer wake-up time. In Mode 5, it takes approximately 3.2 ms to power up all the components.

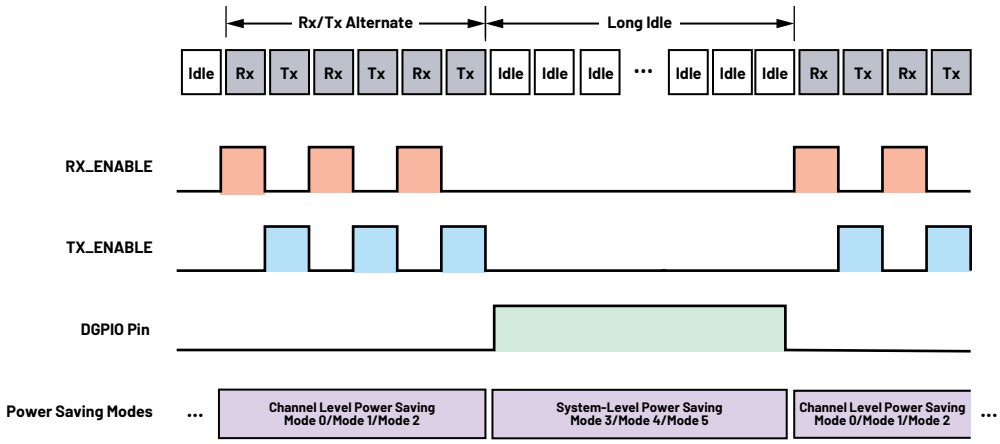

Figure 8. An example of using combined channel-level and system-level power saving.

Different from the channel-level power saving, the system-level power saving must be triggered by a DGPIO pin. Figure 8 shows an example of how to use a combined channel-level power saving and system-level power saving during different time periods of a TDD operation to achieve better power saving.

In this example, during the time period transmit and receive operations are alternate, users can select the highest possible channel power saving mode by using RX_ENABLE and TX_ENABLE signals. During the long idle time period when no channel is operating, the user can employ a DGPIO pin to trigger the highest system-level power saving mode, which allows to power down additional system components. This helps to achieve the better power saving compared with the channel-level power saving only. Similar to the DGPIO pin method in the channel-level power saving Mode 1 and Mode 2, the DPGIO pin method in the system-level power saving can only be employed when both TX_ENABLE and RX_ENABLE signals are low.

Table 5 presents the power consumption for the DMR use case shown in Figure 7 by using power saving Mode 2 when one channel is active, and three different system-level power saving modes when both channels are idle.

Table 5. Power Consumption During Different Time Periods of a TDD DMR Profile Using Channel-Level Power Saving Mode 2 and System-Level Power Saving Modes 3, 4, and 5

System-Level Power Saving Mode (For Idle Only)	Power Consumption (mW)		
	P_{TX} (Transmit Only, Mode 2)	P_{RX} (Receive Only, Mode 2)	P_{IDLE} (Idle)
Mode 3	580	502	100
Mode 4	580	502	65
Mode 5	580	502	35

Compared with Table 3, during the idle time period, it is clear that using the System-Level power saving modes can save more power. For the same 5-5-90 DMR use case, the average power consumption using Mode 5 is further lowered, which can be calculated as 580 × 5% + 502 × 5% + 35 × 90% = 86 mW.

Monitor Mode

In the previous sections, three different levels of power saving options were discussed. To achieve the best power saving in a system, reducing the power consumption for only the ADRV9001 might not be sufficient. Ideally, during the long idle time period, the best power saving of the entire system is achieved when all the major components can be powered down. To achieve this goal, a monitor mode is provided that allows both the ADRV9001 and the BBIC to go into deep sleep during the entire idle time period—except for one receive channel, which could optionally wake up to perform signal detection periodically. When a valid signal is found, the ADRV9001 wakes up the BBIC immediately. This offloads the signal detection responsibility from the BBIC and allows it (and possibly other circuitry in the system controlled by the BBIC) to sleep during the entire idle time period to achieve the highest overall system power saving.

Figure 9 shows a simplified state diagram of the ADRV9001 and how it transitions between normal operation mode and monitor mode.

As shown in Figure 9, with normal operation mode, after the ADRV9001 is powered up, it automatically goes to the standby state, during which the user can configure component-level power saving options. The standby state will switch to the calibrated state if the initialization is successful. As mentioned earlier, in this state, unused channels (although initialized) can be powered down using an API command to move from the calibrate ready substate to hibernate substate. From the calibrated state, the radio on command further primes the channels to prepare for transmit and receive operations and all channels are switched to the primed ready substate. Note: this substate is equivalent to the default

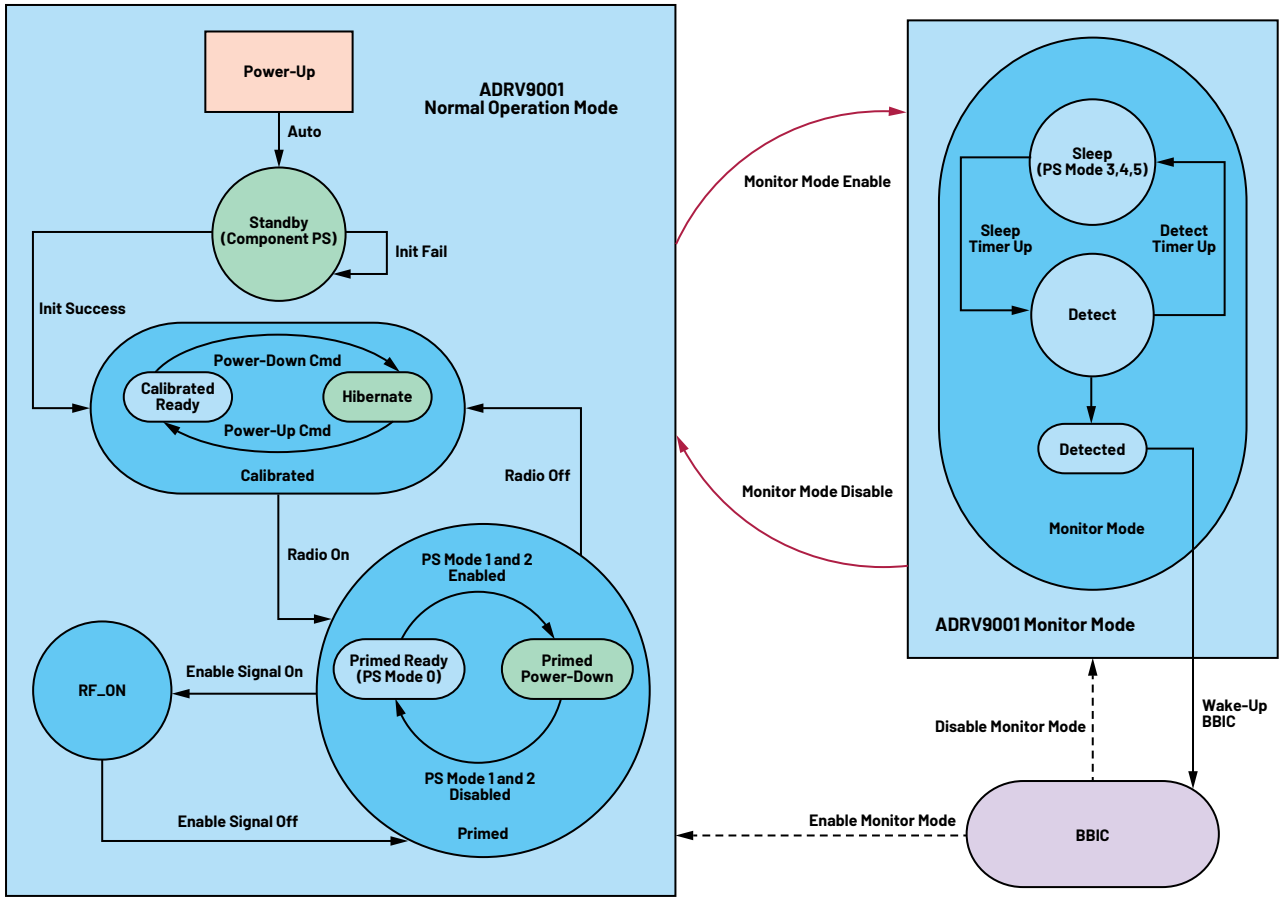

Figure 9. State diagram of the ADRV9001 in normal operation mode and monitor mode.

channel-level power saving Mode 0. When channel enable signal is on, channels are further moved to RF_ON state to start operation. As discussed earlier, during a TDD operation, idle channels can be powered down using channel-level power saving modes. If using power saving Mode 0, it moves the idle channel from RF_ON state to the primed ready substate. If using power saving Mode 1 or Mode 2, it moves the idle channel from RF_ON to primed power-down substate.

The transition from normal operation mode to monitor mode is initiated by the BBIC after it detects the start of a long idle time period. In monitor mode, the BBIC employs system-level power saving Mode 3, Mode 4, or Mode 5 based on the configuration set by the BBIC. Both the ADRV9001 and BBIC go to sleep—except one ADRV9001 receive channel could optionally wake up to perform signal detection periodically. When a valid signal is found, the ADRV9001 will wake up the BBIC and the BBIC will further disable monitor mode to resume normal operation.

As shown in Figure 9, monitor mode consists of three different states: sleep, detect, and detected. The sleep and detect cycles are controlled through timers. When the time is up, one state will transition to another state if no valid signal is detected. The BBIC determines the timer and which state monitor mode should start with. If a valid signal is detected during the detect state, the ADRV9001 will transition to detected state immediately and wake up the BBIC. The BBIC then disables monitor mode, and the ADRV9001 switches back to normal operation mode. The start of monitor mode is triggered by a DGPIO pin as in the system-level power saving mode, since fundamentally these two are very similar except that monitor mode incorporates a signal detection capability. As a matter of fact, the ADRV9001 can dynamically switch between system-level power saving mode and monitor mode through an API command.

Figure 10 describes the detailed timing events happening during monitor mode for both the ADRV9001 and the BBIC. When the monitor mode DGPIO pin is asserted by the BBIC, the BBIC will start sleep and the ADRV9001 will wait for a configurable initial delay before going to sleep-detect pattern by using the configured timers. The ADRV9001 can perform signal detection during the initial delay to make sure that no signal is present before going to sleep. The sleep-detect pattern of the ADRV9001 continues to go on until a valid signal is detected. The ADRV9001 then wakes up the BBIC and starts to buffer the valid receive data to make sure the BBIC will not lose any valid data during the sleep. After the BBIC fully wakes up, it enables the receive channel to first retrieve all the buffered data at a preconfigured higher interface data rate. Then it further disables monitor mode to resume normal operation. Note: the BBIC can set the detect timer to be 0 so that the ADRV9001 will not perform any signal detection, and instead the BBIC will perform signal detection and terminate monitor mode by de-asserting the DGPIO pin at any time when a valid signal is found.

The ADRV9001 provides multiple signal detection methods to accommodate different radio standards, including receive signal strength indicator (RSSI), synchronization (SYNC), and fast Fourier transform (FFT). The RSSI method compares the receive signal level with a threshold to determine a valid signal so it can be used for any type of radio standards. SYNC method detects specific synchronization signal patterns defined by the DMR standard. FFT method is only applicable for standards using FSK modulation schemes. Therefore, there is no limitation to use monitor mode to other standards besides the DMR.

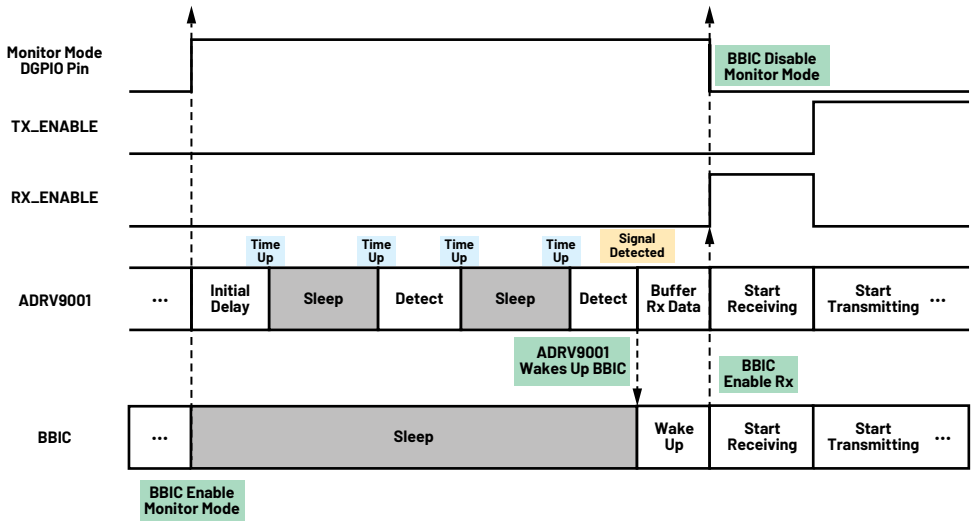

Figure 10. Timing events of ADRV9001 and BBIC during monitor mode.

Table 6 presents the power consumption during the sleep state and detect state utilizing different system-level power saving modes in monitor mode during the idle time period for the DMR use case shown in Figure 7.

Table 6. Power Consumption of a TDD DMR Profile During Sleep and Detect States Using System-Level Power Saving Modes 3, 4, and 5

System-Level Power Saving Mode	Power Consumption (mW)	
	Sleep	Detect
Mode 3	100	240
Mode 4	65	240
Mode 5	35	225

Depending on the timer configuration for sleep and detect states, the average power consumption during monitor mode could be determined. Although the ADRV9001 spends more power performing detection in detect state than sleep state, it allows the BBIC to sleep through the entire idle time period, which could result in higher overall system power saving.

Power Consumption Evaluation Through TES

All the power consumption measurements presented in this article are performed through the ADRV9001 TES with the ADRV9001 evaluation board (EVB). More information about TES and EVB can be found on the ADRV9002 product page. Both Xilinx® ZC706 and ZCU102 FPGA boards are supported by TES.[3] All the power saving options including monitor mode could be configured in TES, as shown in Figure 11.

The self-explanatory power saving configuration pages are very easy to use. To help users further evaluate power consumption, the ADRV9001 EVB is equipped with a power monitor chip to monitor and measure the power consumption in real time. Detailed power consumption at different power domains can be displayed in TES at 30 second intervals, as shown in Figure 12, which is a powerful visual tool to evaluate the power performance on-the-fly at different channel states. Good measurement accuracy can be achieved to be within ±2.5% error tolerance.

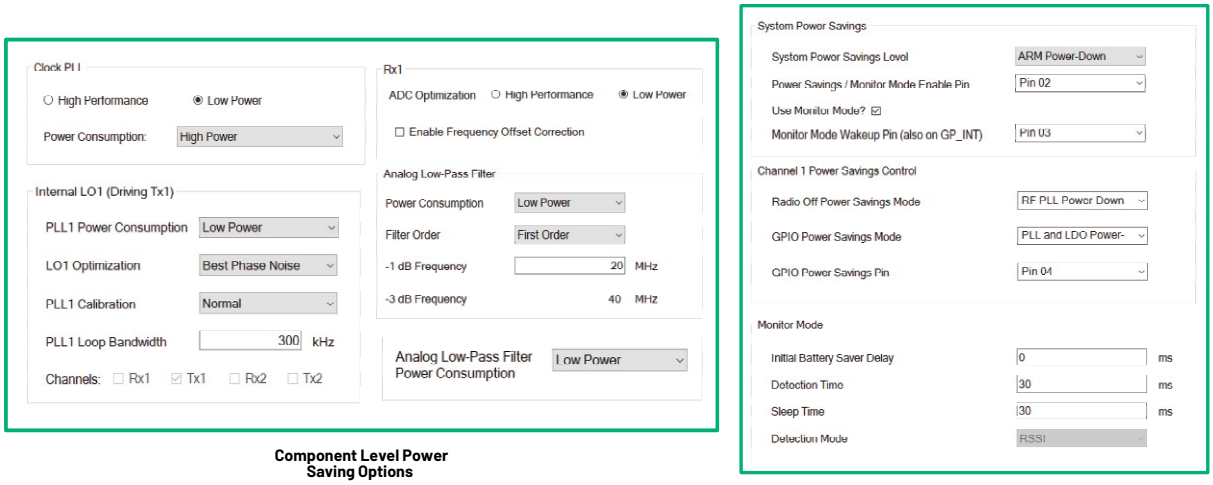

Figure 11. Power saving options and power monitor mode configuration in TES.

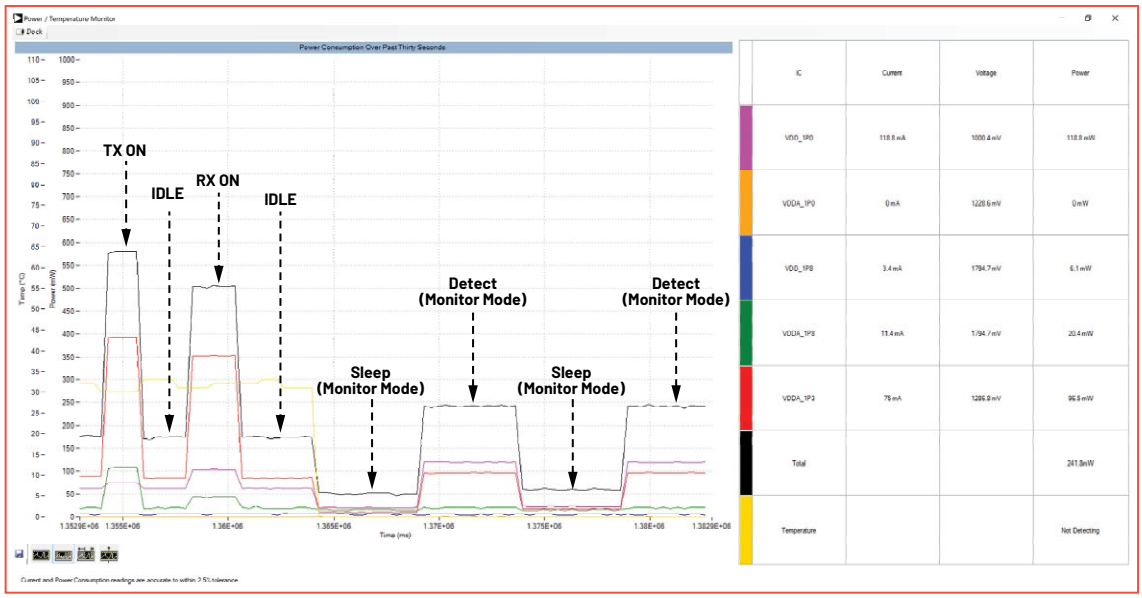

Figure 12. Power consumption real-time display using TES.

Conclusion

As discussed in this article, empowered with a variety of power saving options at the component, channel, and system levels, as well as the monitor mode, the ADRV9001 transceiver family is able to achieve a scalable power and performance for many mission critical applications. Understanding the associated performance trade-offs for each power saving option is crucial to determine the best system power saving strategy. All power saving options can be thoroughly evaluated through the ADRV9001 TES and EVB by a powerful real-time display of power consumptions on all power domains with a high accuracy.

References

[1] "Two-Way Radios and Battery Life." Hytera Europe, December 2016.

[2] ADRV9002 Dual Narrow-Band and Wideband RF Transceiver Data Sheet. Analog Devices, Inc., April 2021.

[3] ADRV9001 System Development User Guide. Analog Devices, Inc., October 2021.

About the Author

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