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The Next-Gen, Software-Defined Radio (SDR) Transceiver Delivers Big Advances in Frequency Hopping (FH)

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Abstract

This article provides an in-depth discussion of the high-level concept of frequency hopping (FH), the design principles of FH enabled through the flexible phase locked loop (PLL) architecture of the ADRV9002 SDR transceiver, and its four major FH features. These features empower users with the FH capabilities to handle applications such as Link 16 and fast real-time carrier frequency loading in both single- and dual-channel operation modes. Furthermore, the combination of FH with multichip synchronization (MCS) and digital predistortion (DPD) makes this SDR transceiver an attractive solution for achieving advanced requirements in today's complex communication systems.

Introduction

In contrast to conventional radio communications, frequency hopping (FH) defines a method of transmitting radio signals by rapidly changing its carrier frequency[1] and was first mentioned by Nikola Tesla in his 1903 U.S. patent, "Method of Signaling." Later, in 1942, actress Hedy Lamarr and composer George Antheil further solidified the concept by using a piano roll to change among 88 frequencies to prevent interference to the radio control of torpedoes. Over the past hundred years, from the non-real-time, slow speed communication between fixed command points in World War I to the real-time, high speed multimedia communication between aircrafts, ships, and land-based systems, FH has arrived at a new era in military applications. In addition to that, FH has been widely adopted in many wireless personal communication networks such as Bluetooth® Personal Area Network (PAN), as well as in consumer and hobby radio areas, such as walkie-talkies, model cars, and drones.

What Is Frequency Hopping?

The high-level concept of FH is described in Figure 1. The entire frequency band and time duration are divided into two-dimensional grids. At any given time slot, a different frequency subband is utilized for communication. This brings the benefit of high resistance to narrow-band interference and strong capability in combating malicious interception and jamming since the randomness of the hopping pattern equivalently adds another layer of security that is only decodable between the transmitter and receiver. In addition, FH signals can easily share the bandwidth with other conventional communications due to the minimal mutual interference, resulting in high spectrum efficiency. With an increased hop rate and a larger set of frequency subbands, the advantages of FH become more prominent, which makes it an attractive solution for many different applications.

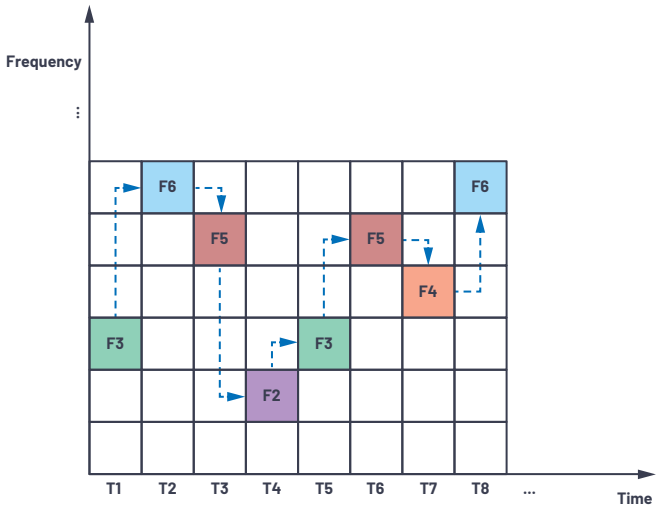


Figure 1. High-level concept of frequency hopping.

The Next-Generation SDR Transceiver

The ADRV9002 is a dual narrow-band and wideband SDR transceiver, which provides state-of-the-art RF performance as well as advanced system features such as DPD and FH. ADRV9002 operates from 30 MHz to 6 GHz and covers the ultrahigh frequency (UHF) bands; very high frequency (VHF) bands; industrial, scientific, and medical (ISM) bands; and cellular frequency bands in narrow-band (kHz) and wideband operation up to 40 MHz. Figure 2 depicts a high-level block diagram of ADRV9002. It includes dual transmit and receive channels with a set of advanced digital signal processing algorithms. The PLL structure highlighted in red is unique in the sense that instead of having one dedicated PLL for the receive datapath and one for the transmit datapath as many other transceivers, two RF PLLs are employed in the device and both PLLs can optionally source any receiver or transmitter, or both, or neither. This flexibility is essential to support FH in various TDD applications such as single-channel and dual-channel operations, including transmit-only mode (1T/2T), receive only mode (1R/2R), and transmit and receive mode (1T1R/2T2R). Both channel diversity and channel multiplexing are supported for the dual-channel operations. Furthermore, two PLLs can be operated in a ping pong mode to satisfy the stringent FH timing requirement.

Four Major FH Features of the ADRV9002

Very Fast FH with Two PLL Muxing and Fast PLL Retuning

FH is achieved by retuning the PLL before switching to a different frequency. The ADRV9002 provides different FH modes based on PLL usage.[2] Each time slot in Figure 1 stands for a hop frame, which is divided into a transition time period and a dwell time period, as shown in Figure 3.

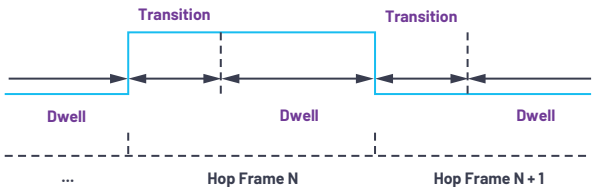


Figure 3. Hopping frame structure.

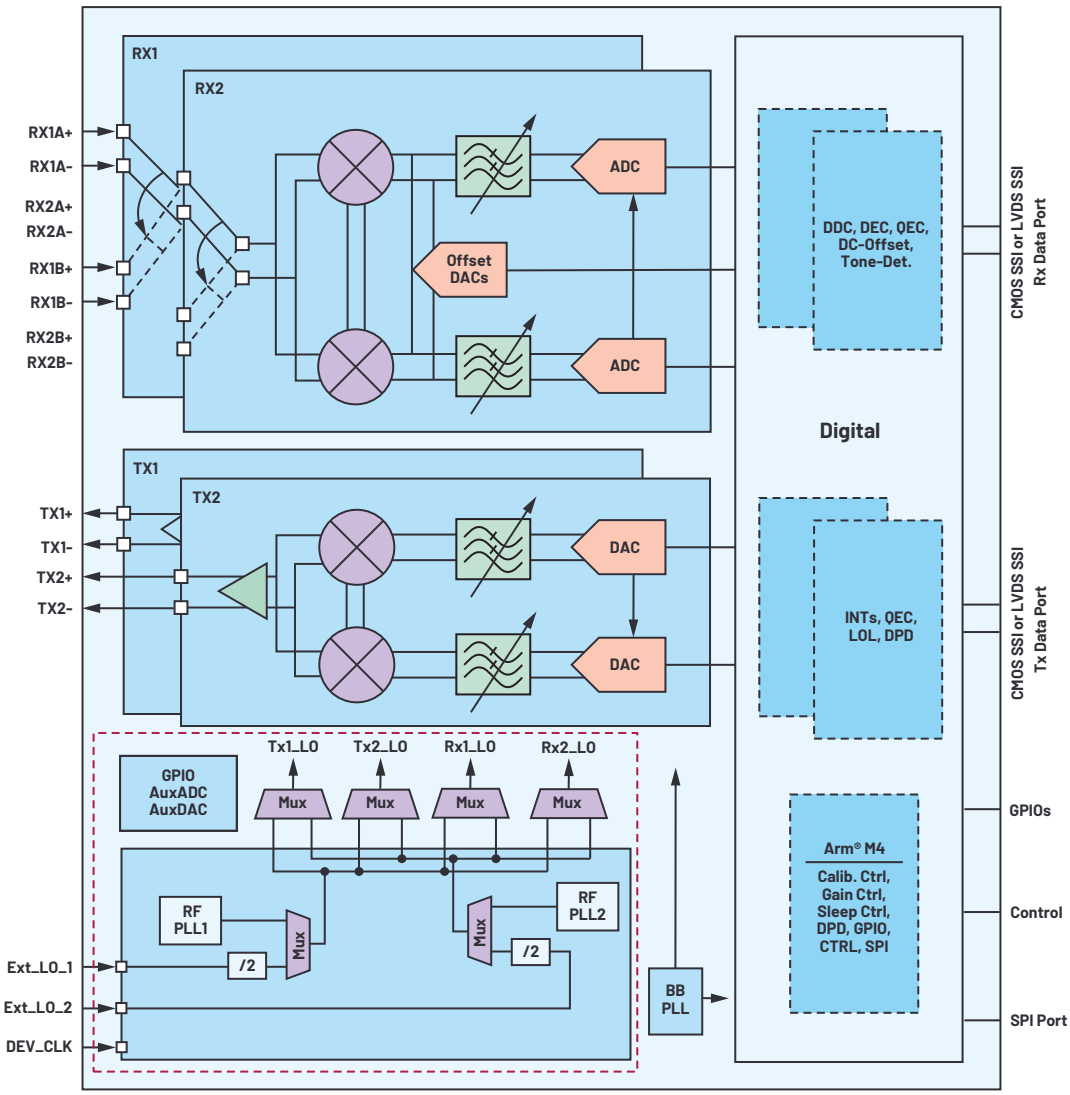


Figure 2. High-level block diagram of the ADRV9002 with flexible PLL design.

In a slower FH mode with a sufficiently long transition time (greater than the channel setup time and required PLL tuning time) between frequency changes, only one PLL is needed for a pair of transmit and receive channels in a TDD operation (PLL retune mode). To achieve faster FH with a shorter transition time (shorter than the channel setup time and required PLL tuning time), two PLLs are employed in the device (PLL mux mode). The two PLLs coordinate with each other in a ping pong fashion: while one PLL is used for the current frequency, the other PLL is retuned to the next frequency. This makes very fast FH possible and could significantly reduce the required transition time between different frequency changes. These two modes are summarized in Table 1.

Table 1. ADRV9002 FH Mode Based on PLL Usage

FH Mode	Transition Time	PLLs for a Pair of Channels	PLL Retune Time Allowed
PLL Mux	<PLL retuning time	Two PLLs	<Two transitions + one dwell
PLL Retune	>PLL retuning time	One PLL	<One transition

As shown in Table 1, the selection of these two modes depends on the transition time the user defines.

Figure 4 further describes the concept of PLL mux mode. As mentioned earlier, each time slot stands for a hop frame consisting of a transition time period and a dwell time period. While one PLL is used during the dwell time, the other PLL has started tuning from the beginning of the transition time of the same hop frame. It can continue the tuning until the end of the transition period of the next hop frame. Therefore, PLL mux mode is successful as long as the required PLL tuning time is less than the summation of one dwell time plus two transition times.

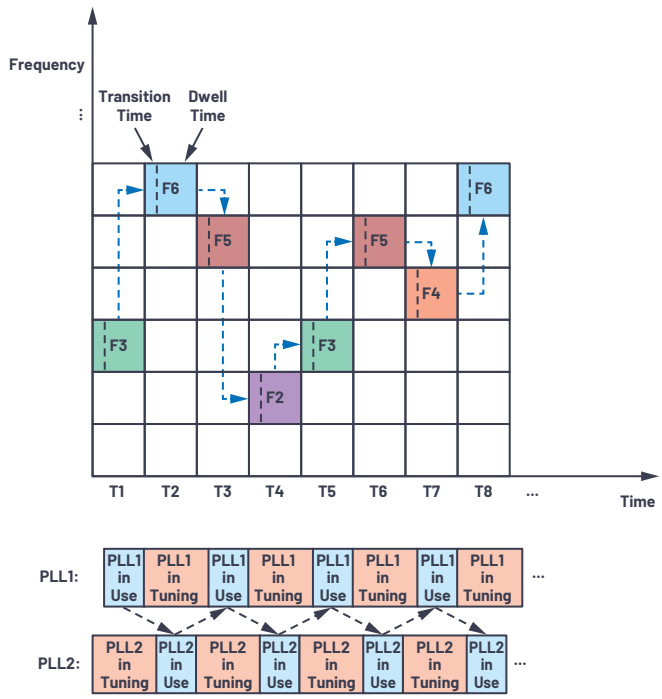


Figure 4. PLL mux mode for fast frequency hopping.

FH with PLL mux mode is critical for military applications such as Link 16. Link 16 is considered one of the most important tactical data link standards used by the North Atlantic Treaty Organization (NATO) as a jam-resistant, high speed digital data link operating in the radio frequency band of 960 MHz to 1.215 GHz.[3] By properly calibrating the entire hop frequency range at the initialization time, the ADRV9002 employs fast PLL retuning mode to meet the stringent timing requirement. PLL retuning time depends on the ADRV9002 PLL reference clock rate. Table 2 shows the fast PLL retuning time required based on a different PLL reference clock rate. At a PLL reference clock rate of 300 MHz, the fast PLL retuning time is approximately 15 µs. With a hop frame length of 13 µs for Link 16, the 15 µs of PLL retuning time when using PLL mux mode can satisfy the timing requirement if the transition time is greater than 2 µs, as shown in Table 1.

Table 2. PLL Retuning Time Using Fast PLL Retuning Mode

PLL Reference Clock (MHz)	Fast PLL Retuning Time (µs)
30	91
38.4	77
50	56
100	27
150	21
200	20
250	17
300	15

As described in the thesis paper "Performance Analysis of a JTIDS/Link 16 Type Waveform Transmitted over Slow, Flat Nakagami Fading Channels in the Presence of Narrowband Interference,"[3] Link 16 message data can be sent as either a single pulse or a double pulse, depending on the packing structure. The single-pulse structure consists of a 6.4 µs on-time and a 6.6 µs off-time with a total duration of 13 µs. The double-pulse structure consists of two single pulses that carry the same data but use different carrier frequencies, as shown in Figure 5. Therefore, the transition time could be 6.6 µs long (>2 µs), which makes Link 16 FH feasible with the ADRV9002.

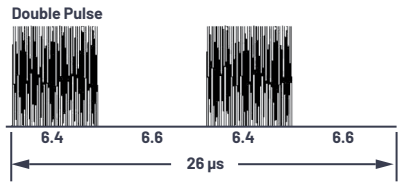


Figure 5. Standard Link 16 double-pulse structure.

Figure 6 shows the ADRV9002 transmit output (power vs. time and frequency vs. time) with Link 16-type hop frames (transmit-only FH is used for simplicity). Note in order to show the minimum transition time achievable by the ADRV9002, the experiment does not follow the standard Link 16 pulse structure in Figure 5. The on-time is increased from 6.4 µs to 11 µs and the off-time is reduced from 6.6 µs to 2 µs. A Tektronix RSA306B spectrum analyzer is connected to the transmit output port on the ADRV9002 evaluation board for observation. The upper plot shows the performance of power vs. time. It can be seen that transmit hopping happens every 13 µs with a transition time about 3 µs between consecutive transmit hop frames. The lower plot shows the performance of frequency vs. time. In this experiment, the transmit carrier frequency cycles through four different frequencies in a 1 MHz step size. As expected, the lower plot proves that the transmit output is also cycling through four different frequencies in a 1 MHz step size with good frequency accuracy throughout the entire dwell time.

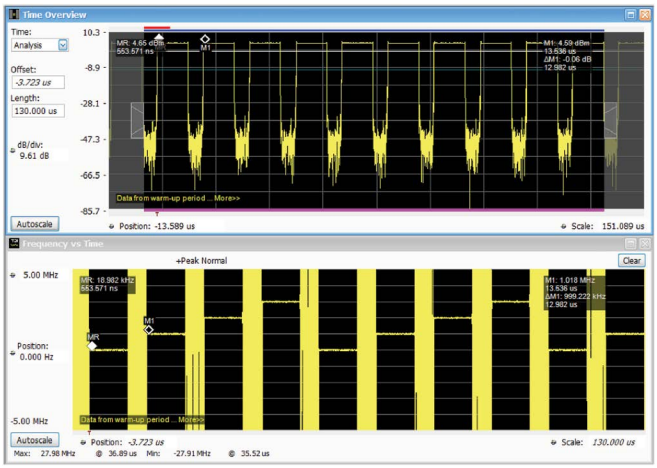


Figure 6. Transmit output for Link 16 Tx frequency hopping.

Further measurements are performed to study the frequency accuracy of the Link 16 FH using more advanced test equipment such as Keysight E5052B and R&S FSWP. In the example measurement shown in Table 3, the transmit carrier frequency is hopping at 400 MHz, 400.1 MHz, 400.2 MHz, and 400.3 MHz. The transmit input is constructed to produce 400 MHz output for all the hop frames. The measurement duration is set at 100 µs, which includes seven complete hopping frames. The frequency is measured at every 128 ns time interval. It can be observed that the PLL is fully locked at the beginning of the dwell time. The frequency error during the dwell time depends on the phase noise performance. Table 3 shows the average, maximum, and minimum frequency offset (the absolute difference between the output frequency and 400 MHz) performance for these consecutive seven hop frames. In most frames, the average frequency error is less than 1 ppm. The results are also found repeatable for tens of measurements. Note that the measurements could vary depending on the equipment and test configurations.

Table 3. Frequency Accuracy Performance with Link 16 Frequency Hopping

Hop Frame Number	Average Frequency Error (Hz)	Max Frequency Error (Hz)	Min Frequency Error (Hz)
1	348	730	46
2	424	997	4
3	267	563	20
4	327	892	7
5	253	569	2
6	394	903	12
7	253	677	17

The ADRV9002 provides user capability to fine tune the PLL loop filter bandwidth. The performance shown in Table 3 is achieved when the PLL loop filter bandwidth is configured at 1200 kHz. Larger PLL filter bandwidth improves the PLL retuning time, which guarantees the full lock of PLL before dwell time starts. When selecting the loop filter bandwidth, users should also evaluate the phase noise performance required in their applications.

Static and Dynamic Table Load up to 128 Different Frequency Entries

The ADRV9002 utilizes a hop table concept for all modes of FH.[2] A hop table contains a list of frequencies and other operation parameters for each hop frame. A hop table can be static, meaning it is loaded during the initialization and not allowed to change on-the-fly. It can also be dynamic, which means it is loaded while performing the hopping; in such a case, the user can change the table content on-the-fly. A similar concept of ping pong is employed so that the user can optionally load two different tables, each with a minimum of 1 to a maximum of 64 entries. While one table is being used for the current hop frame, the other table is being loaded to prepare for the next hop frame. Each entry notifies the ADRV9002 of the configurations for a certain hop frame. A hop table can be indexed by either incrementing the index automatically (start from the first entry of the first table to the last entry of the second table and then go back to the first entry of the first table again with two hop tables or loop continuously with one hop table) or accessing a specific entry at any time indicated through digital GPIOs.

Figure 7 shows hop table A and B, each with N entries ($1 \leq N \leq 64$). Each entry in the table includes four key parameters: hop frequency, intermediate frequency (for receive IF mode only), receive gain index, and transmit attenuation. In a TDD operation, users must notify the ADRV9002 which channel (either transmit or receive) is enabled for each hop frame by using a dedicated channel setup signal (one for each transmit channel and one for each receive channel). Therefore, although each entry in the hop table contains parameters for both receive and transmit, only the relevant parameters are utilized.

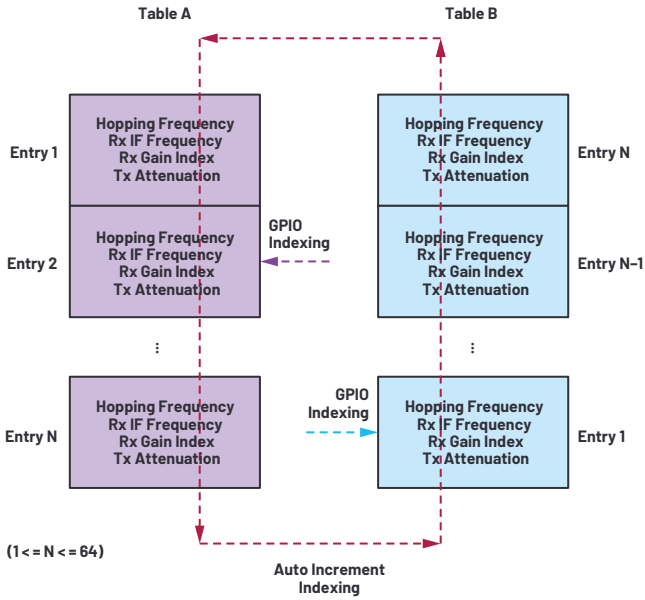


Figure 7. ADRV9002 hop tables content and the indexing method.

Before further discussing the hop table operation in FH, it is worthwhile to understand the high-level communication between the ADRV9002 and the baseband integrated circuit (BBIC).

As shown in Figure 8, BBIC acts as the main for FH operation, which sets up FH mode, the channel setup signals (Rx1_ENBALE, Rx2_ENABLE, Tx1_ENABLE, and Tx2_ENABLE), the HOP signals (HOP1 and HOP2), and the static or dynamic hop tables (hop frequency, receive IF frequency, receive gain, and transmit attenuation). BBIC communicates with the ADRV9002 through an SPI interface or DGPIOs. The ADRV9002 acts as the node for FH by accepting the signals from BBIC and then configures the datapath and LOs accordingly.

An example of a dynamic table loading with only one frequency per hop table A and B is described in Figure 9. This is an extreme case that allows users to change the hop frequency every frame on-the-fly. PLL mux mode is utilized in this example. As shown in Figure 8, both the rising and falling edge of the hop signal define the timing boundaries of a hop frame, each consisting of a transition time and a dwell time as mentioned earlier. The channel setup signal rising edge defines the type of hop frame that follows a one frame delay (this delay is necessary for PLL mux mode).

Note that the channel setup signal could stand for either the transmit setup signal or receive setup signal. Figure 9 shows a simplified version of the signal. Because TDD operation involves both transmit and receive, users need to configure both the transmit setup signal and receive setup signal separately. In addition to indicating the hop frame type, the channel setup signal can also be used to trigger the loading of a hop table initiated by the BBIC. The hop table loading should be completed before the hopping signal edge after the channel setup signal falling edge, and then PLL starts tuning to this frequency at the same hop edge and becomes ready for the next hop frame signaled by the next hop edge. Table A and Table B operate in a ping pong mode so that, after loading is complete, FH operates on the frequency of one table while the frequency of the other table is being tuned.

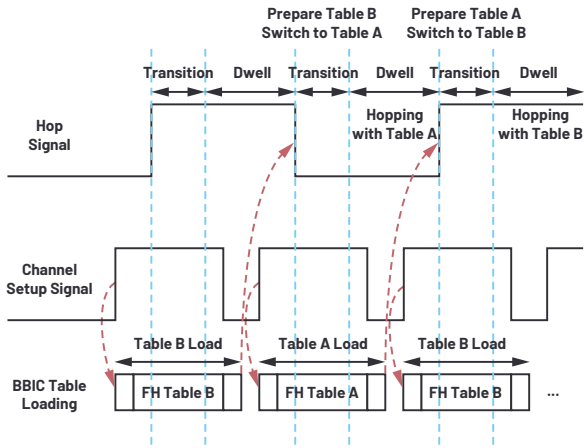
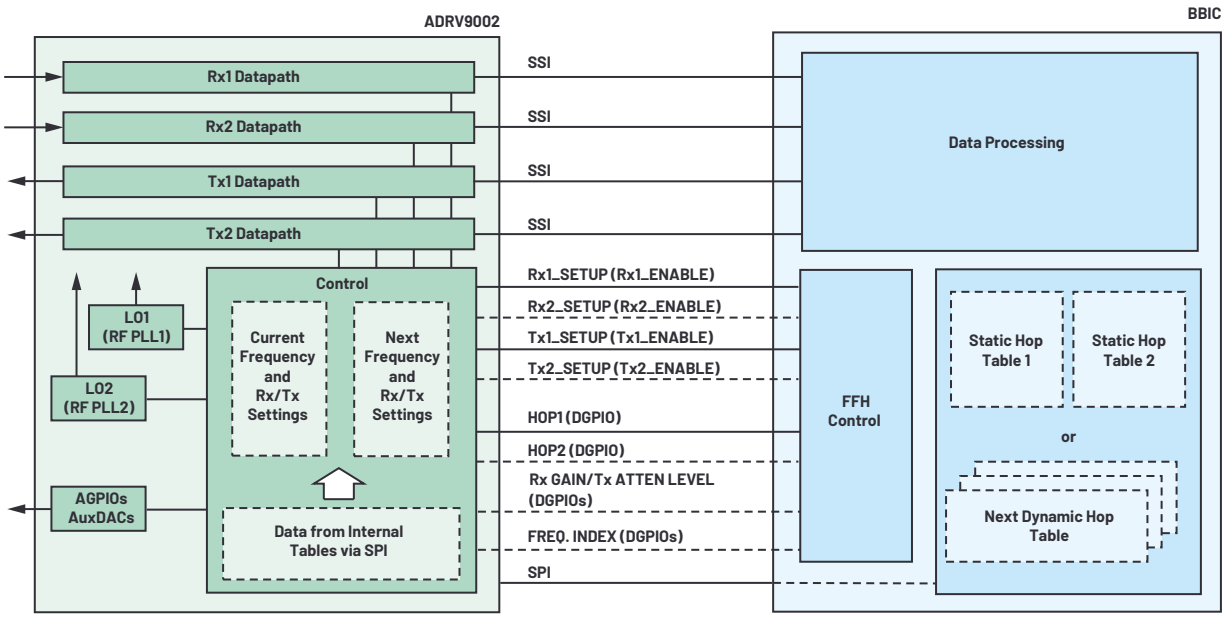


Figure 9. An example of dynamic table loading with one frequency per table using PLL mux mode.

Figure 10 presents the transmit frequency vs. time output with dynamic table loading for four entries per load and eight entries per load. The transmit input has four frames at 0 kHz, –100 kHz, –200 kHz, and –300 kHz frequency, and it is fed to the ADRV9002 by looping the frames continuously. It is also fully aligned and synchronized with hop frames so that the 0 kHz input frame aligns with 3.1 GHz LO. During FH, when LO changes to the next frequency, the transmit input frequency also changes to the next frequency.

Table A and Table B are dynamically loaded while performing FH (for simplicity and easy observation, the table content does not change from load to load). For four entries per load, we expect to see four consecutive transmit output frames at 3.1 GHz and then four consecutive frames at 3.1004 GHz, and the same pattern repeats again and again. For eight entries per load, we expect to see four consecutive transmit output frames at 3.1 GHz, four consecutive frames at 3.1004 GHz, four consecutive frames at 3.1008 Hz, and four consecutive frames at 3.1012 GHz, and the same pattern repeats again and again. The transmit output shown in Figure 8 proves that the dynamic table loading works as expected.



HOP*n*: Input event that indicates it is time to switch to the new frequency
TX*n*_SETUP: Input event that indicates that the next hopping will be on TX*n* channel
RX*n*_SETUP: Input event that indicates that the next hopping will be on RX*n* channel
Rx GAIN/Tx ATTEN LEVEL: Optional signal to select gain level during active Rx/Tx frame
FREQ. INDEX: Optional signal to select new frequency from preloaded tables inside the ADRV9002

Figure 8. A high-level block diagram of communication between the ADRV9002 and BBIC during frequency hopping.

Channel Diversity vs. Channel Multiplexing Using Dual Channels

As shown in Figure 2, the ADRV9002 supports dual transmit and receive channels. FH can be applied on both channels to achieve either channel diversity or channel multiplexing.

For diversity, both channels are hopping simultaneously by using the same PLL (either one or two), and the same hop tables and TDD timing configurations. The MCS capability provided by the ADRV9002 could be enabled to ensure that multiple channels on the same or different ADRV9002 devices are fully synchronized with each other with deterministic latency. Phase synchronization can also be achieved through MCS, which is performed each time PLL retunes frequency. With MCS, multiple channels could achieve synchronicity even during FH, making the ADRV9002 an attractive solution for MIMO diversity applications involving FH. More detailed descriptions regarding the requirements and limitations of using MCS during FH can be found in the ADRV9001 System Development User Guide.[2]

For channel multiplexing, each pair of channels uses one PLL and performs FH independently from each other. One limitation is that the very fast FH, which requires two PLLs for a pair of transmit and receive channels, can't be applied for channel multiplexing with one ADRV9002 device.

Besides 2T2R mode, it is worth mentioning that the ADRV9002 also supports 1T2R and 2T1R operations for FH, which provides greater flexibility to meet users' specific requirements.

Support of FH with DPD Operation

The ADRV9002 also supports DPD operation for both narrow-band and wideband applications. It corrects the nonlinearity of the power amplifier (PA) to significantly improve PA efficiency while achieving standard compliant adjacent channel power leakage ratio (ACPR) performance.

One advanced feature of the ADRV9002 is that DPD can be performed together with FH. In such a case, the ADRV9002 allows users to configure up to eight frequency regions, and the DPD algorithm creates an optimal solution for each frequency region. A DPD solution as a set of coefficients can also be stored and loaded at the end and the beginning of a transmission, respectively, for each region. This ensures PA linearity for the entire hop frequency range.

Since DPD is an adaptive filtering process that must capture a set of samples periodically for coefficient computation, the hopping frame length needs to be sufficiently long to satisfy the DPD capture length requirement. However, in cases when users only utilize the initially loaded DPD coefficients without the need for DPD updates, this restriction can be removed.

ADRV9002 tracking calibrations are usually not performed during fast FH. However, the initial calibrations are performed based on multiple frequency regions according to users' FH configurations to achieve the best possible performance.

FH Performance Evaluation Using ADRV9002 Transceiver Evaluation Software (TES)

FH performance can be evaluated thoroughly through the ADRV9002 TES with the evaluation board. Both the Xilinx® ZC706 and ZCU102 FPGA boards are supported by TES.[2] As shown in Figure 11, the FH configuration pages are easy to use to configure FH parameters, including FH operation mode, the hopping tables, the GPIO setting, the TDD timing, etc. FPGA synchronization features are built into the TES to allow users to accurately control the TDD timing so that the transmit or receive frames can be fully synchronized with hop frames. Many FH examples are also provided in TES for users to further explore.

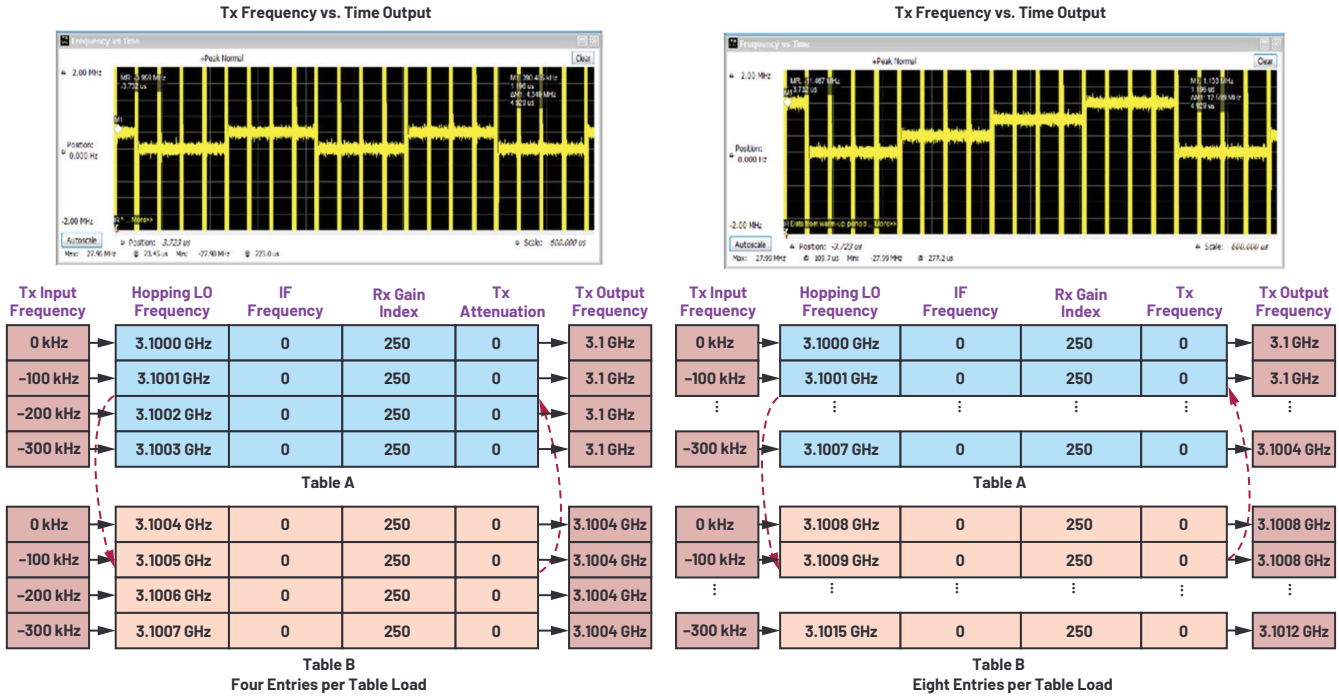


Figure 10. A comparison of dynamic table loading with four entries per loading and eight entries per loading.

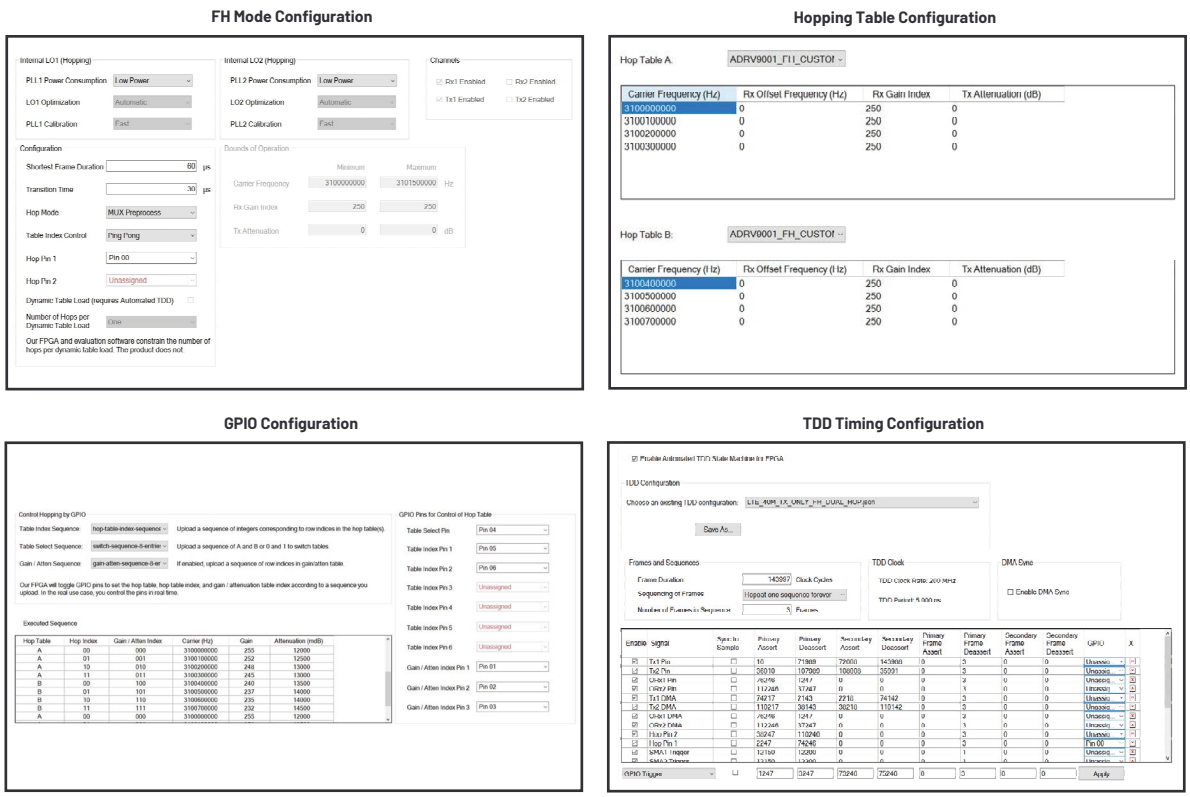


Figure 11. Configure FH through TES.

Conclusion

FH is one of the advanced system features provided by the next-generation SDR transceiver, the ADRV9002. With two PLLs, multiple FH modes, and flexibility in loading and indexing hop tables, the ADRV9002 empowers users with great FH capabilities to handle various applications and achieve advanced system requirements. All features can be thoroughly evaluated through the ADRV9002 TES and Software Development Kit (SDK).

References

[1] John G. Proakis. *Digital Communications*, 3rd edition. McGraw-Hill, March 1994.

[2] *UG-1828: ADRV9001 System Development User Guide*. Analog Devices, Inc., December 2020.

[3] Kao Chin-Han. "Performance Analysis of a JTIDS/Link-16-Type Waveform Transmitted over Slow, Flat Nakagami Fading Channels in the Presence of Narrowband Interference." Naval Postgraduate School, 2008.

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