JESD204C Primer: What's New and in It for You—Part 1

By **Del Jones**

Data-intensive applications across many industries continue to push the boundaries for delivering payload data fast and efficiently. 5G communications networks employ systems demanding more bandwidth in the infrastructure and its connecting components. In aerospace and defense industries, this translates into processing more information in a shorter amount of time in radar applications and complex data analysis instruments. Relatedly, testing and analysis of this rapid expansion in bandwidth translates into the need for higher speed and capacity in electronic test equipment.

This ever-increasing demand for data has led to the need for the JEDEC Solid State Technology Association to introduce the latest evolution in the JESD204 standard for high speed serial links between data converters and logic devices. The B revision of the standard, released in 2011, pushed the serial link data rates to 12.5 Gbps and ensured deterministic latency from one power cycle to the next while enabling the higher bandwidth requirements of the converter-based applications at the time. The newest revision of the standard, JESD204C, was released late in 2017 to continue to support the upward trend in performance requirements for this and next generation's multigigabit data processing systems. The JESD204C subcommittee established four high level goals for this new revision of the standard: increase the lane rates to support even higher bandwidth applications' needs, improve the efficiency of payload delivery, and provide for an improved robustness of the link. In addition, they wanted to write a spec that had more clarity than JESD204B while also fixing some of the errors that were in that version of the standard. It was also desired that a backward-compatible option to JESD204B be made available. The complete JESD204C specification is available through JEDEC.

This two-part primer serves as an introduction to the JESD204C standard by highlighting the differences from JESD204B and detailing the key new features intended to meet the previously stated goals and make for a more user-friendly interface while delivering the bandwidth capability needed for a variety of industries. Part one of this series provides a high level view of these differences and the new features. Part two will dive a little deeper into the most important new features.

Summarizing the Changes for JESD204C

The JESD204C specification has been organized for improved readability and clarity, and it includes five major sections. The "Introduction and Common Requirements" section covers requirements that apply to all layers of the implementation. The sections for the physical, transport, and each of the data link layers (8b/10b, 64b/66b, and 64b/80b) cover requirements that apply specifically to those layers of the implementation. Several new terms are introduced throughout the standard, mostly associated with the new 64b/66b and 64b/80b link layers as well as the new synchronization process for these link layers. While the transport layer remains intact from JESD204B, the physical layer has undergone quite a bit of change. The aforementioned changes, along with small changes to clocking and synchronization and the addition of forward error correction (FEC), are all summarized in the following sections.

New Terminology

There are several new terms and configuration parameters introduced in JESD204C that are primarily used to describe the functions associated with the 64b/66b and 64b/80b link layers. Table 1 lists the most relevant terms and parameters along with a brief description of each. These will be described further in the following sections.

Table 1. New Terms and Parameters

Term	Definition
Block	A structure starting with a 2-bit sync header containing either 66 or 80 (BkW) bits total
BkW	Block width; the number of bits in a block
cmd	Command, as related to the command channel
Command Channel	Data stream using extra bandwidth afforded from sync headers
E	The number of multiblocks in an extended multiblock
EMB_LOCK	A state that asserts that extended multiblock alignment has been achieved
EoEMB	End of extended multiblock identifier bit
EoMB	End-of-multiblock sequence (00001); also known as the pilot signal
Extended Multiblock	A set of data containing one or more multiblocks
FEC	Forward error correction
Fill Bit	A bit used to artificially extend the block size in 64b/80b encoding mode
LEMC	Local extended multiblock clock
Multiblock	A set of data containing 32 blocks
PCS	Physical coding sublayer
SH	Sync header
SH_LOCK	A state that asserts that sync header alignment has been achieved
Sync Header	Two bits, which guarantee a transition preceding every block

Transport Layer

For JESD204C, the transport layer remains intact from JESD204B. The frames of data assembled in the transport layer are sent across the link in 8-octet blocks. Changes to the organization, text, and figures have been made to this section of the standard to provide improved clarity.

Due to the nature of the 64-bit encoding schemes, there are some configurations where frame boundaries will not align with the block boundaries (frames may not include exactly eight octets). The details and implications of this will be covered in part two of this series.

Data Link Layer

As previously implied, there are two major sections of the standard that cover the different data link layer schemes. The 8b/10b encoding scheme from previous versions of the JESD204 standard, including the use of the SYNC~ pin and use of K.28 characters for synchronization, lane alignment, and error monitoring, remains intact as a backward-compatible option. However, most applications, in the long-term, are likely to use one of the new 64-bit encoding schemes that have been added in JESD204C. The 64b/66b scheme will provide the highest efficiency and is based on IEEE 802.3. While it is referred to as encoding, there is not actually any encoding (similar to 8b/10b) going on. The scheme just adds two header bits to 64 bits of payload data. Since this is the case, scrambling is made mandatory so that dc balance is maintained and to ensure enough transition density so that the clock and data recovery (CDR) circuitry in the JESD204C receiver can reliably recover the clock. This will be covered in more detail in part two of this series. A 64b/80b option has also been added that keeps the same clock ratios as the 8b/10b scheme while allowing for the use of new features like forward error correction. Neither of the 64-bit encoding schemes is compatible with the 8b/10b encoding used in JESD204B.

Physical Layer

JESD204C has increased the upper limit on lane rates to 32 Gbps while maintaining the lower limit of 312.5 Mbps established in earlier revisions. The upper limit in JESD204B is 12.5 Gbps. While not strictly forbidden, 8b/10b encoding is not recommended for lane rates above 16 Gbps and neither of the 64b schemes are recommended for lane rates below 6 Gbps.

JESD204C introduces two categories of classes to define the characteristics of the physical interface. Table 2 lists the lane rate associated with each class. Table 3 lists the channel types within Class C and the associated emphasis and equalization characteristics.

Table 2. Lane Data Rates for Data Interface Classes

Data Interface Class	Minimum Data Rate (Gbps)	Maximum Data Rate (Gbps)
B-3	0.3125	3.125
B-6	0.3125	6.375
B-12	6.375	12.5
C	6.375	32

Table 3. JESD204C 32 Gbps Interface Device Class Features

Class	Relative Power	Transmitter FFE (Minimum)	Receiver CTLE (Minimum)	Receiver DFE Taps (Minimum)
C-S	Low	9.5 dB	6 dB	0
C-M	Medium	9.5 dB	9 dB	3
C-R	High	9.5 dB	12 dB	14

JESD204C also introduces the concept of the JESD204 channel operating margin (JCOM), which is used to confirm compliance to the Class C PHY layer standard. This calculation of the operating margin supplements the eye masks that apply the Class B PHY layer implementations that are described in this and in previous revisions of the standard.

Clocking and Synchronization

JESD204C will retain the use of SYSREF and device clock as defined in JESD204B. However, when using either of the 64-bit encoding schemes, instead of aligning the LMFC, the SYSREF is used to align the local extended multiblock counter (LEMC) to provide a mechanism for deterministic latency and multichip synchronization.

The synchronization process for the 64-bit encoding schemes is completely different than the one used in JESD204B. The SYNC signal has been eliminated and sync initialization and error reporting will now be handled in application layer software. Therefore, there is no code-group sync (CGS) or initial lane alignment sequence (ILAS). Sync header sync, extended multiblock sync, and extended multiblock alignment are new sync-related terms used to describe the synchronization process. Each of these synchronization phases are achieved using a 32-bit sync word. This is discussed in detail in part two of this series.

Note that for 8b/10b encoding, both the SYNC pins and the ILAS are retained.

Deterministic Latency and Multichip Synchronization

As implied above, the mechanism for achieving deterministic latency and multichip synchronization remains mostly intact from JESD204B. When using one of the 64-bit encoding schemes, there is no Subclass 2 option. Instead, only Subclass 1 operation is supported and the SYSREF signal is used to align the LEMC across all devices in the JESD204 subsystem.

Forward Error Correction

To meet the goal of providing a more robust link at higher lane rates, an FEC option has been included in JESD204C. This algorithm is based on fire codes and may be particularly useful for instrumentation applications. This is an optional feature that is only available when using one of the 64-bit encoding schemes.

Fire codes are cyclic codes that correct single-burst errors. The advantage of cyclic codes is that their codewords can be represented as polynomials—as opposed to vectors—over a finite field. Fire codes use a syndrome that can be split into two components for faster decoding.

More Information

Coming soon, in part two of the JESD204C primer series, we will dive a little deeper into the key elements of the JESD204C standard that enable the problem-solving technology we described in the opening paragraphs. Specifically, the bandwidth efficiency improvements enabled by the 64b/66b encoding scheme is given a closer look as is the bandwidth-increasing 32 Gbps physical layer specification. More depth is also provided on the new synchronization process as well as the optional forward error correction aspect of the standard that improves link robustness.

For more information on JESD204 and its implementation in Analog Devices products, please visit ADI's JESD204 serial interface page.

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