Flexible ECG Front-End IC Serves Ultralow Power IoT Edge Node Signal Processing Designs

By David Plourde

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As system designers search for power efficient, signal conditioning components, they may find that there are very few ICs available under 100 μ A supply current and even fewer that include a small package variant. With battery life and board space becoming critical specifications for the growing number of wireless sensor networks (WSNs), the lack of available options can be frustrating. In a search for a low power edge node IoT component, an analog front-end IC such as a heart rate monitor for wearable products may not even show up, or it may be quickly dismissed as too application specific. However, at 50 μ A supply current and a tiny 2 mm \times 1.7 mm WLCSP package, an ADI ECG front-end IC deserves a closer look. When designers dig deeper, they'll find that its flexible architecture is basically an instrumentation amplifier (IA) and a handful of op amps that can be configured to make some useful ultralow power signal processing circuits for more than just healthcare or fitness applications.

A simplified, single-lead electrocardiogram (ECG) front end is shown in Figure 1. It consists of an indirect current mode IA with a standalone transfer function of:

$$IA_{OUT} = \left(1 + \frac{Rfb}{Rg}\right)(V_{IN}) + Ref$$

In the case of this front end, giving a fixed gain of 100. The reference of the IA is driven by the high-pass amplifier (HPA), which is configured as an integrator in feedback with its input tied to IA_{0UT} and crossover frequency set by an external capacitor and resistor. The HPA will force HPDRIVE to whatever voltage is needs to keep HPSENSE and therefore IA_{0UT} at the ref voltage. This circuit creates a first-order high-pass filter with cutoff frequency:

$$fc = \frac{100}{2\pi RC}$$

For diagnostic quality ECG, the cutoff frequency is typically set to 0.05 Hz, while 7 Hz may be suitable for fitness applications detecting heart rate only. The high-pass filter function solves the issue of rejecting the large dc half-cell potential (due to electrode/skin contact) and low frequency baseline wander associated with ECG measurements, while amplifying the higher frequency ECG signal (1 mV to 2 mV). The architecture enables a large gain since the rejection of the dc half-cell potential (up to 300 mV) occurs at the input of the IA. An added benefit is the rejection of the IA's offset and offset drift. Monitoring HPDRIVE with respect to ref will show an inverted version of the input offset being autocorrected.

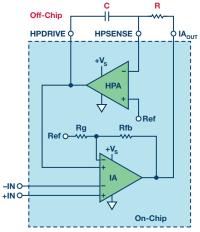


Figure 1. Simplified single-lead ECG front end.

While the design originally targeted ECG applications, any application that requires amplification of small, low frequency signals could benefit from its low power and small size—an electromagnetic water flow sensor, for example. If dc measurements are required, then a simple modification to the circuit is all that is needed. Figure 2 shows a dc-coupled IA with a fixed gain of 100. This is done by removing the R and C from Figure 1 and shorting HPSENSE to HPDRIVE, making the HPA a unity-gain buffer. This will still force the IA reference to the reference voltage. In this case, IA offset voltages should be considered.

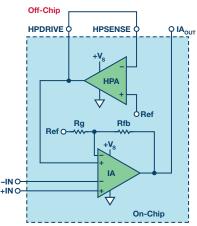


Figure 2. DC-coupled IA with fixed gain of 100.

If a gain of 100 is too high or the bandwidth of 1 kHz is too low, the circuit could be modified, as shown in Figure 3. The HPA is now configured as an inverting amplifier with a gain of -R2/R1 and input fed back from IA_{out}. The new transfer function can be simplified as follows:

$$IA_{OUT} = \frac{V_{IN}}{\left(\frac{1}{100} + \frac{R2}{R1}\right)} + Ref$$

By configuring the HPA as an attenuator (R2 < R1), gains of less than 100 can be achieved. Due to the 300 mV differential input limit and stability of the circuit, it is not recommended to go below a gain of 10. Table 1 shows some gain configurations to consider.

Table 1. DC-Coupled IA with Different Gain and Bandwidth Configurations

R2	R1	Gain	Bandwidth
Short	Open	100	1.2 kHz
10 kΩ	1 MΩ	50	2.4 kHz
40 kΩ	1 MΩ	20	6.5 kHz
90 kΩ	1 MΩ	10	15.2 kHz

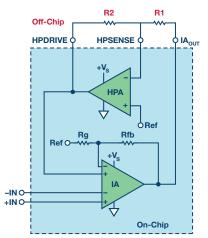


Figure 3. DC-coupled IA with adjustable gain and bandwidth.

If dc precision remains important, then leaving the IA in a gain of 100 and modifying the circuit per Figure 4 provides a means of compensating offsets of the IA and any attached sensors. The adjusted transfer function is shown below:

$$IA_{OUT} = 100 \left(V_{IN} - \left(\frac{R2}{R1} \right) V_{TUNE} \right) + Ref$$

 V_{TUNE} is the source voltage used to correct for offset voltages and could be provided by a filtered PWM signal from a microcontroller or driven directly from a low power DAC. The HPA remains configured as an inverting amplifier with gain of –R2/R1 and can be used to further adjust the range and resolution of the offset correction. Breaking down $V_{\rm IN}$ to components and plugging into above equation gives target transfer function:

$$V_{IN} = V_{SIGNAL} + V_{OS}$$
$$V_{OS} = \left(\frac{R2}{R1}\right) V_{TUNE}$$

 $IA_{OUT} = (100) V_{SIGNAL} + Ref$

The total offset can be compensated by attaching a sensor without V_{SIGNAL} applied. Just measure IA_{out} with respect to reference and adjust (R2/R1) V_{TUNE} until the voltage is close enough to zero.

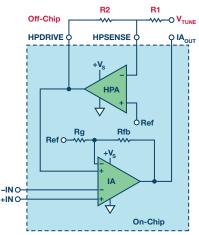


Figure 4. DC-coupled IA with offset compensation.

Before utilizing the above mentioned circuit configurations for low power loT designs, the rest of the AD8233 ECG front-end solution should be understood. The circuit is detailed in Figure 5. The first op amp, A1, is fully uncommitted and typically used for additional gain and/or filtering after the IA stage. It could be similarly advantageous for other sensor applications. Amplifier A2 is typically used as the right leg drive in ECG solutions. A buffered version of the IA's input common mode appears at the inverting input of A2 where:

$$V_{CM} \sim \frac{+IN + -IN}{2}$$

The amplifier would normally be configured as an integrator with a capacitor placed between RLDFB and RLD, while RLD drives a third electrode improving the overall system common-mode rejection ratio (CMRR). Unless a useful circuit can be built from this amplifier, it is better to power down the amplifier by tying RLDSDN digital input to ground, and leaving the RLD and RLDFB pins floating.

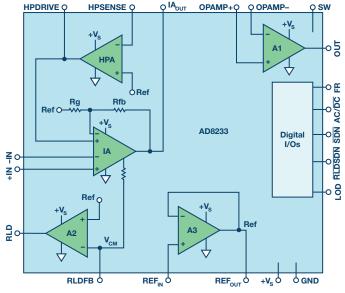
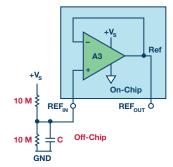


Figure 5. Complete ECG and low power signal conditioning front end.

The third op amp, A3, is an integrated reference buffer that drives the reference voltage both on-chip and off-chip at REF_{out} . Usually, $\text{REF}_{\mathbb{N}}$ is set to +Vs/2, where the single-supply +Vs can range from 1.7 V to 3.5 V. An easy low power solution is to tie two 10 M Ω resistors as a voltage divider from +Vs to GND, as shown in Figure 6. A capacitor is added between REFIN and GND to help with any noise pickup. Alternatively, REF_{\mathbb{N}} could be driven from an ADC reference or used to level shift the IA output.



3 V

Figure 6. Low power reference.

The digital input FR enables the fast restore function, which is beneficial when using the ac-coupled circuit in Figure 1. It will take some time to charge the external capacitor during startup or in the event of a dc step at the input. When this happens, the IA will rail until the integrator has settled. The automatic fast restore detects this event and switches a smaller resistor in parallel with the external resistor for a fixed amount of time, greatly speeding up the settling time. The SW pin is used to quickly settle a second external high-pass filter if needed.

The AC/DC digital input determines the method for lead off detection used in ECG applications, but could also be utilized as a wire break detection for other sensors at the input. If configured correctly, the digital output LOD would indicate when one of the IA inputs becomes disconnected from the sensor.

In addition to its small size and low active power dissipation, the AD8233 incorporates a shutdown pin (SDN) that drops the total supply current to less than 1 μ A. This is convenient when taking infrequent sensor measurements, which greatly increases overall battery life. The wire break detection will remain functional even in shutdown mode.

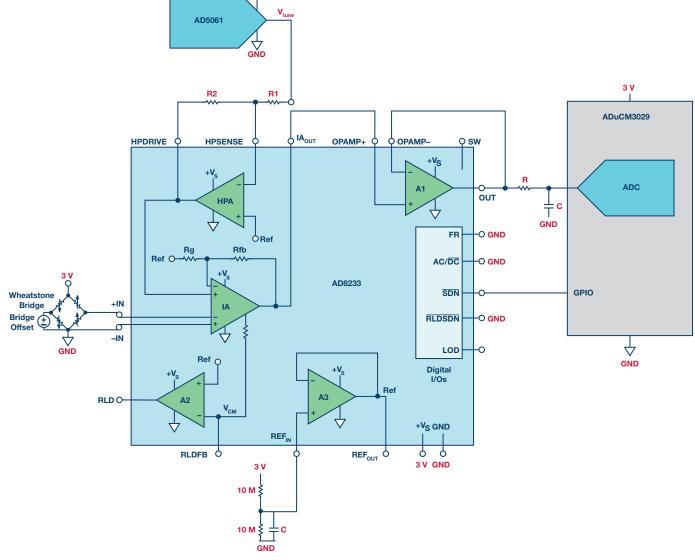


Figure 7. Low power pressure sensor circuit.

Now that the complete AD8233 chip is better understood, let's take a look a couple of different sensor application ideas. Table 2 provides a getting started guide for building non-ECG circuits.

Table 2. AD8233 Starting Guide for Non-ECG Applications

Pins	Action	
+Vs to GND	Battery or regulated voltage (1.7 V to 3.5 V)	
REF _ℕ	Set to +Vs/2—Figure 6	
+IN, -IN	Connect sensor (nominal Vcm = $+Vs/2$)	
HPSENSE, HPDRIVE, IA_{out}	Reference figures 1 to 4	
RLD, RLDFB, SW, LOD	Float	
FR, AC/ $\overline{\text{DC}}$, $\overline{\text{RLSDN}}$	Tie to GND	
SDN	Tie to +Vs (active), tie to GND (shutdown)	
OPAMP+, OPAMP-, OUT	Flexible use (additional gain/filtering after IA)	
REF _{OUT}	External reference for A1 and ADC or microcontroller	

IoT Edge Node Applications for the AD8233

A great example of where the fixed gain of 100 and offset correction in Figure 4 could be suitable is a pressure sensor application based on a Wheatstone bridge. The bridge naturally sets the input common mode to +Vs/2. Depending on measurement range and current required, the bridge could be driven by REF_{out} or the uncommitted op amp, such that the bridge supply current is disabled in shutdown. Figure 7 shows an example circuit. The AD5601 DAC is a good choice for correcting the bridge and IA offset, due to its low power (60 μ A at 3 V), shutdown pin, and small SC70 package. The op amp (A1) is left as a placeholder buffer with option to set additional gain or filtering of noise and 60 Hz. The output amplifier drives an on-board ADC of the ultralow power ARM[®] Cortex[®]-M3 (ADuCM3029) that also comes in a space saving WLCSP package. A GPIO from the ADuCM3029 can control the shutdown pin of the AD8233.

Another application that could take advantage of the circuit in Figure 4, is making a temperature measurement with a thermocouple. A K-type thermocouple is fairly linear over a wide temperature range with a Seebeck coefficient of about 41 μ V/°C at room temperature (25°C). Assuming the reference or cold junction was compensated for, the output of the IA would be a gained up version of the measurement junction ~4.1 mV/°C (for more accurate results, use a NIST lookup table). The output of a thermocouple is the difference between the measurement junction and the reference junction, so an equivalent reference junction drift must be added to cancel it.

To start the process, determine the expected reference junction temperature range use the NIST table to determine the expected drift. For example:

0°C to 50°C:
$$\frac{2.023 \text{ mV} - 0 \text{ mV}}{50°C} = 40.46 \ \mu\text{V}/°C$$

25°C to 100°C: $\frac{4.096 \text{ mV} - 1 \text{ mV}}{75°C} = 41.28 \ \mu\text{V}/°C$

By placing an accurate temperature sensor at the reference junction, the results can be fed back into $V_{\mbox{\tiny TUNE}}$ and adjusted by $-\mbox{\scriptsize R2/R1}$ to get the correct drift. Note that the drift of temperature sensor should be negative or the IA

inputs swapped in order to get a positive drift at the IA output. To separate offset and drift correction, the circuit could be split into a summing node where the offset is fixed at V_{TUNE2} via -R2/R3. See updated transfer function:

$$IA_{OUT} = 100 \left(V_{IN} - \left(\frac{R2}{R1}\right) V_{TUNE} - \left(\frac{R2}{R3}\right) V_{TUNE2} \right) + Ref$$
$$V_{IN} = V_{MEAS_{TC}} - V_{REF_{TC}} + V_{OS_{IA}}$$

The modified circuit is shown in Figure 8. Note that the input common mode is set to +Vs/2 by 10 M Ω pull-up on +IN and 10 M Ω pull-down on -IN. This configuration would enable use of lead off detection of the AD8233 by pulling +IN to +Vs in the event of a wire break. This could be monitored at the LOD pin. The AD8233 also has an integrated RFI filter to assist with any high frequency pickup from the thermocouple. Placing additional resistance in series with the inputs can reduce the cutoff frequency.

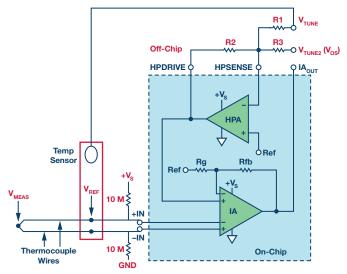


Figure 8. Thermocouple circuit with reference junction compensation and wire break detection.

Conclusion

Breaking down the AD8233 proved it to be more than an ECG front end. Its unique mix of active low power (50 μ A), tiny 2 mm \times 1.7 mm WLCSP package, shutdown pin, and flexible architecture enables smaller, lighter designs with extended battery life. So the next time you are searching for components for your IoT, WSN, or any other low power design acronym, take a look at the AD8233 and see what circuits you can come up with. Your battery's life may depend on it.

References

Castro, Gustavo and Scott Hunt. "How to Stay Out of Deep Water when Designing with Bridge Sensors." *Analog Dialogue*, Volume 48, 2014.

Duff, Matthew and Joseph Towey. "Two Ways to Measure Temperature Using Thermocouples Feature Simplicity, Accuracy, and Flexibility." *Analog Dialogue*, Volume 44, 2010.

ITS-90 Table for Type K Thermocouple.

David Plourde [david.plourde@analog.com] is an analog IC design engineer in Analog Devices' Linear and Precision Technology Group in Wilmington, MA. His interests include low power design and system-level solutions, primarily for healthcare applications. David received his B.S. and M.S. degrees from Worcester Polytechnic Institute. He joined Analog Devices in 2006 as a product/test engineer.

