Powering GSPS or RF Sampling ADCs: Switcher vs. LDO

By Umesh Jayamohan

Introduction

The analog-to-digital converter (ADC) is an integral component in any system that depends on gathering information from the outside (analog) world for (digital) processing. These systems vary in applications from communications receivers to electronic test and measurement, to military and aerospace, to name a few. Advancements in silicon processing technology (such as 65 nm CMOS and 28 nm CMOS) have enabled the high speed ADC to cross the GSPS (gigasample per second) barrier. What this provides the systems designer with is the ability to sample wider and wider bandwidths for digital processing. Systems designers are constantly trying to reduce overall power for environmental and cost reasons. Traditionally, low noise LDO (low dropout) regulators have been recommended by ADC manufacturers for powering GSPS (or RF sampling) ADCs in order to extract maximum performance. However, this is not an efficient power delivery network (PDN) implementation. Systems designers are increasingly demanding to use switching power regulators to power the GSPS ADC directly without a significant drop in ADC performance.

The solution lies in careful PDN implementation and layout to ensure that the ADC performance is not compromised. This article discusses the difference between linear and switching supplies and demonstrates that combining a GSPS ADC with a dc-to-dc converter can significantly improve system power efficiency without any penalty in ADC performance. This article discusses the performance of the GSPS ADC using a combination of power delivery networks and makes comparative analyses on cost and performance.

Traditionally Recommended PDN for GSPS ADCs

A high bandwidth, high sample rate ADC (or GSPS ADC) can have multiple power domains (such as AVDD or DVDD). With the shrinking geometries, not only have the power domains increased in number, but the number of different voltages required to power the ADC have increased as well. For example, the AD9250,[1] a 14-bit,170 MSPS/250 MSPS, JESD204B, dual analog-to-digital converter, is built using the 180 nm CMOS process and has three domains: AVDD, DVDD, and DRVDD. However, all three domains are the same voltage: 1.8 V.

Now consider the AD9680,[2] a 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS JESD204B, dual analog-to-digital converter, which is built on a 65 nm CMOS process. This GSPS ADC has seven different domains (AVDD1, AVDD1_SR, AVDD2, AVDD3, DVDD, DRVDD, and SPIVDD) and three different voltages: 1.25 V, 2.5 V, and 3.3 V.

The proliferation of these supply domains and the various voltages is somewhat of a necessity for operation at these sample rates. They are required to ensure proper isolation between the various circuit domains (such as sampling, clock, digital, and serializer) while providing optimal performance. It is for this very reason that the ADC manufacturers design the evaluation
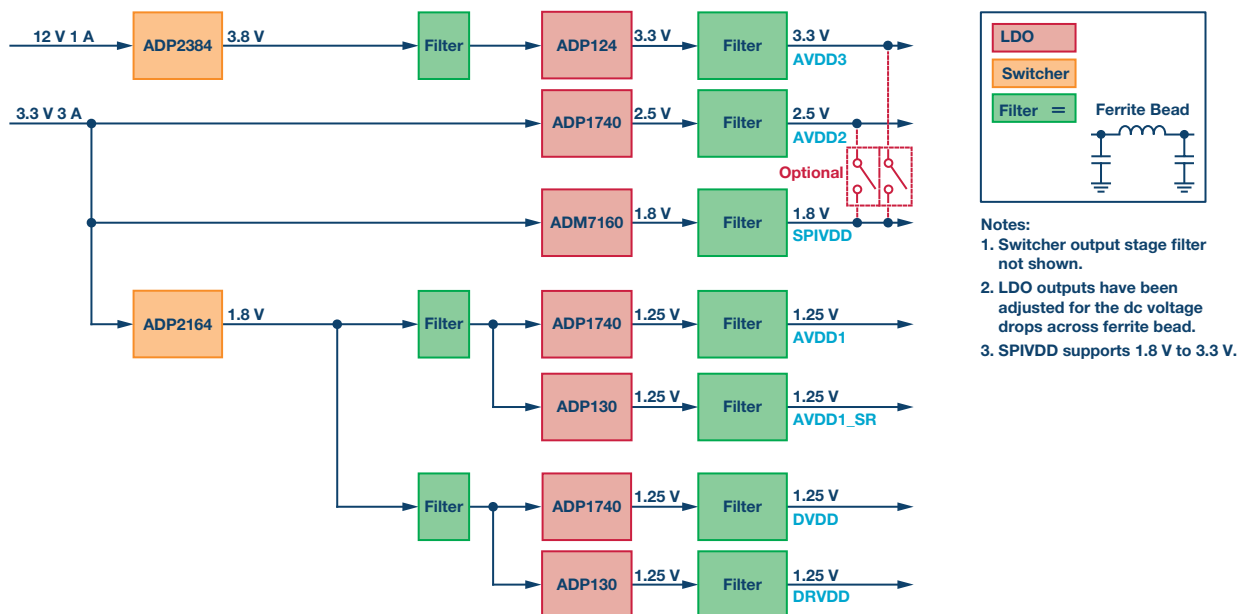

Figure 1. Default PDN for the AD9680 evaluation board.

boards and recommend an elaborate power supply design to ensure minimal risk and maximum performance. For example, Figure 1 shows the block diagram representation of the default PDN used in the AD9680 evaluation board. The power input is derived from the 12 V/1 A and 3.3 V/3 A supplies offered by the FMC (FPGA mezzanine card) connector using the Vita57.1 specification. The ADP2384[3] and ADP2164[4] dc-to-dc converters were used to step down the voltages to a manageable level so the LDOs can regulate without having to go into thermal shutdown.

It does not take much to realize that this is an expensive implementation, with seven LDO regulators—one for each domain. This PDN may be the most optimal in terms of performance, but it certainly is not the most cost effective or efficient in terms of cost of operation. Systems designers find it challenging to implement a system with multiple ADCs. For example, a phased array radar implementation will contain hundreds of AD9680s all working synchronously. It is unreasonable to ask the systems designer to have one LDO regulator per voltage domain across hundreds of ADCs.

A Simpler PDN for GSPS ADCs

A more cost-effective approach to the PDN design would be to combine the domains that have the same voltage value (such as all having 1.25 V analog domains) and drive them from the same LDO. This reduces the component count (and bill of material—BOM—cost) and may be suitable for some designs. The simplified PDN is shown in Figure 2 as implemented on the AD9680 evaluation board. In this implementation, the entire AD9680 can be powered using a single 3.3 V input.

A DC–to–DC Converter Driving the AD9680

A further simplification to the PDN can be implemented by removing the LDO that supplies the 1.25 V domains altogether. This would be the most efficient and cost-effective solution. The challenge here is to ensure stable operation to the dc-to-dc converter so as to not affect the ADC's performance. The PDN where the ADP2164 drives all the 1.25 V domains (AVDD1, AVDD1_SR, DVDD, and DRVDD) of the AD9680 is shown in Figure 3.
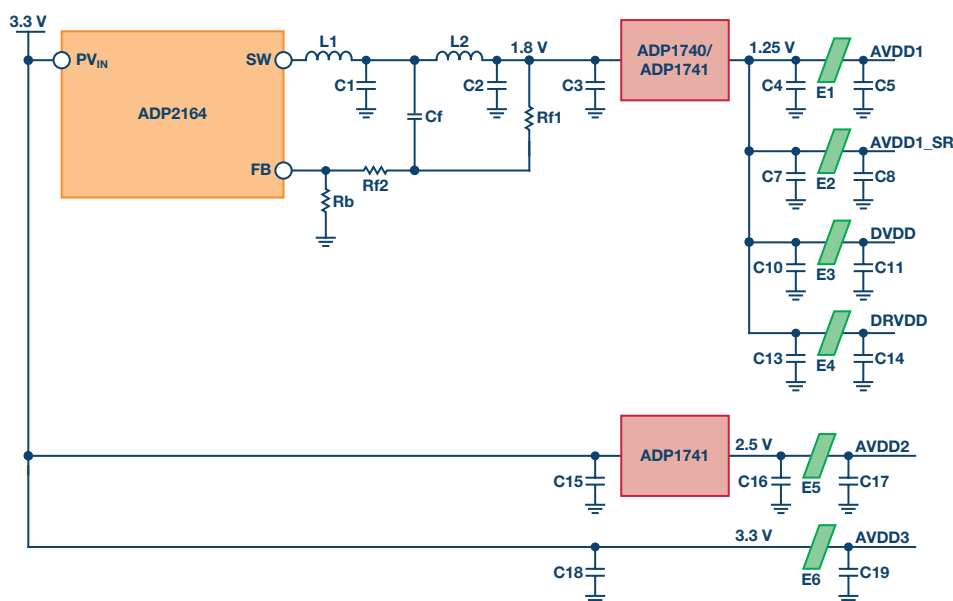

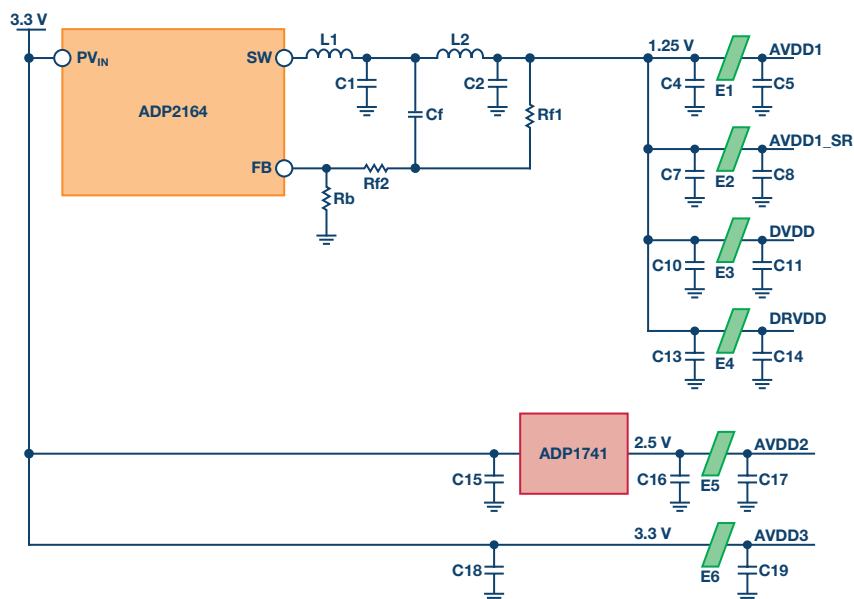Figure 2: Simplified PDN for the AD9680 evaluation board.

Figure 3: Using a dc-to-dc converter to power the AD9680.

Comparing the Various PDNs

The three PDNs discussed above were put to test along with a fourth network where the AD9680 evaluation board was powered from the bench supplies. Table 1 lists the various power delivery networks implemented on the AD9680 evaluation board.

Table 1. List of Power Delivery Networks

PDN Setup	Description
Bench	AD9680 run using bench supply
PDN #1	Default PDN on evaluation board (shown in Figure 1)
PDN #2	All 1.25 V domains driven from one LDO (shown in Figure 2)
PDN #3	All 1.25 V domains driven from a dc-to-dc converter (shown in Figure 3)

Since SPIVDD could support 1.8 V to 3.3 V and was considered a noncritical node, it was powered using a 1.8 V LDO output. In a regular system implementation, the SPIVDD can be connected to the 2.5 V or 3.3 V domain. That said, the SPIVDD connection should still be monitored in systems where the SPI bus is shared between many ADCs and DACs. If this is the case, care must be taken to ensure that the normal SPI operation does not cause supply transients on the SPIVDD domain. Their supply transients might trigger a power-on reset (POR) situation if the SPIVDD goes lower than the threshold level.

Table 2. SNR Performance Comparison (dBFS)

Frequency (MHz)	Bench	Default (PDN #1)	Simplified (PDN #2)	Switcher (PDN #3)
63	66.5	66.5	66.6	66.7
170	66.4	66.1	65.9	66.2
340	64.8	64.5	64.5	64.7
450	64.0	63.7	63.6	63.8
765	62.5	62.2	62.2	62.3
985	61.3	61.0	61.0	61.1
1283	59.8	59.5	59.5	59.5
1725	57.7	57.4	57.4	57.5
1983	56.7	56.4	56.5	56.6

Table 3. SFDR Performance Comparison (dBFS)

Frequency (MHz)	Bench	Default (PDN #1)	Simplified (PDN #2)	Switcher (PDN #3)
63	83	82	88	83
170	86	85	85	84
340	77	76	76	76
450	72	72	71	71
765	77	76	76	82
985	77	76	76	83
1283	74	74	74	75
1725	67	67	68	67
1983	60	60	60	60

Table 2 and Table 3 show the SNR and SFDR performance, respectively, of the AD9680 when using the various PDNs. The recommendations for front-end network and register settings for various Nyquist zones were followed as per the AD9680 data sheet.[2]

The PDN using just the dc-to-dc converter to power the AD9680's 1.25 V domains (PDN #3) shows good performance over the input frequencies. This proves that it is possible to combine domains and power them efficiently and cost effectively without paying a huge penalty in ADC performance. The PDN supplied from the bench provides the best noise performance as it is the lowest noise power source. However, it is worth noting that PDN #3 consistently shows better SNR performance than the default network (PDN #1). This could be attributed to the fact that LDOs are good for low frequency cleanup but do not do much above a few 100 kHz even when they are in the circuit. This could explain the 0.2 dB advantage in SNR when using the PDN #3.

FFT Plots

Figure 4 and Figure 5 show the single tone FFTs at 170 MHz and 785 MHz input, respectively. The FFT shows no spectral degradation due to the fact that the 1.25 V domains have been powered from a single dc-to-dc converter.
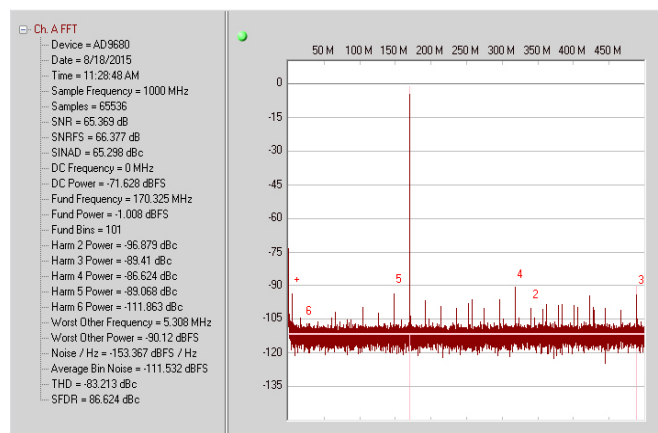

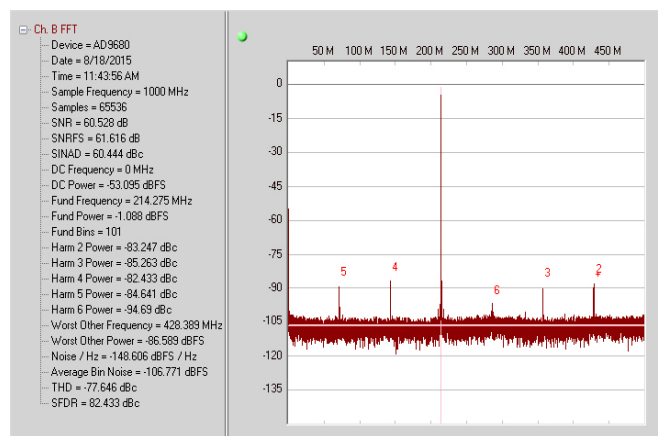
Figure 4. Single–tone FFT at 170 MHz input, with PDN #3.

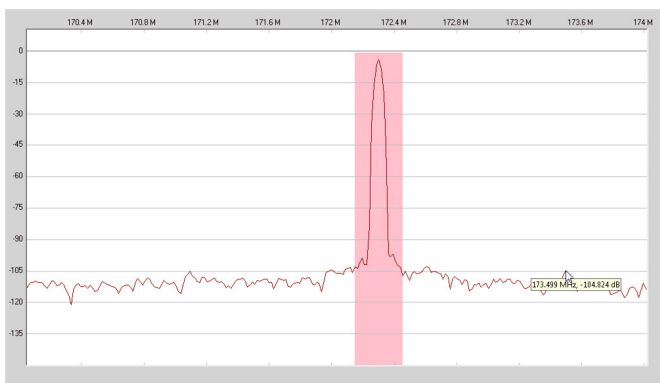*Figure 5. Single–tone FFT at 785 MHz input, with PDN #3.*

Figure 6. 1.2 MHz sideband switching spur at 170 MHz input.
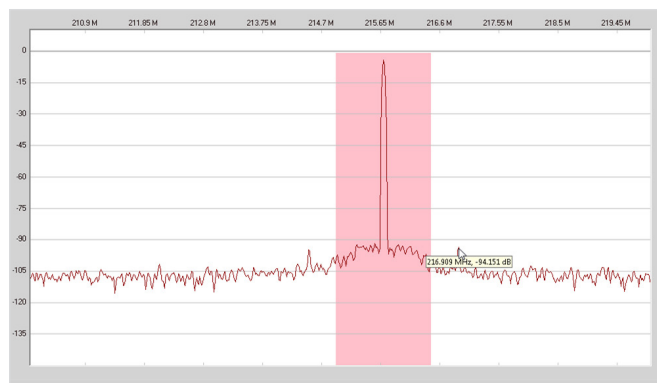Spur level = −105 dBFS.

Figure 7. 1.2 MHz sideband switching spur at 785 MHz input.
Spur level = −94 dBFS.

Switching Spurs

In addition to the noise performance, the dc-to-dc converter implementation should also be checked for spurious content due to the switching elements and the magnetics involved. This is where careful layout techniques to reduce ground loops and ground bounce will be beneficial. There are many resources that can help with measurement of the switching supply noise.[5,6] The sideband spurs appear on either side of the fundamental offset by the switching frequency (in this example, 1.2 MHz). It must be noted that the output filter stage shown in Figure 2 or Figure 3 is a two-stage filter. This two-stage filter is a main contributor in reducing the switching noise (ripple) that helps improve the ADC noise (SNR) performance. In the same token, the two-stage filter also helps in reducing the switching spurs that manifest itself in the output FFT. These are shown in Figure 6 and Figure 7 for 170 MHz and 785 MHz, respectively.

The level of the sideband spur can be estimated by understanding the PSRR (power supply rejection ratio) or the ADC's power supply domain.[7]

Simulating DC–to–DC Converter Switching Circuits

The two-stage filter at the output of the dc-to-dc converter can be simulated using a tool such as ADIsimPE.[8] Figure 8 shows the ADIsimPE schematic generated to simulate the output

noise and stability characteristics of the PDN. ADIsimPE is a convenient and powerful tool that helps the systems engineer design, optimize, and analyze power supply networks.

Figure 9 shows the output ripple at the output of the first stage and the filtered output after the second stage of the circuit, simulated in ADIsimPE. The ripple as shown here is around 3 mV p-p.
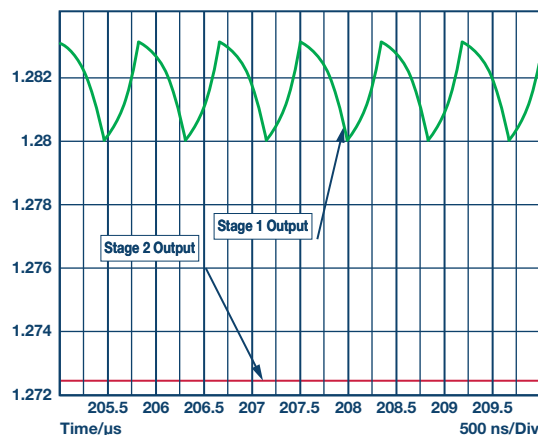

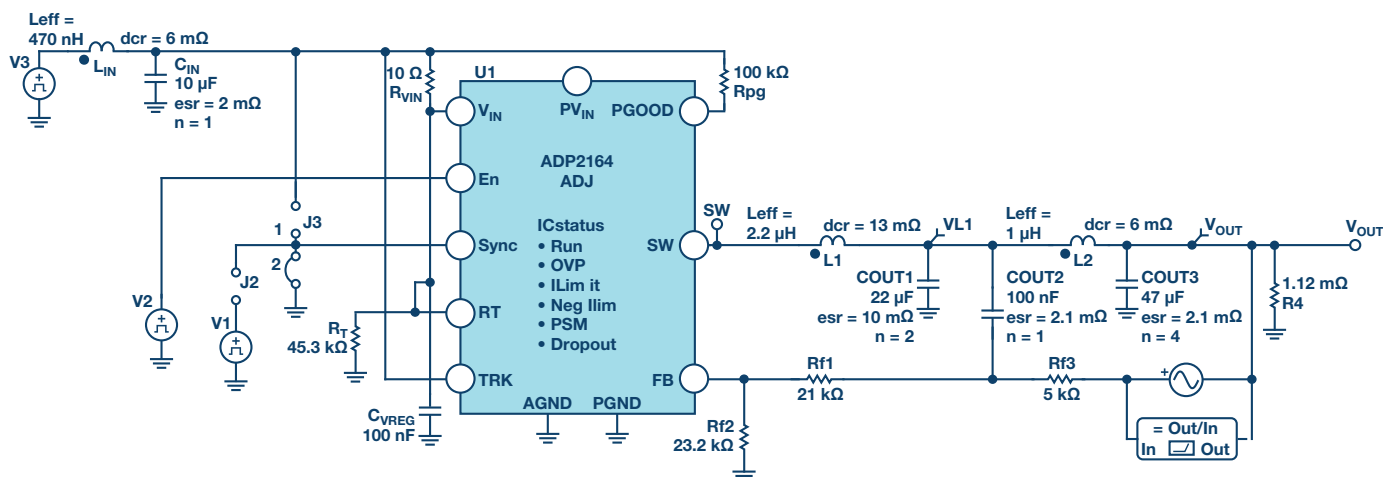Figure 9. Stage 1 and Stage 2 outputs of the ADIsimPE simulation.

Figure 8. ADIsimPE schematic of ADP2164 driving the 1.25 V domains.

Table 4. Bill of Material of PDN Shown in Figure 2

REFDES	Qty	Description	MFG	Part Number	Value
C1	1	22 µF, 6.3 V, X5R 0805 capacitor	Murata	GRM21BR60J226ME39L	22 µF
C2	4	22 µF, 6.3 V, X5R 0805 capacitor	Murata	GRM21BR60J226ME39L	22 µF
Cf	1	0.1 µF, 10 V, X5R 0402 capacitor	Murata	GRM155R61A104KA01D	0.1 µF
C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	17	4.7 µF, 6.3 V, X5R 0402 capacitor	Murata	GRM155R60J475ME47D	4.7 µF
E1, E2, E3, E4, E5, E6	6	Ferrite chip 10 Ω 0402	Murata	BLM15AX100SN1D	10 Ω
L1	1	1.0 µH shielded power inductor, 10 mΩ	Coilcraft	XAL5030-102ME	1.0 µH
L2	1	2.2 µH shielded power inductor, 0.1 Ω	Coilcraft	ME3220-222ML	2.2 µH
Rf1	1	4.99 kΩ, 1% 1, W/10 W 0402 resistor	Panasonic	ERJ-2RKF4991X	4.99 kΩ
Rf2	1	41.2 kΩ, 1% 1, W/10 W 0402 resistor	Panasonic	ERJ-2RKF4122X	41.2 kΩ
Rb	1	23.2 kΩ, 1% 1, W/10 W 0402 resistor	Panasonic	ERJ-2RKF2322X	23.2 kΩ
ADP2164	1	IC, REG, buck ADJ, 4 A, sync, 16-lead LFCSP	Analog Devices	ADP2164ACPZ-R7	
ADP1741	3	IC, REG, LDO, ADJ, 2 A, 16-lead LFCSP	Analog Devices	ADP1741ACPZ-R7	
ADP171	2	IC, REG, LDO, ADJ, 0.3 A, 5-lead TSOT-23	Analog Devices	ADP171AUJZ-R7	

Bill of Material

Table 4 shows the bill of material used for the simplified PDN of the AD9680 evaluation board, which is shown in Figure 2. By using the network shown in Figure 3, a systems designer can realize savings of up to 40% to 45% in BOM cost. The BOM cost is estimated by calculating the 1k unit prices of the components on a popular electronic component vendor website.

Component Selection and Layout

The performance of the ADC when running on the various PDNs depends on not only careful design, but also the selection of components and their layout on the PCB. The high currents produced in a switching power supply often lead to strong magnetic fields that can couple into other magnetic components on the board, including inductors found in matching networks and transformers used to couple analog and clock signals. Careful board layout techniques must be utilized to prevent these fields from coupling into critical signals.

Inductor Selection

Since the inductor and the capacitor that form the output filter stage perform the bulk of the power delivery, they need to be selected carefully. In this example, a mix of shielded and unshielded inductors were used. The first filter stage used a shielded inductor. The second stage could do with an unshielded inductor in this case. However, it is recommended to use shielded inductors in both stages to minimize possible EMI emissions. The inductors also were chosen to have enough headroom in terms of saturation current (ISAT) and dc resistance (DCR) to make sure they didn't go into saturation or cause too much voltage drop across themselves.

Capacitor Selection

X5R or X7R capacitors are recommended for use as output filter capacitors. The capacitors also have to have low ESR (equivalent series resistance). The low ESR helps in reducing switching ripple at the output. Another trick that is employed to minimize the total ESR and ESI (equivalent series inductance) is to combine capacitors in parallel. As shown in Figure 3 and Table 4, the first filter stage uses 2× 22 µF capacitors, whereas the second filter stage uses 4× 22 µF capacitors. The voltage rating of the capacitors is also an important factor in its selection. This is because the dielectric of the ceramic capacitor degrades as the dc bias increases. This means that a 6.3 V rated 22 µF capacitor could degrade by up to 50% at a 4 V dc bias.[9,10] In this example, the 6.3 V rated capacitor is used for the 1.25 V supplies. Adding more capacitors at the output does increase the BOM cost and board space slightly but this is a good insurance against switching noise and ripple that could interfere with ADC performance.

Ferrite Bead Selection

As shown in Figure 3, ferrite beads are used to isolate the various domains. The selection of the ferrite bead is also critical, as a higher than desired DCR (dc resistance) of the ferrite bead will cause lower than optimal voltage at the domains. This low voltage results in less than optimal ADC performance (SNR and SFDR). Sufficient attention must be paid to the impedance characteristics, maximum dc carrying capability, and the DCR of the ferrite bead.[11]

PCB Layout Considerations

In order to minimize the interactions between the switching regulator and the ADC, the dc-to-dc converter and its switching elements should be placed far away from any magnetics that interact with the ADC (such as the front-end matching network or clock network). Within the dc-to-dc converter layout, the two stage filter should be placed as close to the dc-to-dc converter as possible so as to minimize loop currents.

Acknowledgement

Conclusion

RF sampling (or GSPS) ADCs offer a unique advantage in systems design by allowing the digitization of wide swaths of bandwidth. The industry is keen on reducing the complexity, size, and cost of power supply designs for these GSPS ADCs. It is possible to have a low noise and cost-effective PDN that can power a GSPS ADC by paying adequate attention to the design, component selection, and PCN layout. Thus implemented, switching regulators also help improve power system efficiency and provide operational cost and BOM savings, without any penalty in performance.

References

[1] AD9250. Analog Devices.

[2] AD9680. Analog Devices.

[3] ADP2384. Analog Devices.

[4] ADP2164. Analog Devices.

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Umesh Jayamohan

Umesh Jayamohan [umesh.jayamohan@analog.com] is an applications engineer with Analog Devices in the High Speed Converter Group (Greensboro, NC). He has been a part of Analog Devices since 2010. Umesh received his B.S.E.E. from the University of Kerala, India, in 1998 and his M.S.E.E. from Arizona State University in 2002.

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