Integrated Multiplexed Input ADC Solution Alleviates Power Dissipation and Increased Channel Density Challenges

By Maithil Pachchigar

Introduction

An increased number of applications in industrial, instrumentation, optical communication, and healthcare industries use multichannel data acquisition systems that result in increased printed circuit board (PCB) density and thermal power dissipation challenges. The need for increased channel density in these applications is driving the demand for a high channel count, low power and compact form factor integrated data acquisition solution. These applications also demand precision measurements, reliability, affordability, and portability. System designers make trade-offs among performance, thermal stability, and PCB density to maintain optimum balance and they are continually pressed to find innovative ways to tackle these challenges while minimizing overall bill of material (BOM) cost. This article highlights the design considerations for multiplexed data acquisition systems and focuses on an integrated multiplexed input ADC solution to address these technical challenges for space constrained applications such as optical transceivers, wearable medical devices, the Internet of Things (IoT), and other portable instruments. The proposed low power solution using integrated, multiplexed input 4-channel/8-channel, 16-bit, 250 kSPS PulSAR® ADCs AD7682/AD7689 available in a miniature, 2.39 mm × 2.39 mm, wafer level chip scale package (WLCSP) footprint saves over 60% board space to address the challenges for increased channel density and battery-powered portable systems while offering a flexible configuration and precision performance.

Multiplexed Data Acquisition Systems

Multichannel data acquisition systems typically employ different types of discrete single-channel or integrated multiplexed and simultaneously sampled analog signal chains for interfacing with various sensor types such as temperature, pressure, optical, vibration, and many more based on application requirements. For example: multiplexing multiple input channels into a single ADC, using individual track and hold amplifiers, and multiplexing them into a single ADC, and using individual ADCs to allow the simultaneous sampling of each channel. The successive approximation register (SAR) analog-to-digital converter (ADC) is typically used in the first case, as shown in Figure 1. It offers significant power, space, and cost savings, where individual channels may need low-pass antialiasing filter at inputs, and their channel switching and sequencing are properly synchronized with the ADC conversion time. In the second case, as shown in Figure 2, the achievable throughput rate is divided by the number of channels simultaneously sampled, but the constant phase between the sampled channels can still be maintained. As shown in Figure 3, some applications require a dedicated amplifier and ADC on a per channel basis for simultaneously sampling the inputs to obtain an increased sampling rate per channel and to preserve the phase information at the expense of additional area and power. The simultaneous sampling ADCs are typically used in automated test equipment, power line monitoring, and multiphase motor controls that require continuous sampling at a higher throughput rate per channel to preserve the phase information between channels for accurate instantaneous measurements.

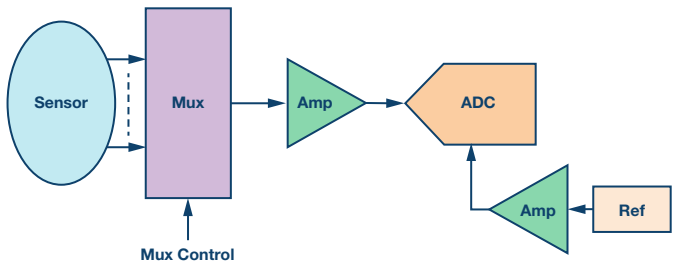

Figure 1. Simplified multichannel data acquisition signal chain case I.

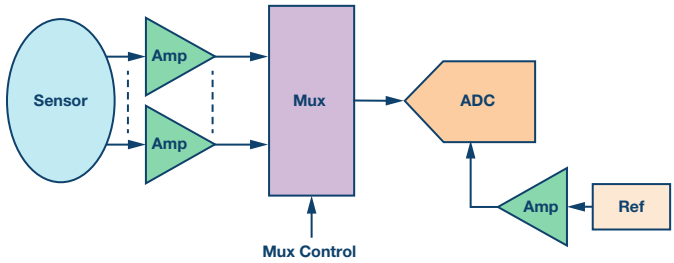

Figure 2. Simplified multichannel data acquisition signal chain case II.

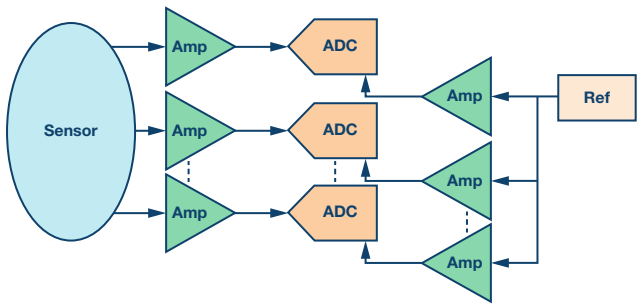

Figure 3. Simplified multichannel data acquisition signal chain case III.

The key benefit of multiplexing is that a fewer number of ADCs per channel are required, resulting in reduced space, power, and cost. However, the achievable throughput rate in a multiplexed system is the single ADC throughput rate divided by the number of channels being sampled. The SAR ADCs offer inherent merits of low latency and dynamic power scaling with throughput. They are often used in channel multiplexed architectures ideally suited for sensing and monitoring functions. Multiplexed data acquisition systems utilized in optical transceiver modules need high channel density and wearable medical devices require small form factors and low power, where the signals from multiple sensors need to be monitored and multiplex many input channels into a single or several ADCs. One of the main challenges with multiplexed data acquisition systems is that when the input is switched to the next channel, it requires a fast response to step input near full-scale amplitude to minimize any settling time or crosstalk issue. The following section presents a real-world use case of an SAR architecture-based multiplexed input ADC for optical transceivers and wearable electronic devices. It explains why the AD7689 is ideally suited for these types of applications.

Optical Transceivers

The market for 100 Gbps optical transceivers is uniquely positioned to grow in the next decade for high speed coherent optical transmission. The key challenge for optical transceivers is to acquire and process wider bandwidth signals or multiplex a number of input channels at lower power in a smaller footprint. The size, power, and cost structure of today's transceivers originally designed for long haul applications limit their utilization in more cost-sensitive metro networks. The metro networks include: metro regional 500 km to 1000 km, metro core 100 km to 500 km, and metro access <100 km applications. Due to fierce competition in metro networks, the space comes at a high premium, making line-card density extremely crucial and, consequently, a path to lower cost optical line cards or pluggable modules in a smaller footprint has become increasingly important for coherent applications.

In optical networks, as the bit rates per channel increases from 10 Gbps toward 100 Gbps and higher, the optical fiber nonidealities severely degrade signal quality and affect its transmission performance. Technical challenges also arise in long haul optical networks when the penalties occur in terms of optical noise, nonlinear effects, and dispersion due to optical fiber impairment. To address these significant challenges, various manufacturers of 40 Gbps and 100 Gbps optical transceivers use coherent technology that allow higher data rate connectivity with maximum reach at longer distances for metro long haul, long haul, and ultralong haul networks. The coherent technology generally combines multilevel signal formats and coherent detection using dual polarization, quadrature, phase-shift keying (DP-QPSK) for optimized signal modulation, allowing immunity to fiber impairments at higher data rates, and making 100 Gbps transmission economically and technically feasible. The next generation of 100 Gbps (and above) data rate optical transceivers will require lower power consumption and a miniature form factor to allow increased channel density for significant space, power, and cost savings. Depending on the requirements, the channel count typically varies anywhere from eight to 64 in an optical system. The component placement and trace routing become prominent for the PCB designers, especially for high channel density system.

A simplified block diagram of generic optical module is shown in Figure 4, which includes transmitter, receiver, micro-ITLA (integrated tunable laser assembly), and data acquisition components. Figure 5 shows the simplified block diagram of a micro-ITLA, which is a wideband electronically tunable laser device that controls rapid wavelength switching. The transmitter includes a Mach-Zehnder driver and modulator to control the amplitude or intensity of the exiting laser light. The multiplexed input ADC is typically used in control and monitoring functions to digitize the data from the multiple channels in optical module and micro-ITLA.

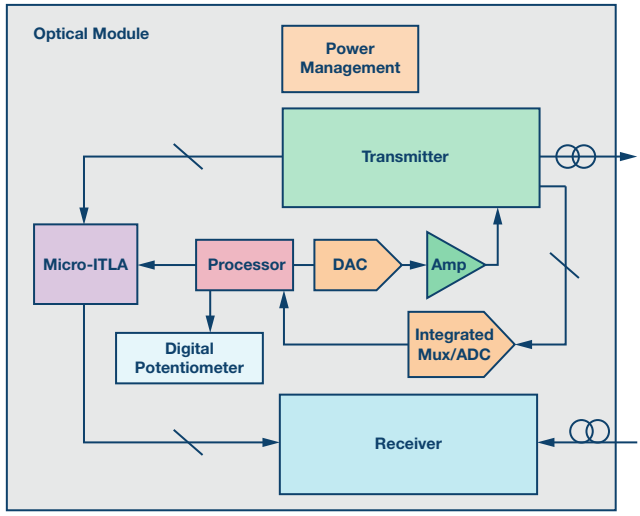

Figure 4. Simplified block diagram of an optical module.

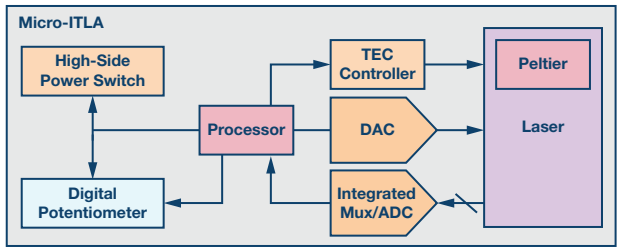

Figure 5. Simplified block diagram of a microintegrated tunable laser assembly.

Vital Sign Monitoring Using Wearable Electronic Devices

A high level block diagram of a typical wearable electronic device is shown in Figure 6. Modern wearable electronic devices integrate various sensors to accurately monitor multiple human biometrics in real-time. They offer flexible user interface for data storage and data transmission through Wi-Fi to a personal smartphone, tablet, or laptop. They use biopotential, bioimpedance, or optical sensors to derive information about multiple vital signs such as the heart rate, respiration rate, and oxygen saturation level in blood (SpO_2). The acoustical sensor is used to extract information about blood pressure and dietary activities, and the temperature sensor is used to measure body temperature. The MEMS-based inertial motion sensor (accelerometer) is used to track daily physical activity. The signals from different sensors require analog signal conditioning, which are then multiplexed into an ADC. Some of the signals might need to get sampled simultaneously as well, depending on the system. The ADC then digitizes these signals and the processor or microcontroller finally postprocess them to extract information about numerous physiological measures.

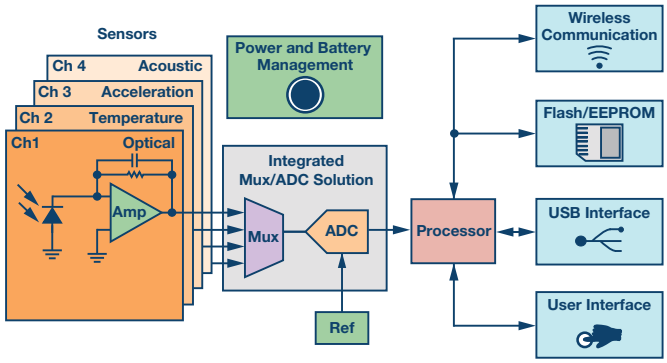

Figure 6. A simplified block diagram of wearable electronic device.

An electrocardiogram (ECG) has traditionally been used to monitor heart activity, which is critical for physiological monitoring and cardiac diagnosis. However, smart wearable systems use optical and bioimpedance sensors that allow integration of heart rate monitors in wearable electronic devices such as wrist-worn watches, bands, or activity trackers.

In optical systems, rapidly flashing infrared light is transmitted through the skin surface and a photodetector measures the light absorbed by the red blood cells. The analog front end conditions and digitizes this tiny signal, which is then post-processed to extract information about multiple physiological variables such as the heart rate, respiration rate, and SpO_2 using a photoplethysmographic (PPG) technique.

The bioimpedance sensors consumes much less power compared to other technology such as optical, extending battery life. Bioimpedance sensors can be used to measure the respiration rate or skin impedance. A sinusoidal signal is injected into the skin (body tissue) through electrodes and a tiny current flow through is measured, digitized, and postprocessed to accurately interpret various physiological signals like the respiration rate, skin conductance, or water in the lungs.

These devices demand highly integrated and very sensitive, cost-effective, power efficient battery-powered solution that can fit into a miniaturized module. They must reliably and accurately monitor multiple physiological variables while offering increased immunity to motion generated artifacts and external environmental conditions, otherwise they can obscure the true signal with noise, leading to inaccurate readings. Therefore, it is important to have good noise performance of the ADC and oversampling or averaging is often used to improve the overall dynamic range. The input frequency band of interest is from dc to 250 Hz, so ADC sampling rates are close to a few kilosamples per second (kSPS).

Integrated Multiplexed Input 4-Channel/8-Channel, 16-Bit, 250 kSPS ADCs

The AD7682/AD7689 is the industry's leading integrated, multiplexed input 4-channel/8-channel, 16-bit, 250 kSPS SAR-based ADC manufactured on Analog Devices' proprietary 0.5 µm CMOS process. The integrated 4-channel/8-channel low crosstalk multiplexer introduces minimal mismatch from between adjacent channels and allows sequential sampling. These ADCs allow the choice of a very low temperature drift internal 2.5 V or 4.096 V precision voltage reference, an external reference, or an external buffered reference and on-board temperature sensor monitors the typical internal temperature of the ADC. This eliminates the need for external components, significantly saving PCB area and BOM cost. They include a channel sequencer useful for scanning channels as singles or pairs, with the internal temperature sensor enabled or disabled in a repeated fashion. It offers a flexible serial digital interface compatible with SPI, MICROWIRE, QSPI, and other digital hosts. Its 14-bit internal configuration register allows the user to select various options including a number of channels to be sampled, a reference, a temperature sensor, and a channel sequencer. The interface allows a 4-wire read during conversion, read after conversion, and read spanning conversion modes with and without a busy indication. The AD7682/AD7689 is ideally suited for high channel density applications such as optical transceivers, wearable medical devices, and other portable instruments for precision sensing and monitoring.

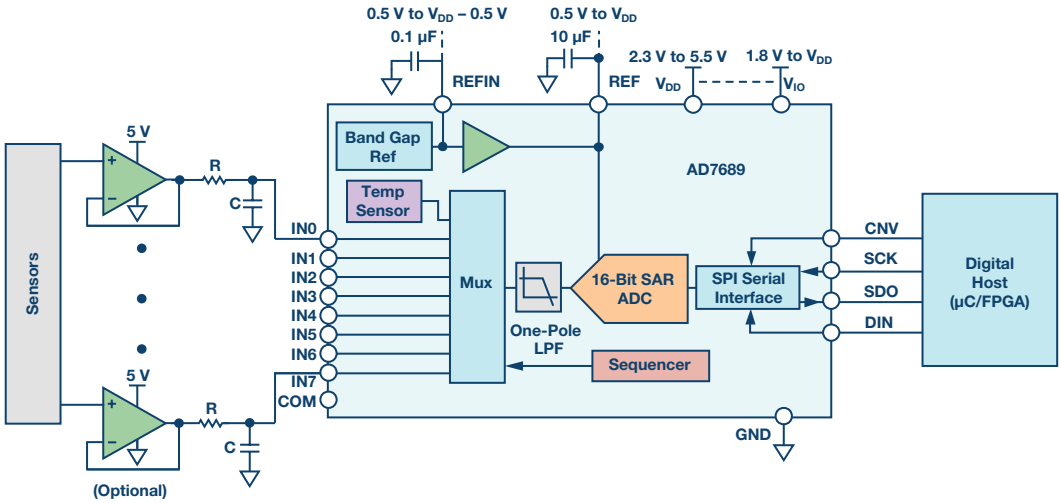

Figure 7. AD7689 typical application diagram (all connections and decoupling not shown).

The Figure 7 shows a simplified AD7689 block diagram for a multichannel data acquisition system, which offers easy to use flexible configuration options and precision performance. It solves the complex design issues related to the channel switching, sequencing, and settling time and it saves design time.

For multichannel, multiplexed applications, some designers use a low output impedance buffer to handle the kickback from the multiplexer inputs depending on the throughput rate used. The input bandwidths of the SAR ADC (tens of MHz) and ADC driver (tens to hundreds of MHz) are higher than the sampling frequency, whereas the desired input signal bandwidth is typically in the tens of Hz to hundreds of kHz range. Therefore, depending on the system requirements, a single-pole, low-pass RC antialiasing filter may be required at the input of the multiplexer to eliminate unwanted signals (aliases) from folding back into the bandwidth of interest, to limit the noise and to reduce settling time issues. The value of the RC filter used at each input channel should be carefully selected based on the following trade-off because too much band limiting can affect settling time and increase distortion; if the capacitance is large, it will help attenuate the kickback from the multiplexer, but it can also make the previous amplifier stage unstable by degrading its phase margin. C0G or NP0 type capacitors are recommended for an RC filter that has a high Q, low temperature coefficient, and stable electrical characteristics under varying voltages. A reasonable value of series resistance should be chosen to keep the amplifier stable and limit its output current. The resistance cannot be too large or the ADC driver will not be able to recharge the capacitor after the multiplexer kickback.

Small Form Factor

The AD7682/AD7689 is now available in 2.39 mm × 2.39 mm, pin-compatible, wafer level chip scale package (WLCSP), which is an over 60% smaller form factor compared to its existing 4 mm × 4 mm lead frame chip scale package (LFCSP) or other competitive device of its class, allowing increased circuit density in a small system footprint. Figure 8 compares the miniaturized size of its WLSCP with the size of a standard 6 mm pencil.

Figure 8. Size comparison of AD7682/AD7689 wafer level, chip scale package with a standard pencil.

The active side of the of AD7682/AD7689 WLCSP die is inverted and can be connected to the PCB using solder balls and its dimensions after PCB assembly are as shown in Figure 11. The actual separation between the surface of the die and the substrate (standoff) after PCB assembly varies with the amount of solder screen printed on to the substrate and pad diameter.

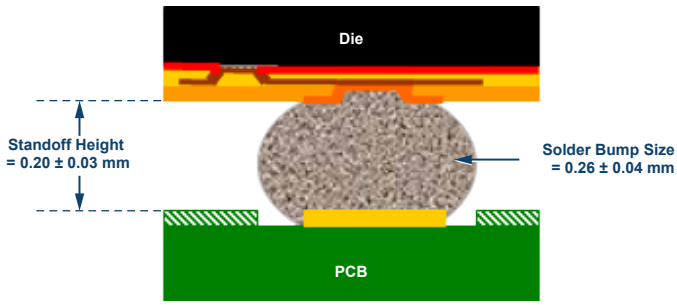

Figure 9. AD7682/AD7689 WLCSP dimensions after PCB assembly.

Low Power Dissipation

The AD7682/AD7689 requires an analog and digital core supply (V_{DD}) and a digital input/output interface supply (V_{IO}) for a direct interface with any logic between 1.8 V and V_{DD}. The V_{DD} and V_{IO} pins can also be tied together to save on the number of supplies required in the system, and they are independent of power supply sequencing. Powered from 5 V (V_{DD}) and 1.8 V (V_{IO}) supplies, its power scales linearly with throughput rate, enabling very low power consumption—

typically around 1.7 µW typ at 100 SPS and 12.5 mW at 250 kSPS with a 5 V external reference, as shown in Figure 10. This makes the ADC power efficient and well-suited for both high and low sampling rates even as low as a few Hz and for portable and battery-powered systems. One of the key features of this part is that it powers down automatically at the end of each conversion phase and consumes a very low standby current of typically only 50 nA, allowing conservation of the battery when the device is not utilized, thus extending battery life.

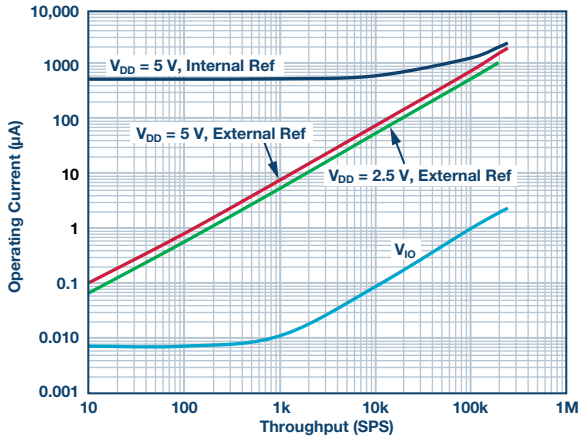

Figure 10. AD7682/7689 operating current vs. throughput.

Precision Performance

For applications that require multiple AD7682/AD7689 devices, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk. The best SNR is achieved with a 5 V external reference since the internal reference is limited to 4.096 V. It offers excellent ac and dc performance in terms of INL of ±1.5 LSB, signal-to-noise plus distortion ratio (SINAD) of ~93 dB and an effective number of bits (ENOB) of ~15.2 bits using a 5 V external reference for a 2 kHz input tone while running at the full speed of 250 kSPS. Figure 11 shows the typical performance of SNR, SINAD, and ENOB for a given external reference voltage utilized.

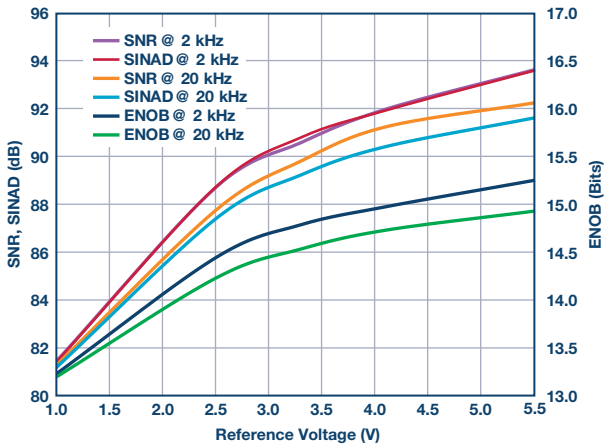

Figure 11. AD7682/7689 SNR, SINAD, and ENOB vs. reference voltage.

Conclusion

The next generation of pluggable optical transceiver modules and other portable systems demand power efficient data acquisition system in a small, low cost form factor. The AD7682/AD7689, with industry leading integration and precision performance, supports a wide range of sensor interfaces and enables designers to differentiate their systems while meeting stringent user requirements. This power efficient integrated ADC solution addresses the increased circuit density and thermal power dissipation challenges for space constrained applications by saving over 60% space compared to its existing LFCSP and competitive offerings, which is well-suited for both high and low sampling rates applications.

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A Low Power Data Acquisition Solution for High Temperature Electronics Applications

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